Low-Power, RRIO, 1MHz Operational Amplifier for Cost-Sensitive Systems

General Description

The ET8500X series are low voltage (1.8V to 5.5V) operational amplifiers included single-channel (ET85001) and dual-channel (ET85002) and quad-channel (ET85004) with rail-to-rail input and output swing capabilities.These op amps provide a cost-effective solution for space-constrained applications such as smoke detectors, wearable electronics, and small appliances where low-voltage operation and high capacitive-load drive are required. The capacitive-load drive is 500 pF and the resistive open-loop output impedance makes stabilization easier with much higher capacitive-loads. ET8500X features unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions.

The ET8500X are specified for the extended industrial/automotive temperature range (-40°C to +125°C).

The ET85001 single amplifier is available in SOT23-5, SC70-5, DFN4, and SOP8 packages.

The ET85002 dual amplifier is available in MSOP8, SOP8 packages.

The ET85004 quad amplifier is available in a TSSOP14 package.

Features

- Low input offset voltage: ±0.4 mV (Typ)
- Unity-gain bandwidth: 1 MHz (Typ)
- Low broadband noise: 27 nV/$\sqrt{Hz}$ (Typ)
- Low input bias current: 5 pA (Typ)
- Low quiescent current: 60 μA/Ch (Typ)
- Rail-to-rail input and output
- Unity-gain stable
- Internal RFI and EMI filter
- Operational at supply voltages as low as 1.8 V
- Easier to stabilize with higher capacitive load
- Extended temperature range: -40°C to 125°C

Applications

- Temperature sensors
- Sensor signal conditioning
- Power modules
- Active filters
- Low-side current sensing

Device information

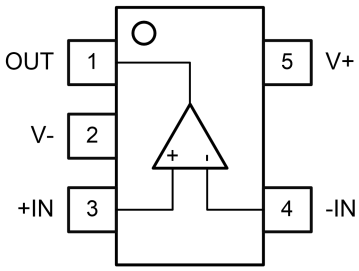
ET 8500 X① X②

X① Channel number	
1	Single channel
2	Dual channel
4	Quad channel

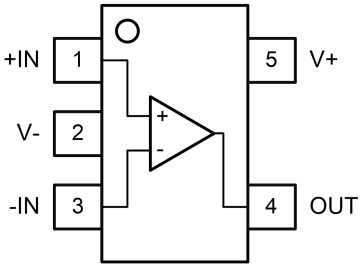
X② Package		
M		SOP8
U		MSOP8
V		TSSOP14
D		DFN4(0.8×0.8)
E	EA	SOT23-5
SC	SCA	SC70-5

Part No.	Package	Packing Option	Marking	MSL
ET85001E	SOT23-5	Tape and Reel , 3k/Reel	85001 XXXXX	3
ET85001EA	SOT23-5	Tape and Reel , 3k/Reel	85001A XXXXX	3
ET85001SC	SC70-5	Tape and Reel , 3k/Reel	85001 XXXXX	1
ET85001SCA	SC70-5	Tape and Reel , 3k/Reel	801A XXXXX	1
ET85001D	DFN4(0.8×0.8)	Tape and Reel , 3k/Reel	1X	1
ET85001M	SOP8	Tape and Reel , 4k/Reel	801M XXXXX	3
ET85002M	SOP8	Tape and Reel , 4k/Reel	85002 XXXXX	3
ET85002U	MSOP8	Tape and Reel , 4k/Reel	802U XXXXX	3
ET85004V	TSSOP14	Tape and Reel , 4k/Reel	804 XXXXX	3

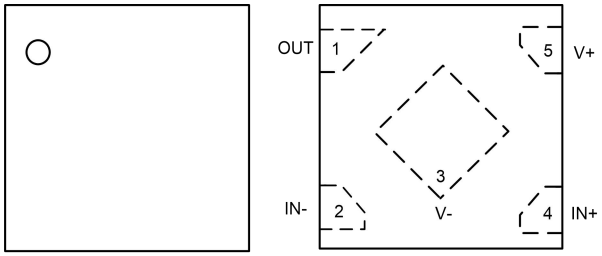
Pin Configuration



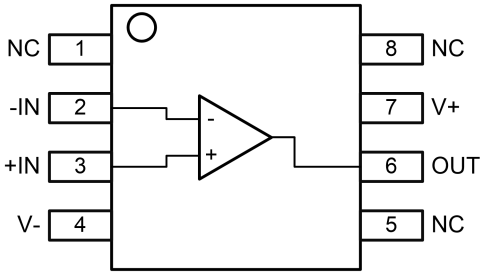
ET85001EA/SCA



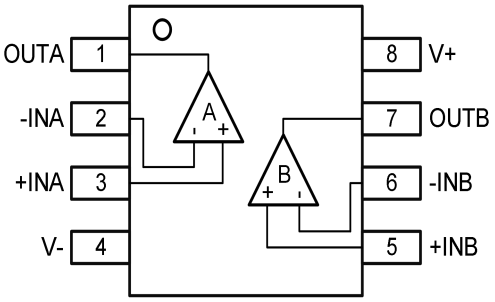
ET85001E/SC



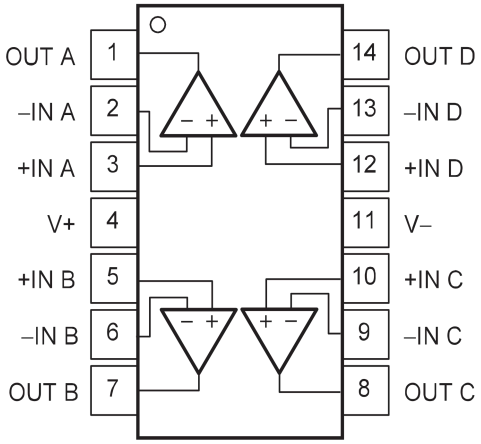
ET85001D



ET85001M



ET85002M/U



ET85004V

Top View

Pin Function

	Pin Number	Symbol	Descriptions
ET85001M	1	NC	/
	2	-IN	Inverting input
	3	+IN	Non-inverting input
	4	V-	Negative supply
	5	NC	/
	6	OUT	Output
	7	V+	Positive supply
	8	NC	/

	Pin Number	Symbol	Descriptions
ET85001EA ET85001SCA	1	OUT	Output
	2	V-	Negative supply
	3	+IN	Non-inverting input
	4	-IN	Inverting input
	5	V+	Positive supply

	Pin Number	Symbol	Descriptions
ET85001E ET85001SC	1	+IN	Non-inverting input
	2	V-	Negative supply
	3	-IN	Inverting input
	4	OUT	Output
	5	V+	Positive supply

	Pin Number	Symbol	Descriptions
ET85001D	1	OUT	Output
	2	-IN	Inverting input
	3	V-	Negative supply
	4	+IN	Non-inverting input
	5	V+	Positive supply

	Pin Number	Symbol	Descriptions
ET85002M ET85002U	1	OUTA	Output
	2	-INA	Inverting input
	3	+INA	Non-inverting input
	4	V-	Negative supply
	5	+INB	Non-inverting input

	6	-INB	Inverting input
	7	OUTB	Output
	8	V+	Positive supply

	Pin Number	Symbol	Descriptions
ET85004V	1	OUTA	Output
	2	-INA	Inverting input
	3	+INA	Non-inverting input
	4	V+	Positive supply
	5	+INB	Non-inverting input
	6	-INB	Inverting input
	7	OUTB	Output
	8	OUTC	Output
	9	-INC	Inverting input
	10	+INC	Non-inverting input
	11	V-	Negative supply
	12	+IND	Non-inverting input
	13	-IND	Inverting input
	14	OUTD	Output

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are only stress ratings, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Symbol	Parameter	Value	Unit
V_S	Supply Voltage[(1)] (V+) - (V-)	0 to 6	V
V_{IN}	Signal input terminals Voltage	(V-)-0.3V to (V+)+0.3	V
V_{ID}	Differential Input Voltage	(V+) - (V-)+0.2	V
V_{ESD}	ESD (Human Body Model)	±2000	V
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_J	Junction Temperature Range	-65 to +150	°C
T_A	Operating Temperature Range	-40 to +125	°C

Note1:All voltage values, except differential voltage are with respect to network terminal.

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_S	Supply Voltage: (V+) - (V-)	1.8(±0.9) ~ 5.5(±2.75)	V
T_A	Operating Temperature Range	-40 ~ +125	°C

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	SOP8	Thermal Characteristics, Thermal Resistance, Junction-to-Air	160	°C/W
	MSOP8		200	°C/W
	SOT23-5		233	°C/W
	SC70-5		240	°C/W
	DFN4(0.8×0.8)		250	°C/W
	TSSOP14		148	°C/W

Electrical Characteristics

V_S = (V+) – (V-) = 1.8 V to 5.5 V (± 0.9 V to ± 2.75 V), T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{CM} = V_{OUT} = V_S/2 (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.4	±2	mV
		V_S = 5 V, T_A = -40°C to 125°C			±2.5	
dV_{OS}/dT	V_{OS} vs temperature	T_A = -40°C to 125°C		±0.6		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 to 5.5 V, V_{CM} = (V-)	80	105		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V-)-0.1		(V+)+0.1	V
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V-) - 0.1 V < V_{CM} < (V+) - 1.4 V, T_A = –40°C to 125°C		86		dB
		V_S = 5.5 V, (V-) - 0.1 V < V_{CM} < (V+) - 1.4 V, T_A = -40°C to 125°C		95		
		V_S = 5.5 V, (V-) -0.1 V < V_{CM} < (V+) + 0.1 V, T_A = -40°C to 125°C		77		
		V_S = 1.8 V, (V-) - 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = -40°C to 125°C		68		
INPUT BIAS CURRENT						
I_B	Input bias current	V_S = 5 V		±5		pA
I_{OS}	Input offset current			±2		pA
NOISE						
E_n	Input voltage noise (peak to peak)	f = 0.1 Hz to 10 Hz, V_S = 5 V		4.7		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz, V_S = 5 V		30		nV/√Hz
		f = 10 kHz, V_S = 5 V		27		
i_n	Input current noise density (2)	f = 1 kHz, V_S = 5 V		23		fA/√Hz
INPUT CAPACITANCE(2)						
C_{ID}	Differential			1.5		pF
C_{IC}	Common-mode			5		pF

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OPEN-LOOP GAIN						
A_{VO}	Open-loop voltage gain	V_S = 5.5 V, R_L = 10 kΩ (V-) + 0.05 V < V_O < (V+) - 0.05 V	104	117		dB
		V_S = 1.8 V, R_L = 10 kΩ (V-) + 0.04 V < V_O < (V+) - 0.04 V		100		
		V_S = 1.8 V, R_L = 2 kΩ (V-) + 0.1 V < V_O < (V+) - 0.1 V		115		
		V_S = 5.5 V, R_L = 2 kΩ (V-) + 0.15 V < V_O < (V+) – 0.15 V		130		
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V_S = 5 V		1		MHz
φ_m	Phase margin	V_S = 5 V, G = 1		78		°
SR	Slew rate	V_S = 5 V		2		V/µs
t_S	Settling time(2)	To 0.1%, V_S = 5 V, 2V step, G = +1, C_L = 100 pF		2.5		µs
		To 0.01%, V_S = 5 V, 2V step, G = +1, C_L = 100 pF		3		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.85		µs
THD+N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz,		0.004		%
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ		10	20	mV
		V_S = 5.5 V, R_L = 2 kΩ		35	55	
I_{SC}	Short-circuit current	V_S = 5.5 V		±40		mA
Z_O	Open-loop output impedance(2)	V_S = 5 V, f = 1 MHz		1200		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5 V		60	85	µA
		I_O = 0 mA, V_S = 5.5 V, T_A = -40°C to 125°C			90	

Note2:Guaranteed by design.

Application Notes

Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

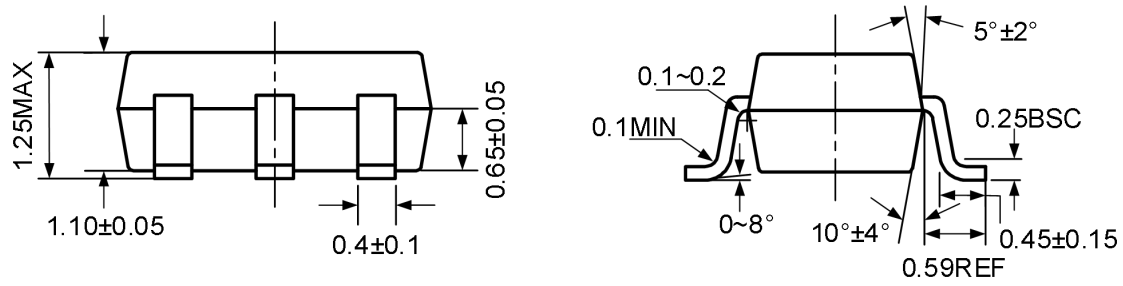
Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.

To reduce parasitic coupling, run the input traces as far away from the supply lines and digital signal as possible.Low-ESR, 0.1 μF ceramic bypass capacitors must be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single supply applications.

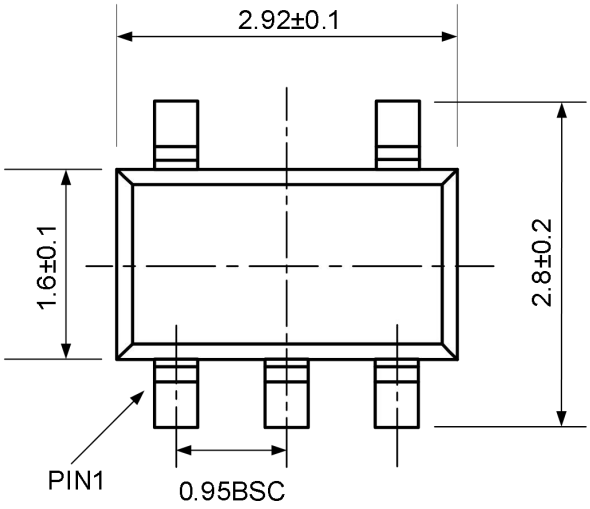
Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

Package Dimension

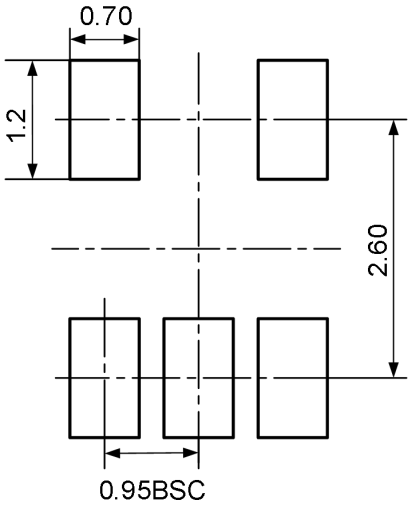
SOT23-5



SIDE VIEW



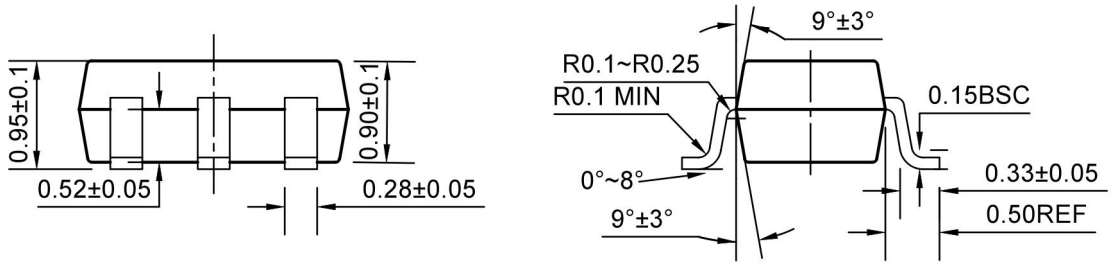
TOP VIEW



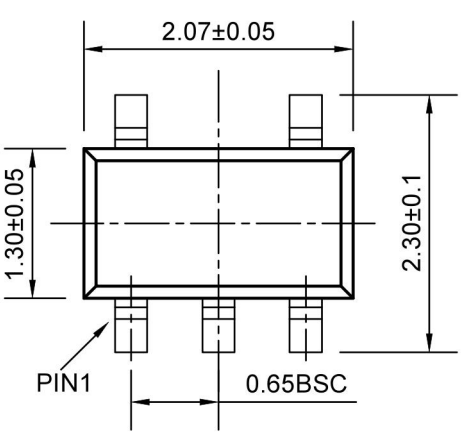
Recommended Land Pattern

Unit: mm

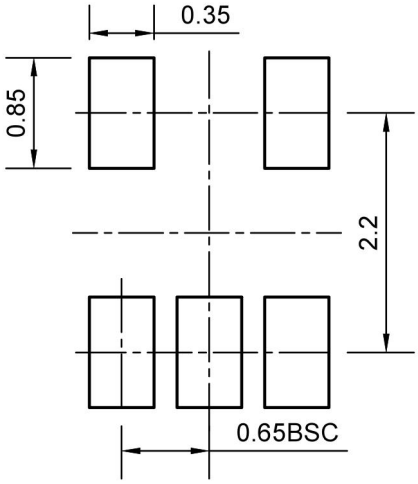
SC70-5



SIDE VIEW



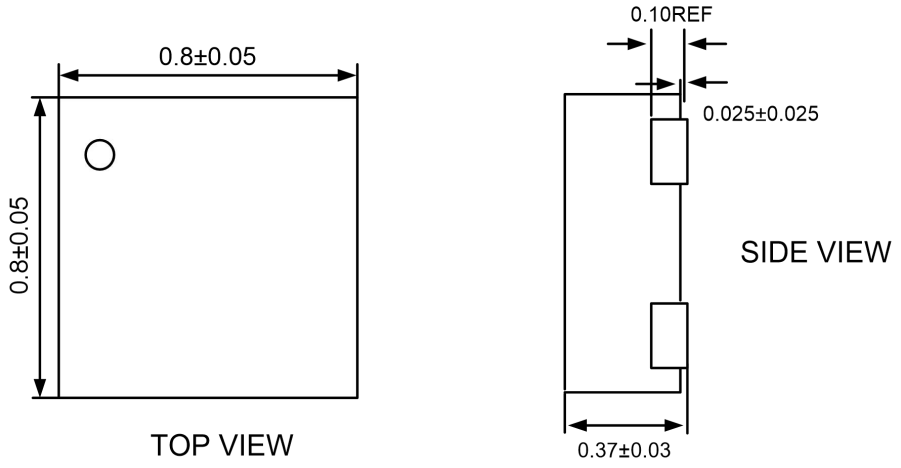
TOP VIEW

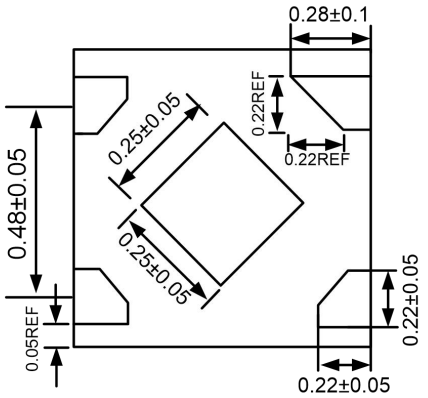


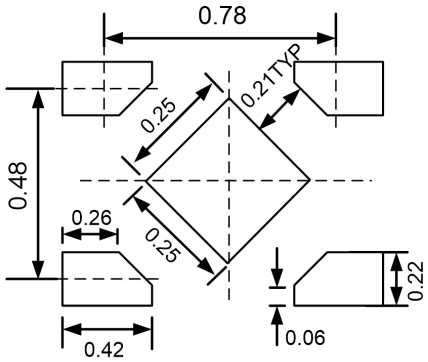
Recommended Land Pattern

Unit: mm

DFN4-0.8×0.8



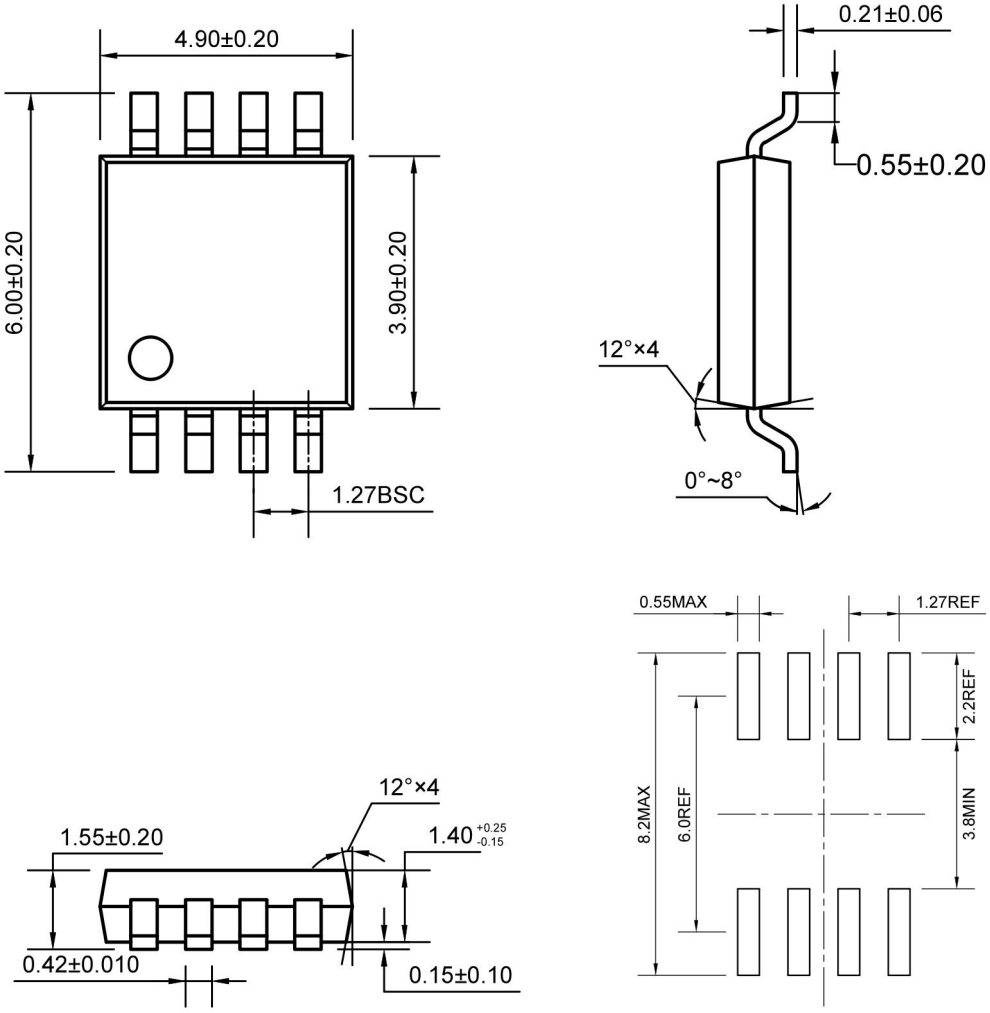




Recommended Land Pattern

Unit: mm

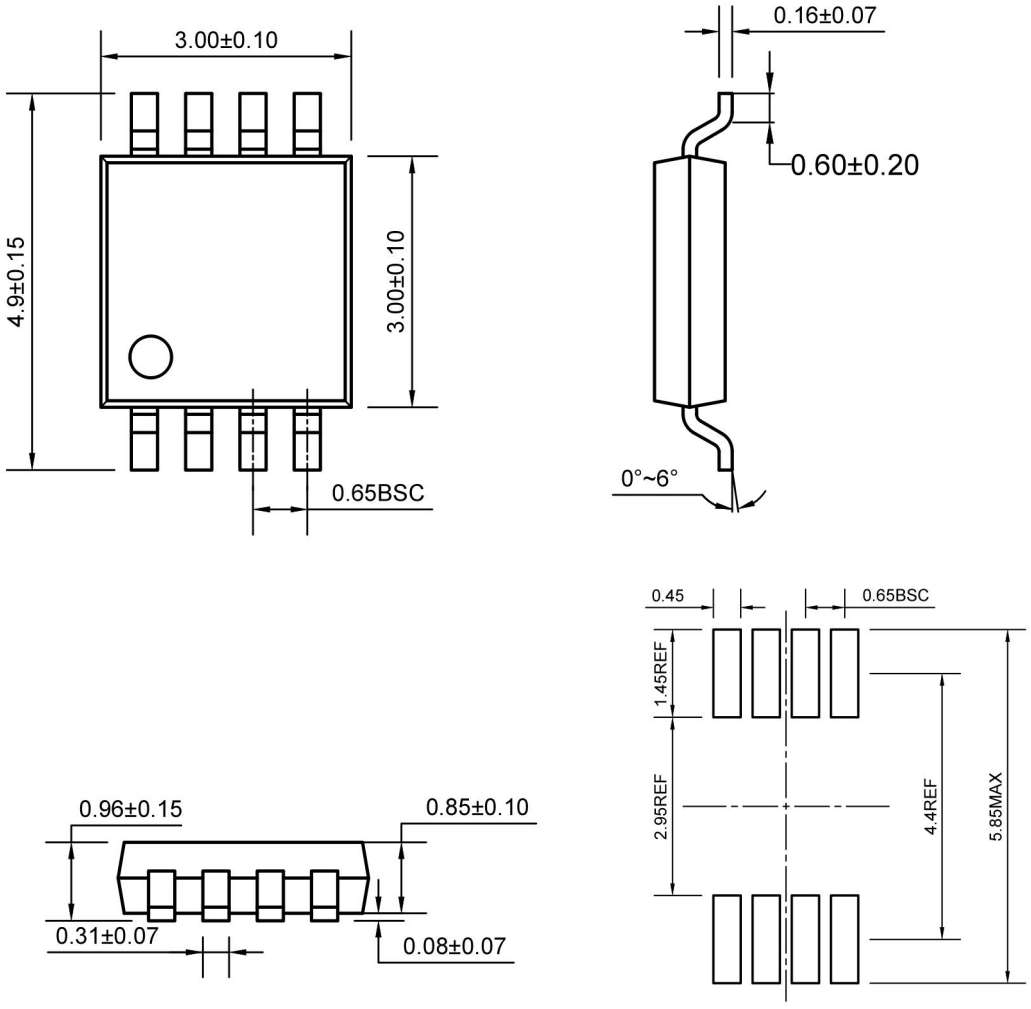
SOP8



Recommended Land Pattern

Unit: mm

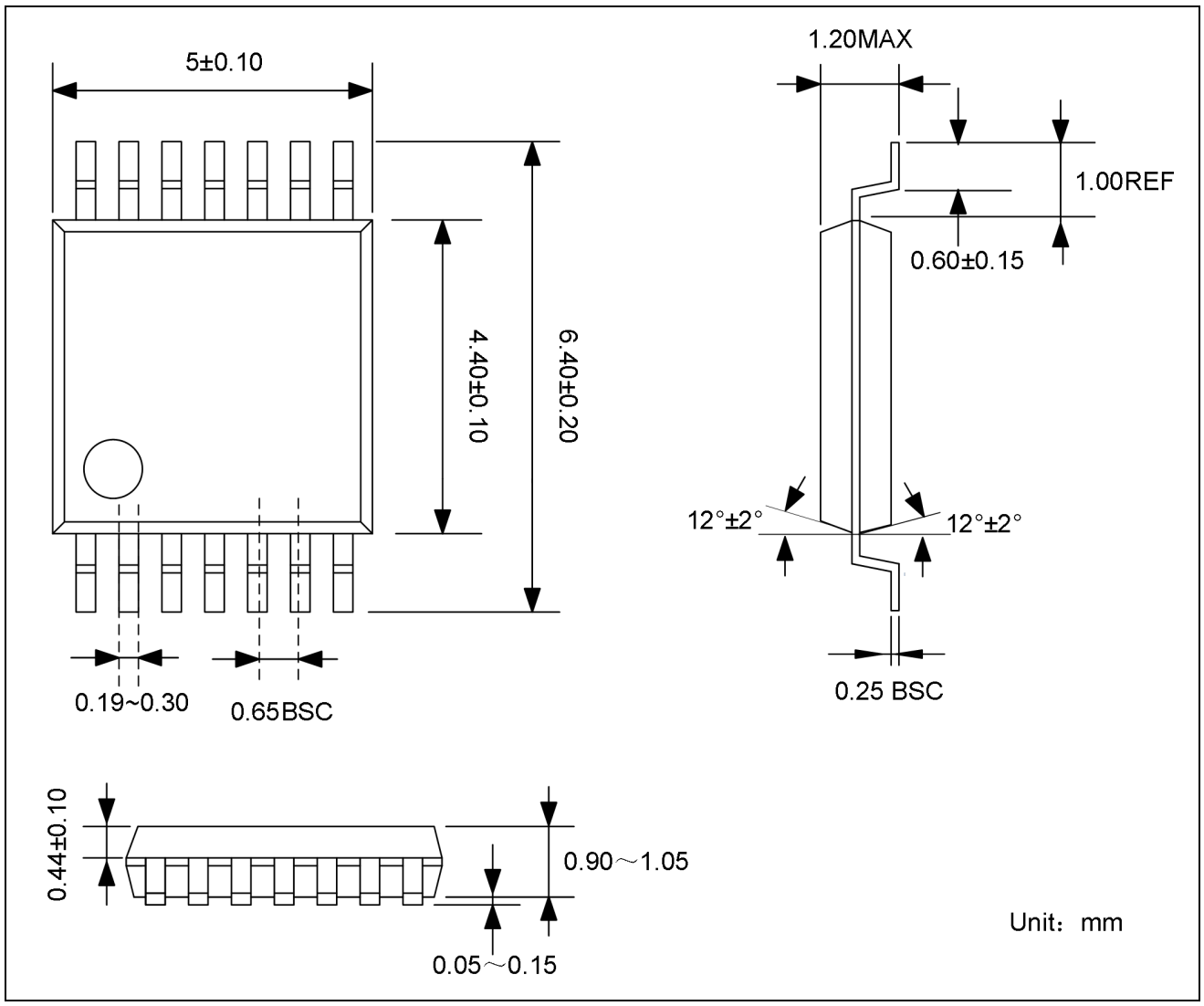
MSOP8



Recommended Land Pattern

Unit: mm

TSSOP14


5±0.10
4.40±0.10
6.40±0.20
0.19~0.30
0.65BSC
1.20MAX
1.00REF
0.60±0.15
12°±2°
12°±2°
0.25 BSC
0.44±0.10
0.90～1.05
0.05～0.15
Unit：mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2022-9-21	Preliminary Version	Shibo	Wanggp	Liujy
1.0	2023-4-6	Original Version	Huyt	Chenh	Liujy
1.1	2023-9-28	Naming updates	Huyt	Wanggp	Liujy
1.2	2024-4-8	Add TSSOP14 Package	Huyt	Wanggp	Liujy
1.3	2024-11-27	IQ max changed 82uA	Shibo	Wanggp	Liujy
1.4	2025-3-27	Update VOS max and IQ max	Huyt	Chenh,Tangyx	Liujy
1.5	2025-4-11	Update MSL Grade	Huyt	Chenh,Tangyx	Liujy
1.6	2025-6-25	Update format	Huyt	Wanggp	Liujy