# 400mA Ultra-Low Noise, High PSRR LDO for RF and Analog Circuits

## General Description

The ET538XXZB of low-dropout (LDO), low-power linear regulators offer up to 400mA with PMOS pass transistor. The device offers low noise, high PSRR, low quiescent current and very good line/load transients, suitable for RF applications and analog circuits.

The ET538XXZB is stable with a 1μF input and 1μF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve accuracy of 1.5%.

It is in a small WLCSP4(0.635mm×0.635mm) package, which is ideal for small form factor portable equipment such as wireless handsets and PDAs.

## Features

- Wide Input Voltage Range from 2.2V~5.5V
- Output Voltage Range from 1.2V to 4.3V
- Output Voltage Accuracy are ±1.5%
- Output Current are up to 400mA
- Very Low IQ of 20μA Typical
- Shutdown Current of 0.1uA Typical
- Low Dropout are Typical 180mV at 400mA, 2.8V Output
- Ultra Low Noise are Typical 8$\mu V_{RMS}$ (Load=200mA)
- Very High PSRR are 100dB at 1KHz, 45dB at 1MHz,30mA
- Excellent Line/Load Transient Response
- Built-in $I_{LIMIT}$ Protection and Thermal Shutdown Circuit
- Built-in Auto Discharge Function
- Package Information:

| Part No. | Package | MSL |
|---|---|---|
| ET538XXZB | WLCSP4(0.635mm×0.635mm) | Level 1 |

## Applications

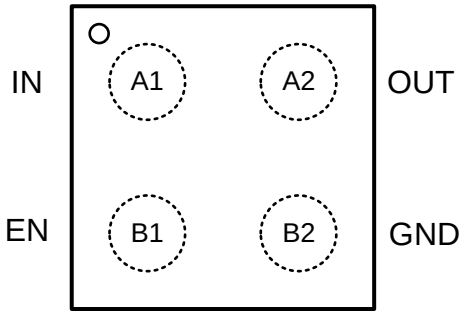
- Smart Phones and Cellular Phones
- PDAs
- MP3/MP4 Player
- Digital Still Cameras
- Portable instrument

## Device information

**ET 538 XX Z B**

| XX Output Voltage | | Z Package | | B Auto-discharge Function | |
|---|---|---|---|---|---|
| XX | Fixed Output Voltage | Z | CSP4 -0.635×0.635 | B | Available |

## Pin Configuration

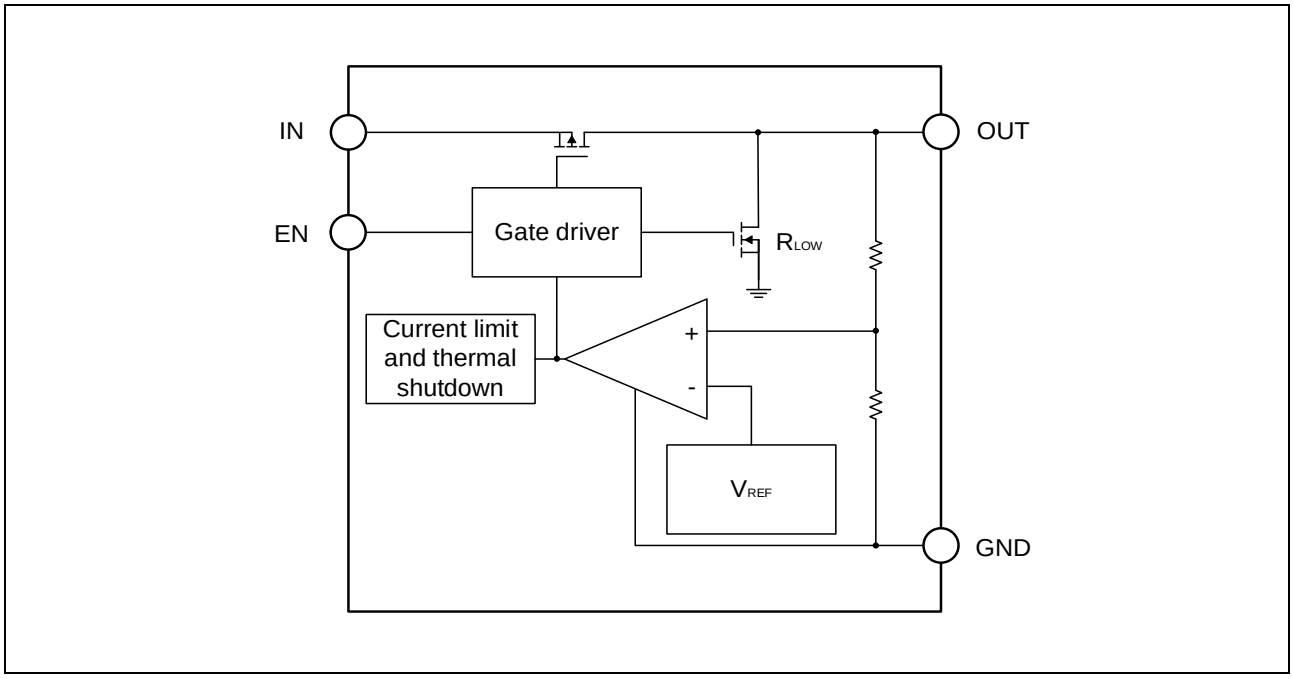



Top View

## Pin Function

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| A1 | IN | Supply input pin. Must be closely decoupled to GND with a 1μF ceramic capacitor. |
| A2 | OUT | Output pin. A 1μF low-ESR capacitor should be connected to this pin to ground. |
| B1 | EN | Enable control input, active high. Do not leave EN floating. |
| B2 | GND | Ground. |

## Block Diagram




## Functional Description

### Input Capacitor

A 1μF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance.

### Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1μF to 10μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins. With a reasonable PCB layout, the single 1μF ceramic output capacitor can be placed up to 10cm away from the ET538XXZB device.

### Remote Output Capacitor Placement

The ET538XXZB requires at least a 1μF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10cm away from the LDO.

### ON/OFF Input Operation

The ET538XXZB is turned on by setting the EN pin higher than $V_{IH}$ threshold, and is turned off by pulling it lower than $V_{IL}$ threshold. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time.

### Low Quiescent Current

The ET538XXZB, consuming only 20μA quiescent current, provides great power saving in portable and low power applications.

### High PSRR and Low Noise

The ET538XXZB, with PSRR of 100dB at 1KHz, 30mA is suitable for most of these applications that require high PSRR and low noise.

### Fast Transient Response

The ET538XXZB's fast transient response from 0 to 400mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

### Dropout Voltage

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage. The ET538XXZB internal circuitry is not fully functional until $V_{IN}$ is at least 2.2V. The output voltage is not regulated until $V_{IN}$ has reached at least the greater of 2.2V or ($V_{OUT}$ + $V_{DROP}$).

### Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuiting to GND, the current limit protection will be triggered and clamp the output current to approximately 650mA to prevent over-current and to protect the regulator from damage due to overheating.

### Output Automatic Discharge

The ET538XXZB output employs an internal 350Ω (Typical) pull-down resistance to discharge the output when the EN pin is low, and the device is disabled.

### Thermal Overload Protection

Thermal shutdown disables the output when the junction temperature rises to approximately 150°C which allows the device to cool. When the junction temperature cools to approximately 120°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the ET538XXZB has been designed to protect against temporary thermal overload conditions. The TSD circuitry was not intended to replace proper heat-sinking. Continuously running the ET538XXZB device into thermal shutdown may degrade device reliability

## Absolute Maximum Ratings

| Symbol | Parameters (Items) | Value | Unit |
|---|---|---|---|
| $V_{IN}$ | Input Voltage (IN Pin) | -0.3 to 6.0 | V |
| $V_{EN}$ | Input Voltage (EN Pin) | -0.3 to 6.0 | V |
| $V_{OUT}$ | Output Voltage (OUT Pin) | -0.3 to $V_{IN}$+0.3 | V |
| $P_{D\_MAX}$ (1) | Maximum Power Consumption | 700 | mW |
| $I_{MAX}$ | Maximum Load Current | 400 | mA |
| $T_J$ | Operating Junction Temperature | -40 to 150 | °C |
| $T_{STG}$ | Storage Temperature | -65 to 150 | °C |
| $T_{SLOD}$ | Lead Temperature (Soldering, 10 sec) | 260 | °C |
| $V_{ESD}$ | HBM (ESDA/JEDEC JS-001-2017) | ±4000 | V |
| | CDM (ESDA/JEDEC JS-002-2014) | ±1500 | V |
| $I_{LU}$ | Latch up Current Maximum Rating (JESD78E) | ±200 | mA |

***Note (1)***: Rating at mounting on a board (PCB board dimension: 40mm x 40mm (4layer), copper: 1OZ).

## Recommended Operating Conditions

| Symbol | Parameters | Rating | Unit |
|---|---|---|---|
| $V_{IN}$ (2) | Input Voltage | 2.2 to 5.5 | V |
| $V_{OUT}$ | Output Voltage | 1.2 to 4.3 | V |
| $I_{OUT}$ | Output Current | 0 to 400 | mA |
| $T_A$ | Operating Ambient Temperature | -40 to 85 | ºC |
| $C_{IN}$ | Effective Input Ceramic Capacitor Value | 0.68 to 10 | μF |
| $C_{OUT}$ | Effective Output Ceramic Capacitor Value | 0.68 to 10 | μF |
| ESR | Input and Output Capacitor Equivalent Series Resistance (ESR) | 5 to 100 | mΩ |

***Note (2)***: In order to achieve high performance of PSRR, it is recommended that the $V_{IN}$ needs to be no smaller than ($V_{OUT}$+0.5V).

## Electrical Characteristics

($V_{IN}$ =$V_{OUT}$ +1V, $V_{EN}$ = 1.2V, $C_{IN}$ =1μF, $C_{OUT}$ =1μF. Typical values are at $T_A$=25°C, unless otherwise stated)

| Symbol | Parameters | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ (3) | Input Voltage Range | | 2.2 | | 5.5 | V |
| $V_{UVLO}$ | Under Voltage Lockout | $V_{IN}$ Rising | | 2.0 | | V |
| | | $V_{IN}$ Falling | | 1.9 | | V |
| $V_{DROP}$ (4) | Dropout Voltage | $V_{OUT}$ = 1.8V, $I_{OUT}$ = 400mA | | | 400 | mV |
| | | $V_{OUT}$ = 2.2V, $I_{OUT}$ = 400mA | | 200 | 280 | mV |
| | | $V_{OUT}$ = 2.8V, $I_{OUT}$ = 400mA | | 180 | 260 | mV |
| $I_{Q\_ON}$ | Input Quiescent Current | $I_{OUT}$= 0mA | | 20 | 40 | uA |
| $I_{Q\_OFF}$ | Input Shutdown Quiescent Current | $V_{EN}$=0V | | 0.1 | 1 | uA |
| $V_{OUT}$ | Output Voltage Accuracy | $V_{IN}$ = $V_{OUT(NOM)}$ + 1V, $I_{OUT}$ = 1mA, $T_A$ = -40°C < $T_A$ < 85°C | -1.5 | | 1.5 | % |
| $Reg_{LINE}$ | Line Regulation | $V_{IN}$ = $V_{OUT}$ + 1V to 5.5V, $I_{OUT}$ =1mA | | 0.01 | 0.1 | %/V |
| $Reg_{LOAD}$ | Load Regulation | $I_{OUT}$ = 1mA to 400mA | | 20 | 40 | mV |
| $I_{OUT}$ | Output Current | | 400 | | | mA |
| $I_{LIMIT}$ | Current Limit | $T_A$ = 25°C | 450 | 650 | | mA |
| PSRR (5) | Power Supply Rejection Ratio | f =100 Hz, $I_{OUT}$ = 30mA | | 90 | | dB |
| | | f =1 kHz, $I_{OUT}$ = 30mA | | 100 | | dB |
| | | f =100 kHz, $I_{OUT}$ = 30mA | | 65 | | dB |
| | | f =1 MHz, $I_{OUT}$ = 30mA | | 45 | | dB |
| $e_N$ (5) | Output Noise Voltage | BW =10 Hz to 100 kHz, $I_{OUT}$ = 10mA | | 9 | | $\mu V_{RMS}$ |
| | | BW =10 Hz to 100 kHz, $I_{OUT}$ = 200mA | | 8 | | $\mu V_{RMS}$ |
| $V_{IH}$ | EN Low Threshold | $V_{IN}$ = 2.2 to 5.5V | 0.84 | | | V |
| $V_{IL}$ | EN High Threshold | $V_{IN}$ = 2.2 to 5.5V | | | 0.40 | V |
| $I_{EN}$ | EN Input current | $V_{EN}$ = 0 to 5.5V | | 0.5 | 1 | uA |
| $V_{TRLN}$ (5) | Line Transient | $V_{IN}$ = ($V_{OUT}$+1V) to ($V_{OUT}$+2V) in 10us | | 5 | 20 | mV |
| | | $V_{IN}$ = ($V_{OUT}$+2V) to ($V_{OUT}$+1V) in 10us | | 5 | 20 | mV |
| $V_{TRLD}$ (5) | Load Transient | $I_{OUT}$ = 1mA to 400mA in 10us | | 25 | 60 | mV |
| | | $I_{OUT}$ = 400mA to 1mA in 10us | | 20 | 45 | mV |
| $R_{LOW}$ | Output Discharge FET Rdson | $V_{EN}$=0v, $V_{IN}$=5V, $I_{OUT}$=10mA | 200 | 350 | 500 | Ω |
| $t_{ON}$ | Output Turn-on Time | From $V_{EN}$ > $V_{ENH}$ to $V_{OUT}$ = 95% of $V_{OUT(NOM)}$ | | 500 | | us |
| $T_{TSD}$ (5) | Thermal Shutdown Threshold | $T_J$ Rising | | 150 | | °C |
| $T_{HYS}$ (5) | Thermal Shutdown Hysteresis | $T_J$ Falling from Shutdown | | 30 | | °C |

***Note(3)***:The maximum input voltage should take into account the maximum power consumption ($P_{D\_MAX}$).The calculation formula is as follows:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT}$$

The maximum power consumption of the circuit is 700mW.

$$V_{IN(MAX)} = 700mW / I_{OUT} + V_{OUT}$$

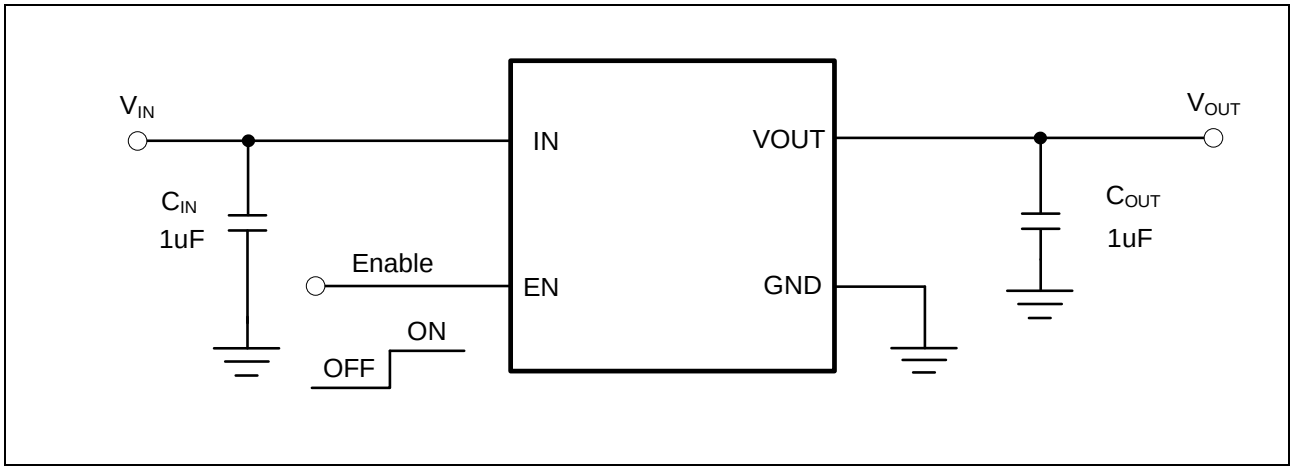
For example:

If $V_{OUT}$= 1.2V, $I_{OUT}$=400mA, the maximum input voltage is $V_{IN(MAX)}$=700mW / 400mA+1.2=2.95V

***Note(4):*** $V_{DROP}$ FT test method: test the $V_{OUT}$ voltage at $V_{SET}$ +$V_{DROPMAX}$ with output current.

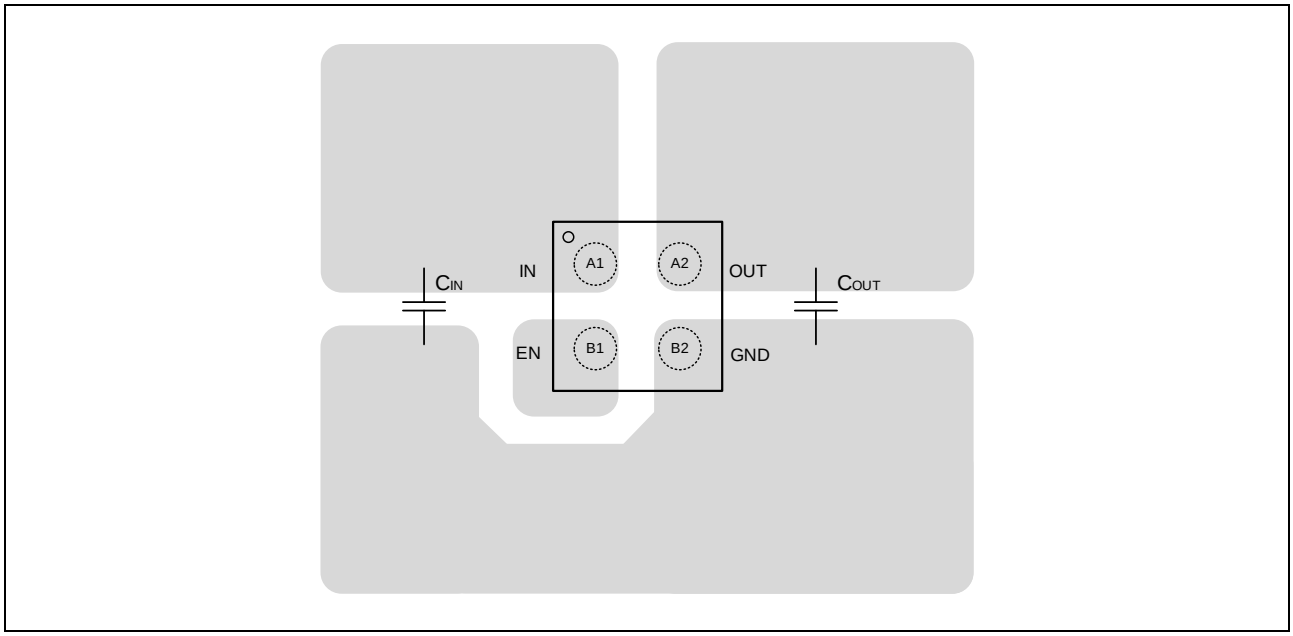
***Note(5):*** Guaranteed by design and characterization. Not a FT item.

## Application Circuits




## PCB Layout Guide

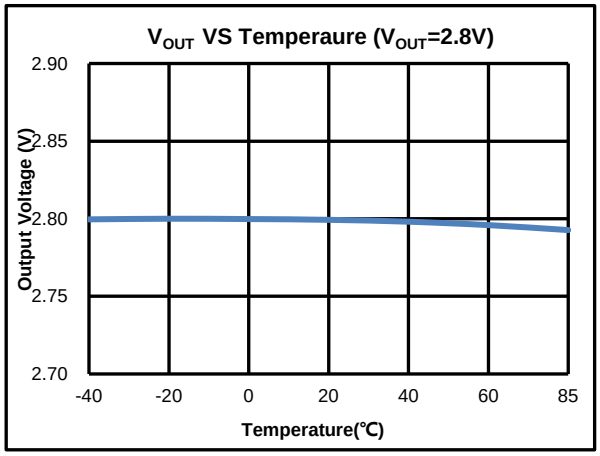
WLCSP4(0.635mm×0.635mm)



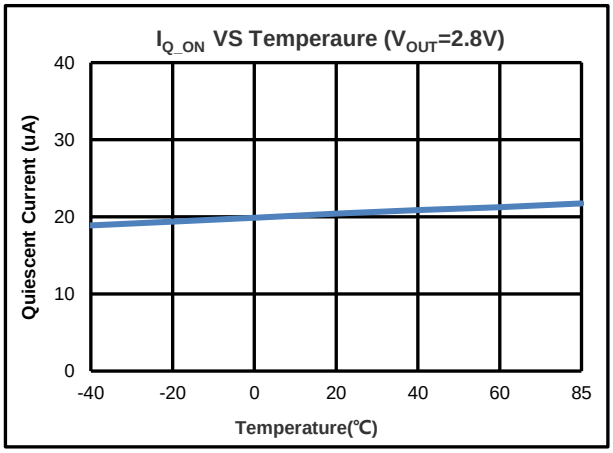
## Typical Characteristics

### VOLTAGE VERSION 2.8 V

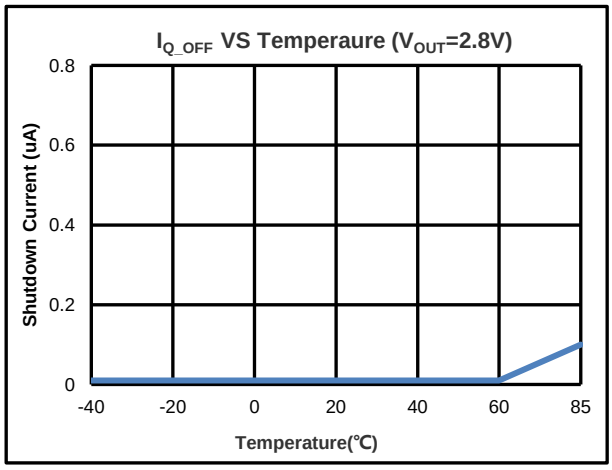
($V_{IN}$=3.8V; $C_{IN}$=$C_{OUT}$ =1.0μF, unless otherwise noted. Typical values are at $T_A$=25°C.)



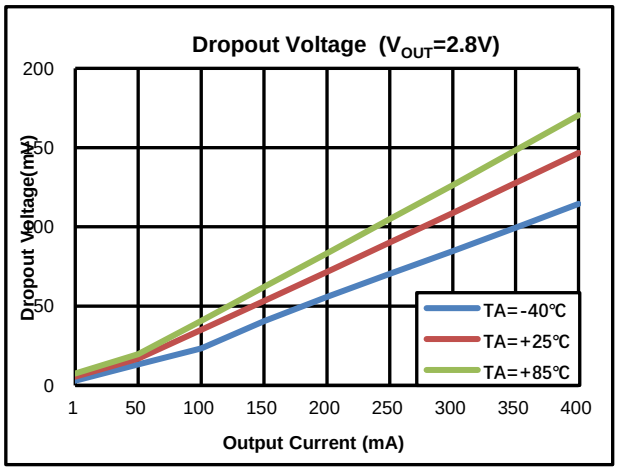

Output Voltage VS Temperature



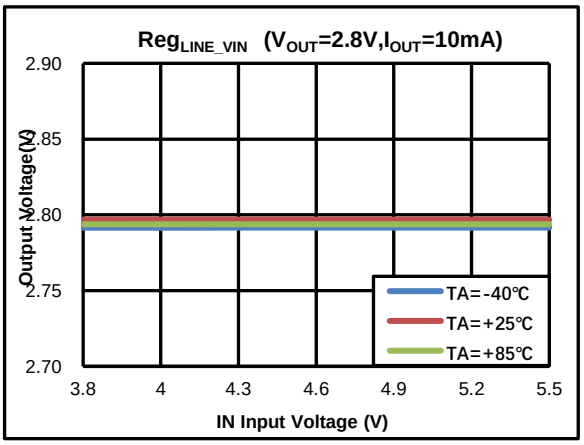

Quiescent Current VS Temperature



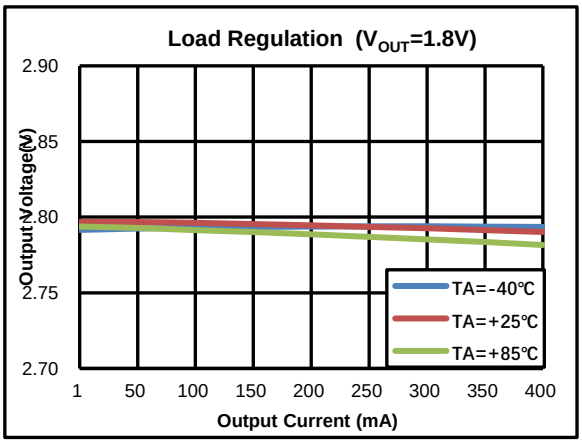

Standby Current VS Temperature




Dropout Voltage VS Output Current



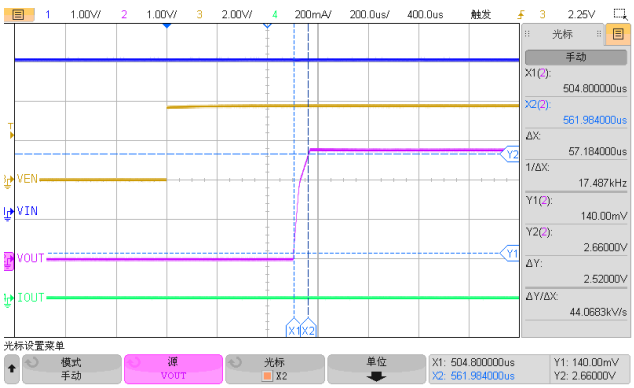

Output Voltage VS Input Voltage




Output Voltage VS Output Current

## Typical Characteristics (Continued)

($V_{IN}$=3.8V; $C_{IN}$=$C_{OUT}$ =1.0μF, unless otherwise noted. Typical values are at $T_A$=25°C.)

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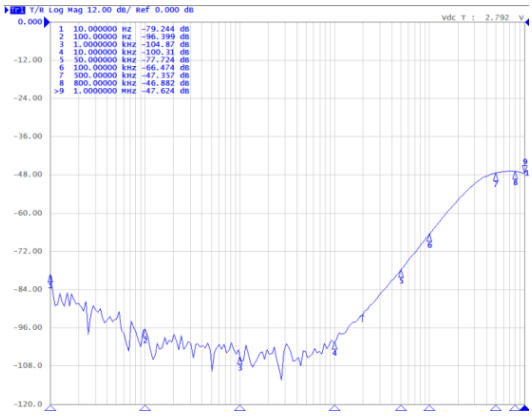
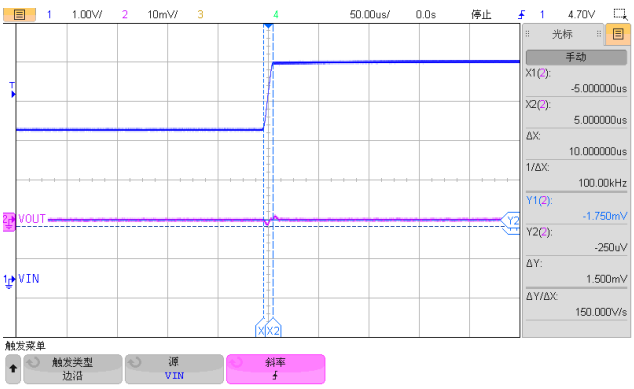
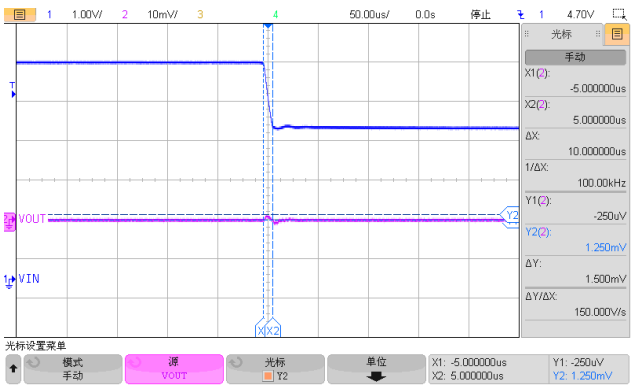


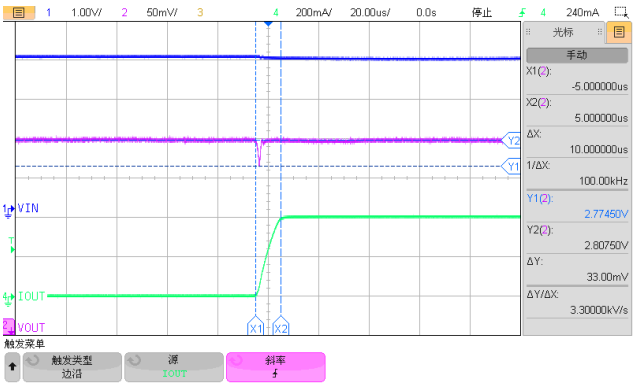
PSRR



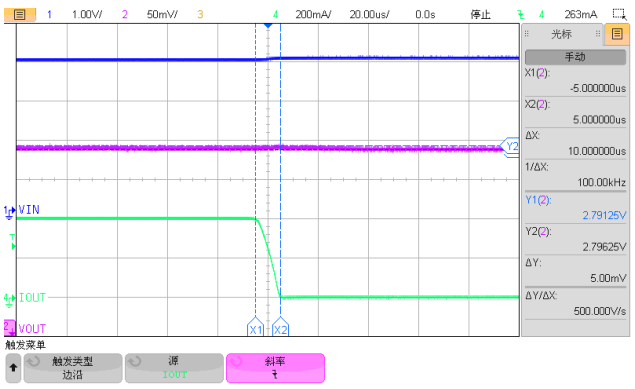

Input-Transient (3.8~5.5V tr=10μs $I_{OUT}$=1mA)




Input-Transient (5.5~3.8V tf=10μs, $I_{OUT}$=1mA)



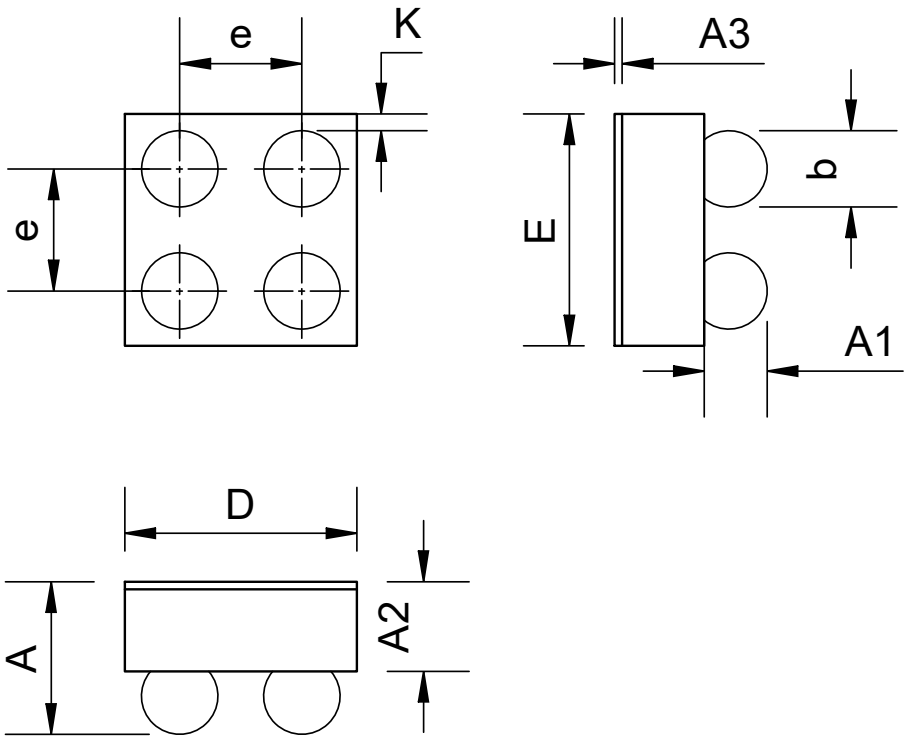

Load-Transient ($V_{IN}$ =3.8V, $I_{OUT}$=1~400mA tr=10μs)




Load-Transient ($V_{IN}$ =3.8V, $I_{OUT}$=400~1mA tf=10μs)

## Package Dimension

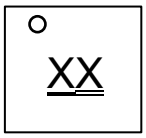
WLCSP4(0.635mm×0.635mm)




**Dimensions Table (Units: mm)**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.27 | 0.30 | 0.33 |
| A1 | 0.05 | 0.06 | 0.07 |
| A2 | 0.22 | 0.24 | 0.26 |
| A3 | 0.025REF | | |
| b | 0.17 | 0.19 | 0.21 |
| D | 0.61 | 0.635 | 0.66 |
| E | 0.61 | 0.635 | 0.66 |
| e | 0.35BSC | | |
| K | 0.05REF | | |

## Marking

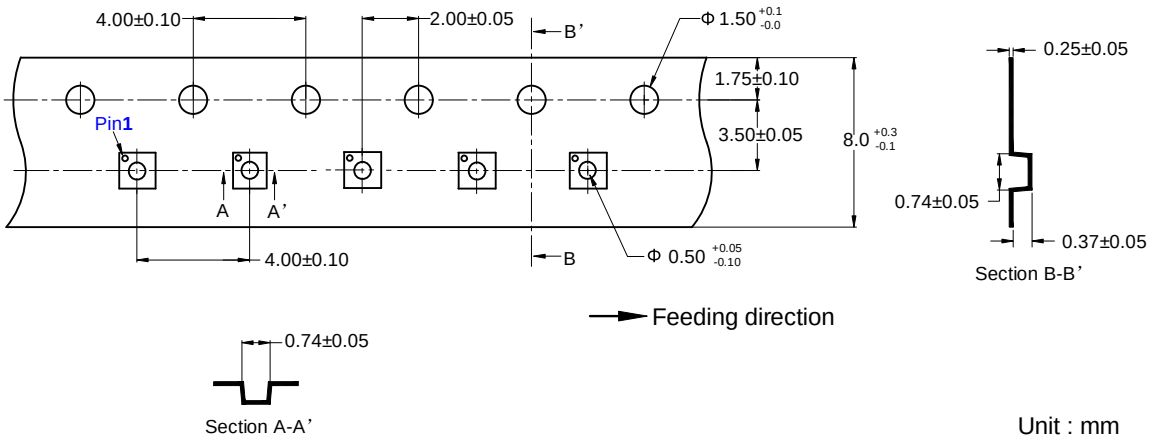



X = Part Number

X = $V_{OUT}$ Version

## Reel

WLCSP4(0.635mm×0.635mm)




## Revision History and Checking Table

| Version | Date | Revision Item | Modifier | Function & Spec Checking | Package & Tape Checking |
|---|---|---|---|---|---|
| 0.0 | 2024-01-02 | Preliminary Version | Li Huan | Liu Yi Guo | Liu Jia Ying |
| 1.0 | 2025-02-25 | Official Version | Wang An Ran | Yang Xiao Xu | Liu Jia Ying |