Hex Schmidt-Trigger Inverters

General Description

The ET74HC14 is a hex inverter with Schmitt-trigger inputs. This device features reduced input threshold levels to allow interfacing to TTL logic levels. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}. Schmitt trigger inputs transform slowly changing input signals into sharply defined jitter-free output signals.

Features

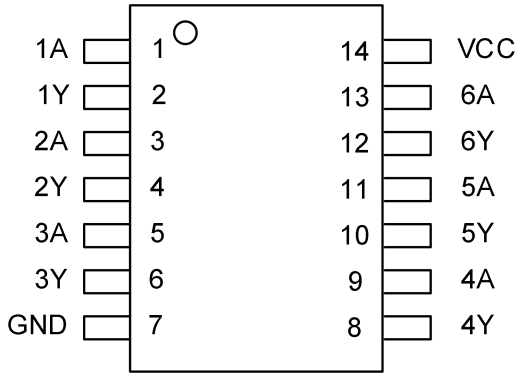
- Wide Operating Voltage Range of 2V to 6V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption I_{CC} = 20μA Max
- ±5.2mA Balanced Output Sink and Source Capability
- Low Input Current of 1μA MAX
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±4000V Pass (JEDEC JS-001)
  -- CDM: ±1000V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±100mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74HC14M	SOP14 (8.65mm × 3.90mm)	Tape and Reel, 4K/Reel	3
ET74HC14V	TSSOP14 (4.96mm × 4.40mm)	Tape and Reel, 4K/Reel	3
ET74HC14P	DIP14 (19.10mm × 6.35mm)	Tape and Reel, 4K/Reel	3

Applications

- Memory chip select decoding
- Data transmission system

Pin Configuration



SOP14/TSSOP14/DIP14

Figure1. Pin Configuration

Pin Function

No.	Name	Function
1	1A	Channel 1 Input.
2	1Y	Channel 1 Output.
3	2A	Channel 2 Input.
4	2Y	Channel 2 Output.
5	3A	Channel 3 Input.
6	3Y	Channel 3 Output.
7	GND	Ground.
8	4Y	Channel 4 Iutput.
9	4A	Channel 4 Input.
10	5Y	Channel 5 Output.
11	5A	Channel 5 Input.
12	6Y	Channel 6 Output.
13	6A	Channel 6 Input.
14	VCC	Positive Voltage Supply.

Block Diagram

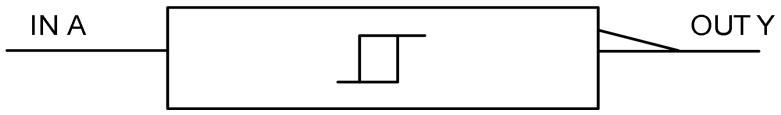


Figure2. Logic Symbol

Functional Table

Input A	Output Y
H	L
L	H

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 7.0	V
V_I	DC Input Voltage (1)		$-0.5 \le V_I \le 7.0$	V
I_{IK}	DC Input Diode Current, V_I < GND		±20	mA
I_{OK}	DC Output Diode Current, V_O < GND, V_O > V_{CC}		±20	mA
I_O	DC Output Sink Current		±25	mA
I_{CC}	DC Supply Current per Supply Pin		50	mA
I_{GND}	DC Supply Current GND Pin		-50	mA
T_{STG}	Storage Temperature Range		-65 to 150	°C
V_{ESD}	ESD Classification	Human Body Model (2)	±4000	V
		Charged Device Model (3)	±1000	
I_{LU}	Max Latch Up Current Above V_{CC} and GND at 125°C (4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended operating conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (VCC Pin)	2	6	V
V_I	Input Voltage	0	V_{CC}	V
V_O	Output Voltage (High or Low State)	0	V_{CC}	V
T_A	Operating Temperature Range	-40	125	°C

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2	1.5			1.5		V
			4.5	3.15			3.15		
			6	4.2			4.2		
V_{IL}	Low-Level Input Voltage		2			0.5		0.5	V
			4.5			1.35		1.35	
			6			1.8		1.8	
V_{OH}	High-Level Output Voltage	I_{OH} = -20μA	2	1.9	1.998		1.9		V
			4.5	4.4	4.499		4.4		
			6	5.9	5.999		5.9		
		I_{OH} = -4mA	4.5	3.98	4.3		3.84		
		I_{OH} = -5.2mA	6	5.48	5.8		5.34		
V_{OL}	Low-Level Output Voltage	I_{OL} = 20μA	2		0.002	0.1		0.1	V
			4.5		0.001	0.1		0.1	
			6		0.001	0.1		0.1	
		I_{OL} = 4mA	4.5		0.17	0.26		0.33	
		I_{OL} = 5.2mA	6		0.15	0.26		0.33	
I_I	Input Leakage Current	V_I = 6V or GND	6		±0.1	±100		±1000	nA
I_{CC}	Quiescent Supply Current	V_I = 6V or GND	6			2		20	μA

Switching Characteristics (C_L = 50pF)

Symbol	From (Input)	To (Output)	V_{CC}(V)	T_A = 25°C		-40°C ≤ T_A ≤ 125°C		Unit
				Typ	Max	Min	Max	
t_{pd}	A	Y	2	45	95		120	ns
			4.5	8	18		24	
			6	7	15		20	
t_r, t_f		Y	2	38	75		95	ns
			4.5	8	15		19	
			6	6	13		16	

Operating Characteristics

Symbol	Parameter	Test Conditions	Typ	Unit
C_I	Input Capacitance	V_{CC} = 6V, V_I = 0V or V_{CC}	3	pF
C_{PD}	Power Dissipation Capacitance (5)	No Load	20	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

AC Test Circuit

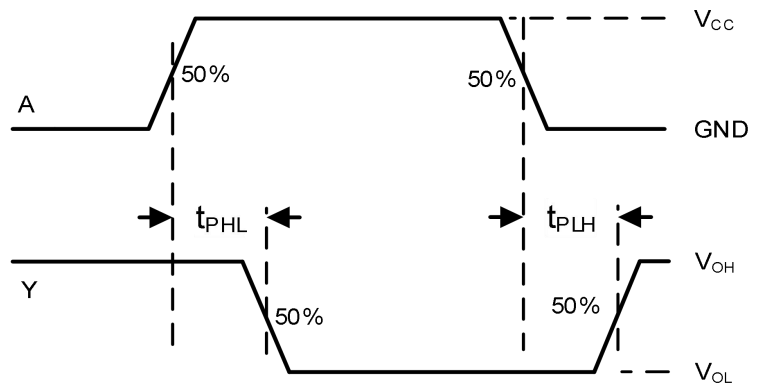


Figure3. Switching Waveform

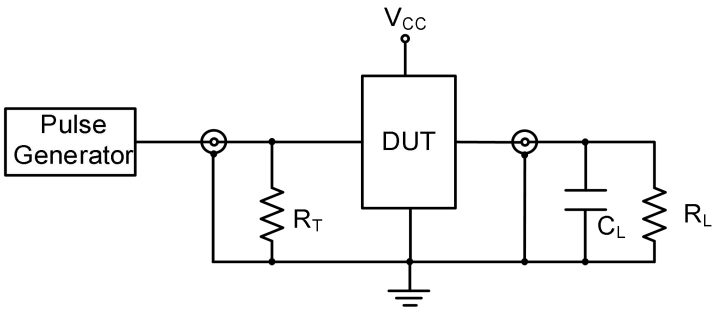
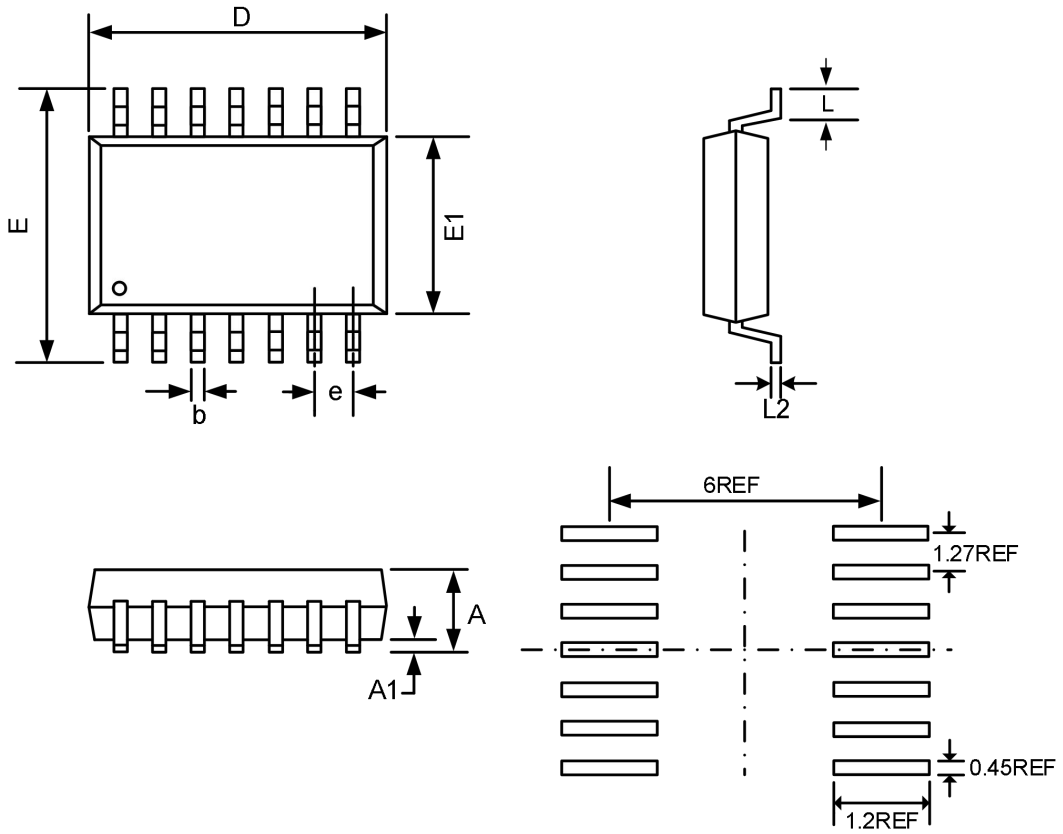


Figure4. Test Circuit

Package Dimension

SOP14 (3.9mm × 8.65mm)

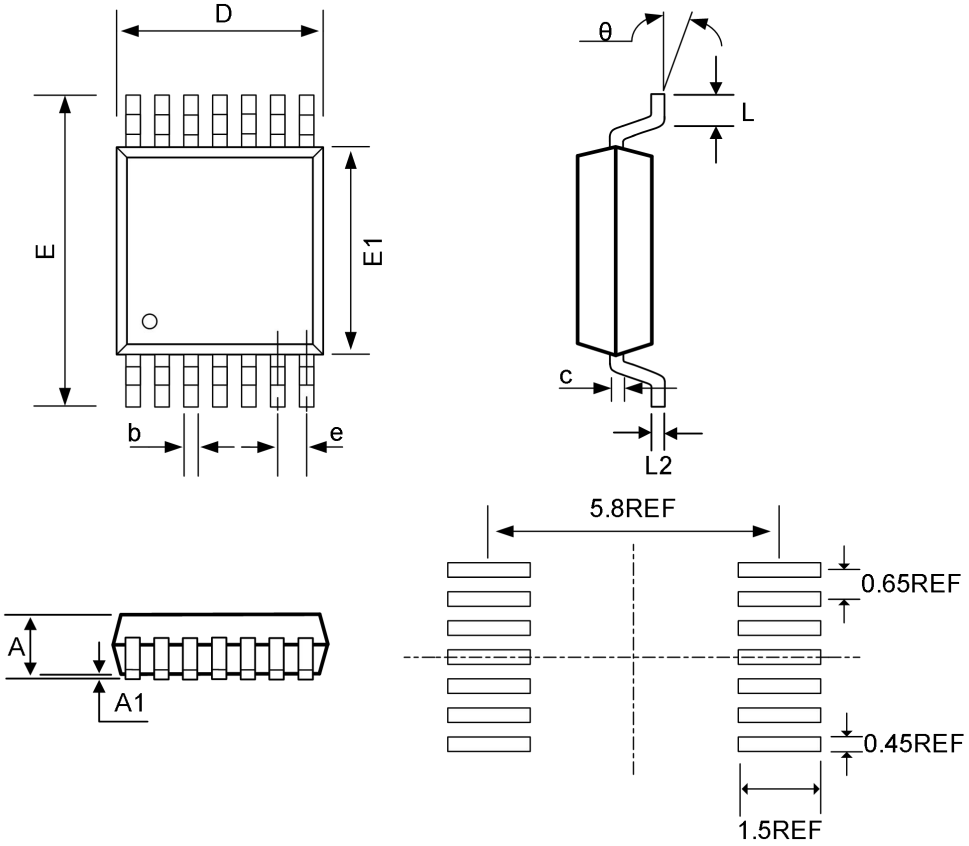


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	MAX
A	--	1.75
A1	0.10	0.25
b	0.36	0.51
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.22	1.32
L	0.45	0.75
L2	0.25 BSC	

TSSOP14 (4.4mm × 5.0mm)

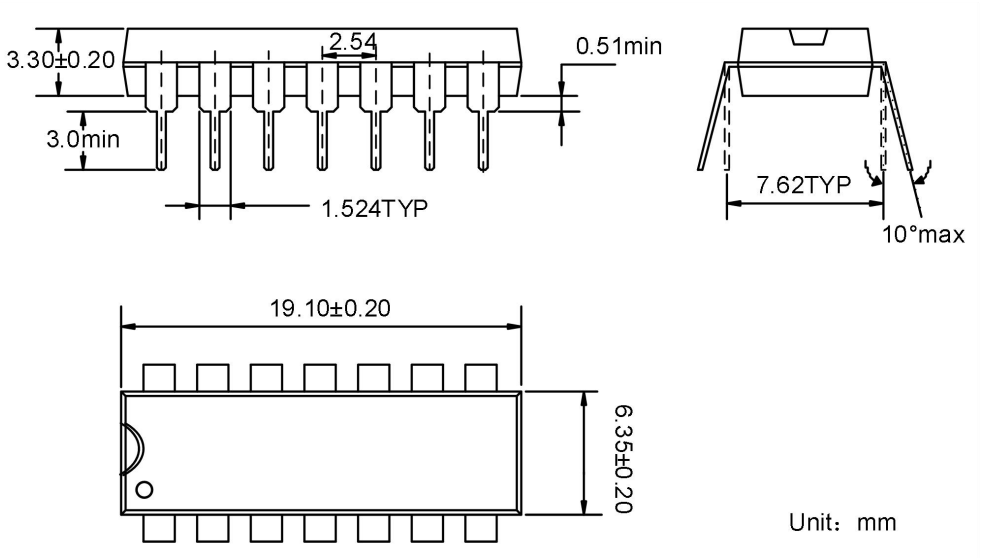


COMMON DIMENSIONS

(Unit: mm)

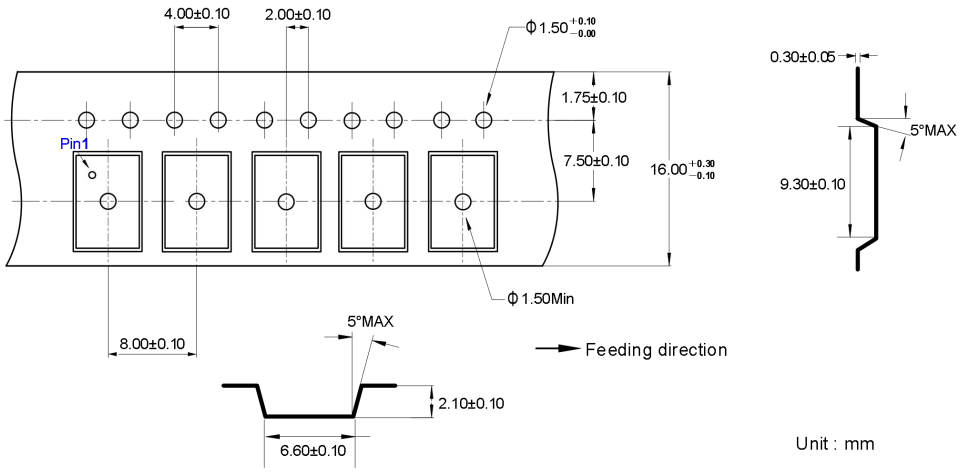
SYMBOL	MIN	MAX
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 REF	
D	4.86	5.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L2	0.25 REF	
θ	0°	8°

DIP14 (19.10mm × 6.35mm)

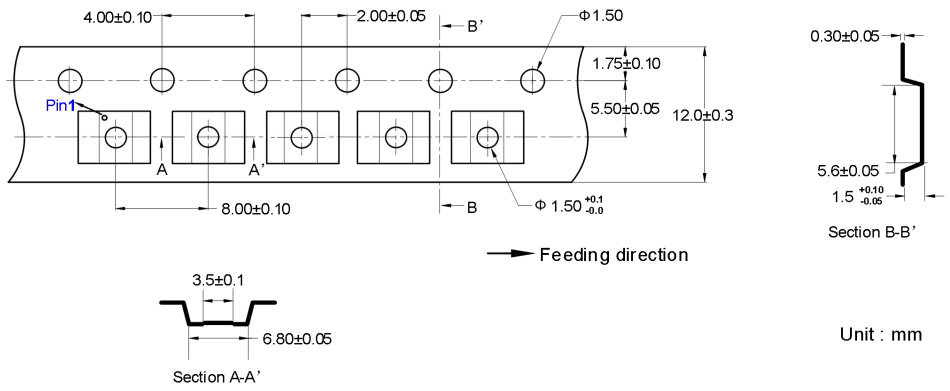


Tape Information

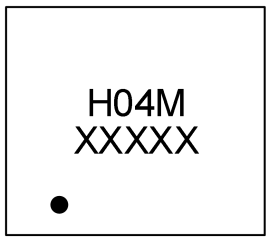
SOP14 (3.9mm × 8.65mm)



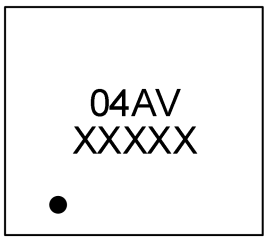
TSSOP14 (4.4mm × 5.0mm)



Marking Information



ET74HC14M
H04M= Part Number
XXXXX = Tracking Number



ET74HC14V
04AV = Part Number
XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-3-30	Official Version	Wang anran	Yang xiaoxu	Liu jiaying
1.1	2026-9-12	Update Marking	Wang anran	Yang xiaoxu	Liu jiaying