I²C Controlled 3.0A Single Cell Battery Charger for High Input Voltage and NVDC Power Path Management

General Description

The ET95611CX device is a highly-integrated 3.0A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I²C serial interface with charging and system settings makes the device a truly flexible solutions.

Features

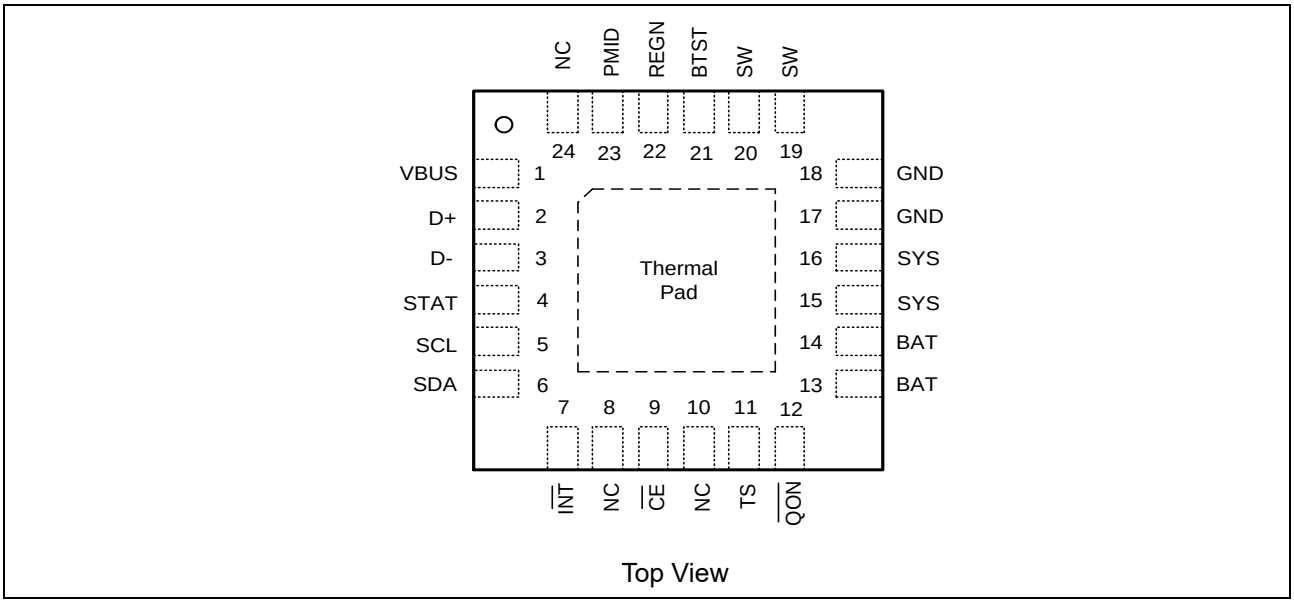
- High-Efficiency, 1.1MHz, Synchronous Switch Mode Buck Charger
  - 92% Charge Efficiency at 2 A from 5V Input
  - 90% Charge Efficiency at 2 A from 9V Input
  - Selectable Low Power Pulse Frequency Modulation (PFM) Mode for Light Load Operations
- Supports USB On-The-Go (OTG)
  - Boost Converter with Up to 1.8A Output
  - 94% Boost Efficiency at 1A Output
  - Accurate Constant Current (CC) Limit
  - Soft-Start Up to 500μF Capacitive Load
  - Output Short Circuit Protection
  - Selectable Low Power PFM Mode for Light Load Operations
- Single Input to Support USB Input and High Voltage Adapters
  - Support 3.9V to 13V Input Voltage Range With 18V Absolute Maximum Input Voltage Rating
  - Programmable Input Current Limit (100 mA to 3.0A With 20mA Resolution) to Support USB 2.0, USB 3.0 Standards and High Voltage Adaptors (IINDPM)
- High Battery Discharge Efficiency With 30mΩ Battery Discharge MOSFET
- Narrow VDC (NVDC) power path management
  - Instant-On Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- BATFET Control to Support Ship Mode, Wake Up
- Flexible Autonomous and I²C Mode for Optimal System Performance
- High Integration Includes All MOSFETs, Current Sensing and Loop Compensation
- 1μA Battery Leakage Current in ship mode
- Integrated 14bit ADC for Voltage, Current, Temperature Monitoring

- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±5% Charge Current Regulation
  - ±5% Input Current Regulation
- Package: QFN24(4mm×4mm)

Applications

- Tablet
- Gaming and Computer Accessories
- IP Camera, EPOS
- Portable Medical Equipment

Pin Configuration



Top View

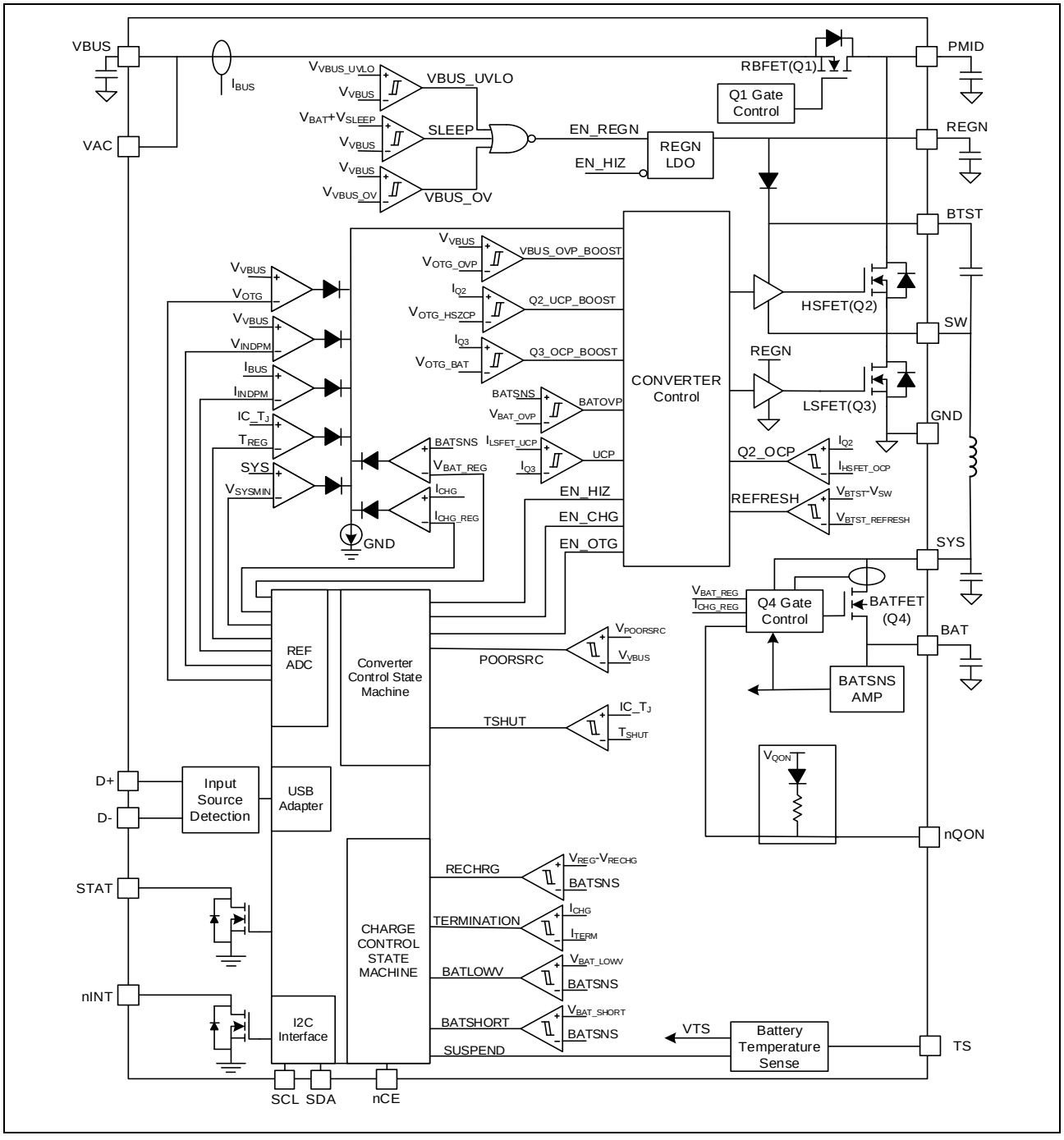
Pin Functions

Pin		TYPE	DESCRIPTION
NAME	NO.		
VBUS	1	AI	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1μF ceramic capacitor from VBUS to GND close to device.
D+	2	AIO	Positive Line of the USB Data Line Pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter
D-	3	AIO	Negative Line of the USB Data Line Pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter.
STAT	4	DO	Open Drain Charge Status Output. It indicates various charger operations. Connect to the pull up rail via 10kΩ resistor. LOW indicates charging in progress. HIGH indicates charging completed or charging disabled. When any fault condition occurs, STAT pin blinks at 1Hz. The STAT pin function can be disabled when DIS_STAT bit is set.
SCL	5	DI	I^2C Interface Clock. Connect SCL to the logic rail through a 10kΩ resistor.
SDA	6	DO	I^2C Interface Data. Connect SDA to the logic rail through a 10kΩ resistor.
INT	7	DO	Open Drain Interrupt Output. Connect to the pull up rail via 10kΩ resistor. The INT pin sends an active low, 256μs pulse to the host to report the charger device status and faults.
NC	8	DO	No Connect. Keep this pin float.
CE	9	DI	Active Low Charge Enable Pin. Battery charging is enabled when EN_CHG bit is 1 and CE pin is LOW. CE pin must be pulled HIGH or LOW, do not leave floating.
TS	11	AI	Temperature Qualification Voltage Input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor.
QON	12	DI	BATFET Enable or System Power Reset Control Input. If the charger is in ship mode, a logic low on this pin with t_{SM_EXIT} duration forces the device to exit ship mode. If the charger is not in ship mode, a logic low on this pin with t_{QON_RST} initiates a full system power reset if either $V_{VBUS} < V_{VBUS_UVLO}$ or BATFET_CTRL_WVBUS = 1. QON has no effect during shutdown mode. The pin contains an internal pull-up to maintain default high logic.
BAT	13	P	Battery connection point to the positive terminal of the battery pack.The internal BATFET is connected between BAT and SYS. Connect a 10μF closely to the BAT pin.
	14		

Pin Functions (Continued)

Pin		TYPE	DESCRIPTION
NAME	NO.		
SYS	15	P	The charger output voltage to system. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage. Connect a 20μF closely to the SYS pin.
	16		
GND	17	P	Ground Return.
	18		
SW	19	P	Switching Node Connecting to Output Inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET.Connect the 47nF bootstrap capacitor from SW to BTST.
	20		
BTST	21	P	High Side Switching MOSFET Gate Driver Power Supply. Connect a 10V or higher rating, 47nF ceramic capacitor between SW and BTST as the bootstrap capacitor for driving high side switching MOSFET (Q2).
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost-strap diode. Connect a 4.7μF (10 V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS pin.
PMID	23	DO	HSFET Drain Connection. Internally PMID is connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET.
NC	24	—	No Connect. Keep the pins float.
Thermal Pad	—	P	Thermal pad and ground reference. This pad is ground reference for the device and it is also the thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane through PCB vias under the pad.

Block Diagram



Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)]

Symbol	Parameter	Min	Max	Unit
Voltage Range (with respect to GND)	VBUS (converter not switching)	-2	18	V
Voltage Range (with respect to GND)	PMID (converter not switching)	-0.3	18	V
Voltage Range (with respect to GND)	BAT,SYS (converter not switching)	-0.3	6	V
Voltage Range (with respect to GND)	SW	-2(50ns)	18	V
Voltage Range (with respect to GND)	BTST (when converter switching)	-0.3	24	V
Voltage Range (with respect to GND)	CE, STAT, SCL, SDA, INT, REGN, QON	-0.3	6	V
Voltage Range (with respect to GND)	D+, D-, TS	-0.3	6	V
Differential Voltage	BTST to SW	-0.3	6	V
Output Sink Current	INT, STAT		6	mA
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C

Note1: Stresses beyond those listed under Absolute maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

ESD Ratings

Symbol	Parameter	Conditions	Value	Unit
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(2)]	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(3)]	± 500	

Note2: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

Note3: JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{VBUS}	Input voltage	3.9		13(4)	V
V_{BAT}	Battery voltage			4.8	V
I_{VBUS}	Input current			3	A
I_{SW}	Output current (SW)			3	A
I_{BAT}	Fast charging current			3	A
	RMS discharge current(continuously)			6	A
	Peak discharge current(up to 1s)			10	A
T_A	Operating ambient temperature	-40		85	°C

Note4: The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BTST or SW pins. A tight layout minimizes switching noise.

Thermal information

Symbol	Thermal Metric	ET95611CX	Unit
		QFN	
		24 Pins	
$R_{\theta JA}$	Junction to ambient thermal resistance	41.3	°C/W
$R_{\theta JC(top)}$	Junction to case (top) thermal resistance	26.1	°C/W

Electrical Characteristics

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS) in buck mode	V_{BAT} = 4 V, V_{VBUS} < V_{BUS_UVLOZ}, leakage between BAT and VBUS, T_J< 85°C			5	µA
I_{BAT}	Battery discharge current (BAT) in buck mode	V_{BAT} = 4 V, No VBUS, I²C Disabled, BATFET Disabled. T_J < 85°C		1		µA
I_{BAT}	Battery discharge current (BAT, SW, SYS)	V_{BAT} = 4 V, No VBUS, I²C Enabled, BATFET Enabled. T_J < 85°C		9		µA
I_{VBUS_HIZ}	Input supply current (VBUS) in buck mode	V_{VBUS} = 5 V, V_{BAT}= 4 V, High-Z Mode		14		µA
I_{VBUS_HIZ}	Input supply current (VBUS) in buck mode	V_{VBUS} = 9 V, V_{BAT}= 4 V, High-Z Mode		20		µA
I_{VBUS}	Quiescent input current (VBUS) in HIZ	V_{VBUS} = 5V, V_{BAT} = 4V, converter switching I_{SYS} = 0 A,		1.2		mA
I_{BOOST}	Battery Discharge Current in boost mode	V_{BAT} = 4.2 V, boost mode, I_{VBUS} = 0 A, converter switching, TS float, TS_IGNORE = 1		1		mA
VBUS / BAT POWER UP						
V_{VBUS_OP}	VBUS operating range	V_{VBUS} rising	3.9		13	V
V_{VBUS_OVP}	VBUS overvoltage rising threshold	VBUS rising, VBUS_OVP = 0	6.1	6.4	6.7	V
V_{VBUS_OVPZ}	VBUS overvoltage falling threshold	VBUS rising, VBUS_OVP = 0	5.6	5.9	6.2	V
V_{VBUS_OVP}	VBUS overvoltage rising threshold	VBUS rising, VBUS_OVP = 1	12.7	13	13.3	V
V_{VBUS_OVPZ}	VBUS overvoltage falling threshold	VBUS falling, VBUS_OVP = 1	12.2	12.5	12.8	V
V_{BUS_UVLOZ}	VBUS for active I²C, no battery	V_{VBUS} rising	3.2	3.35	3.5	V
$V_{BUS_UVLOZ_HYS}$	I²C active hysteresis	V_{VBUS} falling from above V_{VBUS_UVLOZ}		200		mV
V_{SLEEP}	Enter Sleep mode threshold	(V_{VBUS} - V_{BAT}), VBUS falling	9	45	85	mV
V_{SLEEPZ}	Exit Sleep mode threshold	(V_{VBUS} - V_{BAT}), VBUS rising	115	220	340	mV

Electrical Characteristics (Continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT_UVLOZ}	BAT voltage for active I²C, turn on BATFET, no VBUS	V_{BAT} rising	2.3	2.4	2.5	V
V_{BAT_UVLO}	BAT voltage to turn off I²C, turn off BATFET,no VBUS	V_{BAT} falling, VBAT_UVLO = 0	2.1	2.2	2.3	V
		V_{BAT} falling, VBAT_UVLO = 1	1.7	1.8	1.9	V
V_{BUSMIN_FALL}	Bad adapter detection falling threshold	VBUS falling	3.6	3.7	3.75	V
I_{BADSRC}	Bad adapter detection current source	Sink current from VBUS to GND		10		mA
POWER-PATH MANAGEMENT						
V_{SYS_MIN}	System regulation voltage	I_{SYS} = 0A, V_{BAT} < V_{SYSMIN} = B00h (3.52V), Charge Disabled	3.52	3.75		V
V_{SYSMIN_RNG}	VSYSMIN register range		2.56		3.84	V
$V_{SYSMIN_REG_STEP}$	VSYSMIN register step size			80		mV
$V_{SYS_REG_ACC}$	Typical system voltage regulation	I_{SYS}=0A, V_{BAT}>V_{SYSMIN}, Offset above V_{BAT};		50		mV
		I_{SYS}=0A, V_{BAT}<V_{SYSMIN}, Offset above V_{SYSMIN};		230		mV
$R_{ON(RBFET)}$	Top reverse blocking MOSFET on-resistance between VBUS and PMID - Q1	-40°C≤ T_A ≤ 125°C		37		mΩ
$R_{ON(HSFET)}$	Top switching MOSFET on-resistance between PMID and SW-Q2	V_{REGN} = 5V , -40°C≤ T_A ≤ 125°C		80		mΩ
$R_{ON(LSFET)}$	Bottom switching MOSFET on-resistance between SW and GND - Q3	V_{REGN} = 5V , -40°C≤ T_A ≤ 125°C		80		mΩ
$R_{ON(BAT-SYS)}$	SYS-BAT MOSFET on-resistance	QFN package, Measured from BAT to SYS, V_{BAT} = 4.2V, T_J = 25°C		30		mΩ

Electrical Characteristics (Continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BATTERY CHARGER						
V_{REG_RANGE}	Typical charge voltage regulation range		3.84		4.80	V
V_{REG_STEP}	Typical charge voltage step			10		mV
V_{REG_ACC}	Charge voltage accuracy	T_J = 25°C	-0.5		0.5	%
		T_J = -10°C - 85°C	-0.5		0.5	%
I_{CHG_RANGE}	Typical charge current regulation range		0.08		3.04	A
I_{CHG_STEP}	Typical charge current regulation step			80		mA
I_{CHG_ACC}	Charge current accuracy	V_{BAT} = 3.8V, I_{CHG} = 1760mA	-5.5		5.5	%
		V_{BAT} = 3.8V, I_{CHG} = 1040mA	-5.5		5.5	%
$V_{BATLOWV_FALL}$	Battery LOWV falling threshold	Transition from fast charge to pre-charge	2.7	2.8	2.9	V
$V_{BATLOWV_RISE}$	Battery LOWV rising threshold	Transition from pre-charge to fast charge	2.9	3	3.1	V
I_{PRECHG_RNG}	Typical pre-charge current range		100		620	mA
I_{PRECHG_STEP}	Typical pre-charge current step			20		mA
I_{PRECHG_ACC}	Pre-charge current accuracy when V_{BAT} below V_{SYSMIN} setting	V_{BAT} = 2.5V, I_{PRECHG} = 200mA, T_J = -10°C - 85°C	-20		20	%
I_{TERM_RANGE}	Typical termination current range		60		620	mA
I_{TERM_STEP}	Typical termination current step			10		mA
I_{TERM_ACC}	Termination current regulation accuracy	I_{TERM} = 300mA, T_J=-10°C-85°C	-20		20	%

Electrical Characteristics (Continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SHORTZ}	Battery short voltage rising threshold to start pre-charge	VBAT rising, VBAT_UVLO=0		2.25		V
V_{SHORT}	Battery short voltage falling threshold to stop pre-charge	VBAT falling, VBAT_UVLO=0		2.05		V
		VBAT falling, VBAT_UVLO=1		1.85		V
I_{SHORT}	Battery short trickle charging current	V_{BAT} < V_{BAT_SHORTZ}, $I_{TRICKLE}$ = 0		17		mA
		V_{BAT} < V_{BAT_SHORTZ}, $I_{TRICKLE}$ = 1		65		mA
V_{RECHG}	Battery recharge threshold below V_{REG}	V_{BAT} falling, VRECHG=1		200		mV
I_{BAT_LOAD}	Battery discharge load current			15		mA
I_{SYS_LOAD}	System discharge load current	V_{SYS}=4.2V		15		mA
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_RANGE}	Typical input voltage regulation range		3.8		13.2	V
V_{INDPM_STEP}	Typical input voltage regulation step			40		mV
V_{INDPM_ACC}	Input voltage regulation accuracy	V_{INDPM} = 4.6V	-4		4	%
		V_{INDPM} = 8V	-3		3	%
$V_{INDPM_BAT_ACC}$	Input voltage regulation accuracy tracking VBAT	VBAT=3.9V, VINDPM = 4V, VINDPM_BAT_TRACK=1,	4.15	4.3	4.45	V
I_{INDPM_RANGE}	Input Current limit range		0.1		3.0	A
I_{INDPM}	USB input current regulation limit	I_{INDPM}= 500mA, V_{VBUS}= 5V	400	450	500	mA
		I_{INDPM}= 900mA, V_{VBUS}= 5V	750	825	900	mA
		I_{INDPM}= 1500mA, V_{VBUS}= 5V	1350	1425	1500	mA
BATTERY OVER_VOLTAGE/CURRENT PROTECTION						
V_{BATOVP_RISE}	Battery over-voltage rising threshold	As percentage of V_{REG}	103	104	105	%
V_{BATOVP_FALL}	Battery over-voltage falling threshold	As percentage of V_{REG}	101	102	103	%
I_{BATFET_OCP}	BATFET over-current rising threshold		6			A
I_{BAT_PK}	Battery discharging peak current rising threshold	IBAT_PK = 10	6			A
		IBAT_PK = 11	12			A

Electrical Characteristics (Continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	TREG=1		120		°C
		TREG=0		100		°C
T_{SHUT}	Thermal Shutdown Rising Threshold	Temperature Increasing		140		°C
T_{SHUT_HYS}	Thermal Shutdown Falling Hysteresis	Temperature Decreasing by T_{SHUT_HYS}		30		°C
THERMISTOR COMPARATORS(CHARGE MODE)						
V_{TS_COLD}	TS pin rising voltage threshold for TH1 comparator to transition from TS_COOL to TS_COLD. Charge suspended above this voltage.	As Percentage to REGN reference (-5°C w/ 103AT), TS_TH1_TH2_TH3 = 100, 101, 110	75.0	75.5	76.0	%
		As Percentage to REGN reference (0°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 010, 011, 111	72.8	73.3	73.8	%
V_{TS_COLDZ}	TS pin rising voltage threshold for TH1 comparator to transition from TS_COOL to TS_COLD. Charge suspended above this voltage.	As Percentage to REGN reference (-2.5°C w/ 103AT), TS_TH1_TH2_TH3 = 100, 101, 110	73.9	74.4	74.9	%
		As Percentage to REGN reference (2.5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 010, 011, 111	71.7	72.2	72.7	%
V_{TS_COOL}	TS pin rising voltage threshold for TH2 comparator to transition from TS_PRECOOL to TS_COOL. TS_COOL charging settings used above this voltage.	As Percentage to TS pin bias reference (5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 100	70.6	71.1	71.6	%
		As Percentage to TS pin bias reference (10°C w/ 103AT), TS_TH1_TH2_TH3 = 001, 101, 110, 111	67.9	68.4	68.9	%
		As Percentage to TS pin bias reference (15°C w/ 103AT), TS_TH1_TH2_TH3 = 010	65.0	65.5	66.0	%
		As Percentage to TS pin bias reference (20°C w/ 103AT), TS_TH1_TH2_TH3 = 011	61.9	62.4	62.9	%

Electrical Characteristics (Continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TS_COOLZ}	TS pin falling voltage threshold for TH2 comparator to transition from TS_COOL to TS_PRECOOL. TS_PRECOOL charging settings resume below this voltage.	As Percentage to TS pin bias reference (7.5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 100	69.3	69.8	70.3	%
		As Percentage to TS pin bias reference (12.5°C w/ 103AT), TS_TH1_TH2_TH3 = 001, 101, 110, 111	66.6	67.1	67.6	%
		As Percentage to TS pin bias reference (17.5°C w/ 103AT), TS_TH1_TH2_TH3 = 010	63.7	64.2	64.7	%
		As Percentage to TS pin bias reference (22.5°C w/ 103AT), TS_TH1_TH2_TH3 = 011	60.6	61.1	61.6	%
$V_{TS_PRECOOL}$	TS pin rising voltage threshold for TH3 comparator to transition from TS_NORMAL to TS_PRECOOL. TS_PRECOOL charge settings used above this voltage.	As Percentage to TS pin bias reference (15°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 100, 101	65.0	65.5	66.0	%
		As Percentage to TS pin bias reference (20°C w/ 103AT), TS_TH1_TH2_TH3 = 010, 011, 110, 111	61.9	62.4	62.9	%
$V_{TS_PRECOOLZ}$	TS pin falling voltage threshold for TH3 comparator to transition from TS_PRECOOL to TS_NORMAL. Normal charging resumes below this voltage.	As Percentage to TS pin bias reference (17.5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 100, 101	63.7	64.2	64.7	%
		As Percentage to TS pin bias reference (22.5°C w/ 103AT), TS_TH1_TH2_TH3 = 010, 011, 110, 111	60.6	61.1	61.6	%
$V_{TS_PREWARM}$	TS pin falling voltage threshold for TH4 comparator to transition from TS_NORMAL to TS_PREWARM. TS_PREWARM charging settings used below this voltage.	As Percentage to TS pin bias reference (35°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 100, 101	51.5	52.0	52.5	%
		As Percentage to TS pin bias reference (40°C w/ 103AT), TS_TH4_TH5_TH6 = 011, 110, 111	47.9	48.4	48.9	%

Electrical Characteristics (Continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{TS_PREWARMZ}$	TS pin rising voltage threshold for TH4 comparator to transition from TS_PREWARM to TS_NORMAL. Normal charging resumes above this voltage.	As Percentage to TS pin bias reference (32.5°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 100, 101	53.3	53.8	54.3	%
		As Percentage to TS pin bias reference (37.5°C w/ 103AT), TS_TH4_TH5_TH6 = 011, 110, 111	49.2	49.7	50.2	%
V_{TS_WARM}	TS pin falling voltage threshold for TH5 comparator to transition from TS_PREWARM to TS_WARM. TS_WARM charging settings used below this voltage.	As Percentage to TS pin bias reference (40°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 100	47.9	48.4	48.9	%
		As Percentage to TS pin bias reference (45°C w/ 103AT), TS_TH4_TH5_TH6 = 001, 101, 110	44.3	44.8	45.3	%
		As Percentage to TS pin bias reference (50°C w/ 103AT), TS_TH4_TH5_TH6 = 010, 111	40.7	41.2	41.7	%
		As Percentage to TS pin bias reference (55°C w/ 103AT), TS_TH4_TH5_TH6 = 011	37.2	37.7	38.2	%
V_{TS_WARMZ}	TS pin rising voltage threshold for TH5 comparator to transition from TS_WARM to TS_PREWARM. TS_PREWARM charging settings resume above this voltage.	As Percentage to TS pin bias reference (37.5°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 100	49.2	49.7	50.2	%
		As Percentage to TS pin bias reference (42.5°C w/ 103AT), TS_TH4_TH5_TH6 = 001, 101, 110	45.6	46.1	46.6	%
		As Percentage to TS pin bias reference (47.5°C w/ 103AT), TS_TH4_TH5_TH6 = 010, 111	42.0	42.5	43.0	%
		As Percentage to TS pin bias reference (52.5°C w/ 103AT), TS_TH4_TH5_TH6 = 011	38.5	39.0	39.5	%

Electrical Characteristics (Continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TS_HOT}	TS pin falling voltage threshold for TH6 comparator to transition from TS_WARM to TS_HOT. Charging is suspended below this voltage.	As Percentage to TS pin bias reference (50°C w/ 103AT), TS_TH4_TH5_TH6 = 100 or 101	40.7	41.2	41.7	%
		As Percentage to TS pin bias reference (60°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 011, 110 or 111	33.9	34.4	34.9	%
V_{TS_HOTZ}	TS pin rising voltage threshold for TH6 comparator to transition from TS_HOT to TS_WARM. TS_WARM charging settings resume above this voltage.	As Percentage to TS pin bias reference (47.5°C w/ 103AT), TS_TH4_TH5_TH6 = 100 or 101	42.0	42.5	43.0	%
		As Percentage to TS pin bias reference (57.5°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 011, 110 or 111	35.2	35.7	36.2	%
THERMISTOR COMPARATORS (OTG MODE)						
$V_{TS_OTG_COLD}$	TS pin rising voltage threshold to transition from TS_OTG_NORMAL to TS_OTG_COLD. OTG suspended above this voltage.	As Percentage to TS pin bias reference (-20°C w/ 103AT), TS_TH_OTG_COLD = 0	79.5	80.0	80.5	%
		As Percentage to TS pin bias reference (-10°C w/ 103AT), TS_TH_OTG_COLD = 1	76.6	77.1	77.6	%
$V_{TS_OTG_COLDZ}$	TS pin falling voltage threshold to transition from TS_OTG_COLD to TS_OTG_NORMAL. OTG resumes below this voltage.	As Percentage to TS pin bias reference (-15°C w/ 103AT), TS_TH_OTG_COLD = 0	78.2	78.7	79.2	%
		As Percentage to TS pin bias reference (-5°C w/ 103AT), TS_TH_OTG_COLD = 1	75.0	75.5	76.5	%

Electrical Characteristics (Continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{TS_OTG_HOT}$	TS pin falling voltage threshold to transition from TS_OTG_NORMAL to TS_OTG_HOT. OTG suspended below this voltage.	As Percentage to TS pin bias reference (55°C w/ 103AT), TS_OTG_HOT = 00	37.2	37.7	38.2	%
		As Percentage to TS pin bias reference (60°C w/ 103AT), TS_OTG_HOT = 01	33.9	34.4	34.9	%
		As Percentage to TS pin bias reference (65°C w/ 103AT), TS_OTG_HOT = 10	30.8	31.3	31.8	%
$V_{TS_OTG_HOTZ}$	TS pin rising voltage threshold to transition from TS_OTG_HOT to TS_OTG_NORMAL. OTG resumes above this threshold.	As Percentage to TS pin bias reference (52.5°C w/ 103AT), TS_OTG_HOT = 00	38.5	39.0	39.5	%
		As Percentage to TS pin bias reference (57.5°C w/ 103AT), TS_OTG_HOT = 01	35.2	35.7	36.2	%
		As Percentage to TS pin bias reference (62.5°C w/ 103AT), TS_OTG_HOT = 10	32.0	32.5	33.0	%
PWM						
F_{SW}	PWM switching frequency	Oscillator frequency		1100		kHz
D_{MAX}	Maximum PWM duty cycle			97		%
BOOST MODE OPERATION						
V_{OTG_RANGE}	Typical OTG mode voltage regulation range		3.8		9.04	V
V_{OTG_STEP}	Typical OTG mode voltage regulation step			80		mV
V_{OTG_ACC}	OTG mode voltage regulation accuracy	I_{VBUS} = 0A, V_{OTG} = 5V	-3		3	%
		I_{VBUS} = 0A, V_{OTG} = 9V	-2		2	%

Electrical Characteristics (Continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT_OTG}	Battery voltage rising to enable OTG mode	V_{VBAT} rising, VBAT_OTG_MIN = 0	2.9	3.0	3.4	V
V_{BAT_OTGZ}	Battery voltage falling to disable OTG mode	V_{VBAT} falling, VBAT_OTG_MIN = 0	2.7	2.8	2.9	V
V_{BAT_OTG}	Battery voltage rising to enable OTG mode	V_{VBAT} rising, VBAT_OTG_MIN = 1	2.5	2.6	2.7	V
V_{BAT_OTGZ}	Battery voltage falling to disable OTG mode	V_{VBAT} falling, VBAT_OTG_MIN = 1	2.3	2.4	2.5	V
I_{OTG_RANGE}	OTG mode current regulation range		0.1		1.8	A
I_{OTG_STEP}	OTG mode current regulation step			20		mA
V_{OTG_OVP}	OTG overvoltage threshold	Rising threshold		V_{OTG} *1.09		V
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5V, I_{REGN} = 20mA	4.4	4.6		V
		V_{VBUS} = 9V, I_{REGN} = 20mA	4.8	5.0	5.2	V
LOGIC I/O PIN CHARACTERISTICS (CE, STAT, INT)						
V_{ILO}	Input low threshold				0.4	V
V_{IH}	Input high threshold		1.3			V
I_{BIAS}	High-level leakage current	Pull up rail 1.8 V			1	μA
V_{OL}	Low-level output voltage				0.4	V
I2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level	Pull up rail 1.8 V	1.3			V
V_{IL}	Input t low threshold level	Pull up rail 1.8 V			0.4	V
V_{OL}	Output low threshold level	Sink current = 5 mA,			0.4	V
ADC MEASUREMENT ACCURACY AND PERFORMANCE						
t_{ADC_CONV}	Conversion-time, Each Measurement	ADC_SAMPLE = 00		48		ms
		ADC_SAMPLE = 01		24		ms
		ADC_SAMPLE = 10		12		ms
		ADC_SAMPLE = 11		6		ms
ADC_{RES}	Effective Resolution	ADC_SAMPLE = 00	13	14		bits
		ADC_SAMPLE = 01	12	13		bits
		ADC_SAMPLE = 10	11	12		bits
		ADC_SAMPLE = 11	10	11		bits

Electrical Characteristics (Continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ADC MEASUREMENT RANGE AND LSB						
IBUS_ADC	ADC Bus Current Reading (both forward and OTG)	Range	-4		4	A
		LSB		1.0		mA
VBUS_ADC	ADC VBUS Voltage Reading	Range	0		10	V
		LSB		3.0		mV
VPMID_ADC	ADC PMID Volta+ge Reading	Range	0		10	V
		LSB		3.0		mV
VSYS_ADC	ADC SYS Volta+ge Reading	Range	0		6	V
		LSB		1.0		mV
VBAT_ADC	ADC BAT Voltage Reading	Range	0		6.0	V
		LSB		1.0		mV
IBAT_ADC	ADC BAT Current Reading	Range	-7.5		4.0	A
		LSB		2.0		mA
TS_ADC	ADC TS Voltage Reading	Range as a percent of REGN (-40°C to 85 °C for 103AT)	20.9		83.2	%
		LSB		0.09775		%
TDIE_ADC	ADC Die Temperature Reading	Range	-40		140	°C
		LSB		0.5		°C

Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBUS/BAT POWER UP						
t_{BADSRC}	Bad adapter detection duration			30		ms
BATTERY CHARGER						
t_{SAFETY_TRKCHG}	Charge safety timer accuracy in trickle charge		0.85	1	1.1	hr
t_{SAFETY_PRECHG}	Charge safety timer accuracy in pre-charge	PRECHG_TMR = 0	1.75	2	2.2	hr
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			10		μs
t_{SAFETY}	Charge safety timer accuracy in fast charge	CHG_TMR = 0	10.5	12	12.5	hr
QON TIMING						
t_{BATFET_DLY}	Time after writing to BATFET_CTRL before BATFET turned off for ship mode or shutdown	BATFET_DLY = 1		10		s
		BATFET_DLY = 0		24		ms
t_{SM_EXIT}	Deglitch time for QON to be pulled low in order to exit from Ship Mode		1.69	2	2.31	s
t_{QON_RST}	Time QON is held low to initiate system power reset		9.0	10.5	11.5	s
t_{BATFET_RST}	Duration that BATFET is disabled during system power reset			524		ms
DIGITAL CLOCK AND WATCHDOG						
t_{WDT}	Watchdog Reset time (EN_HIZ = 0, WATCHDOG = 200s)			200		s
f_{SCL}	SCL clock frequency				1.0	MHz

Detailed Description

Overview

The ET95611CX is a highly integrated 3.0A switch-mode battery charger for single cell Li-Ion and Li- polymer battery. It includes the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4), and bootstrap diode for the high-side gate driver.

Feature Description

Power-On-Reset (POR)

The ET95611CX power internal bias circuits from the higher voltage of VBUS and BAT. When either voltage rises above its under-voltage lockout (UVLO) threshold, all registers are reset to their POR values and the I^2C interface is enabled for communication. A non-maskable INT pulse is generated, after which the host can access all of the registers.

Device Power Up from Battery without Input Source

If only the battery is present and the V_{BAT} is above depletion threshold (V_{BAT_UVLOZ}), the ET95611CX performs a power-on reset then turns on the BATFET to connect the battery to system. The REGN LDO output remains off to minimize the quiescent current. The low R_{DSON} of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

Device Power Up from Input Source

When a valid input source is plugged in with $V_{BAT} < V_{BAT_UVLOZ}$, the ET95611CX performs a power-on reset then checks the input source voltage to turn on the REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. REGN LDO power up
2. Poor Source Qualification
3. Input source type detection using D+/ D- to set input current limit (I_{INDPM}) register and input source type
4. Input voltage limit threshold setting
5. Converter power-up

REGN LDO Power Up

The REGN LDO regulator supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN LDO also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

- V_{VBUS} above V_{VBUS_UVLOZ}
- V_{VBUS} above V_{BAT} + V_{SLEEPZ}
- EH_HIZ=0
- After 220ms delay is completed

If any one of the above conditions is not valid, the REGN LDO and the converter power stage remain off with the converter disabled. In this state, the battery supplies power to the system.

Poor Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet both of the following requirements in order to move forward to the next power on steps.

- VBUS voltage below V_{VBUS_OVP}
- VBUS voltage above $V_{POORSRC}$ when pulling I_{POORRC}

Once these conditions are met, the device proceeds to input source type detection.

D+/D- Detection Sets Input Current Limit in ET95611CX

After the REGN LDO is powered, the adapter has been qualified as a good source, and AUTO_INDET_EN bit = 1 (POR default), ET95611CX runs input source detection through D+/D- lines to detect USB Battery Charging Specification 1.2 (BC1.2) input sources (CDP / SDP / DCP) and non-standard adapters. If DCP is detected, ET95611CX runs HVDCP detection if either EN_9V is 1. The detection algorithm runs automatically each time that VBUS is plugged in, updating the IINDPM according to Table 2. If AUTO_INDET_EN = 0, the detection algorithm is not run and I_{INDPM} remains unchanged. The host can force the detection algorithm to run and update IINDPM by setting FORCE_INDET to 1.

The USB BC1.2 is able to identify Standard Downstream Port (SDP), Charging Downstream Port (CDP), and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer of 500ms is expired, the non-standard adapter detection is applied to set the input current limit.

The secondary detection is used to distinguish two types of charging ports (CDP and DCP). Most of the time, a CDP requires the portable device (such as smart phone, tablet) to send back an enumeration within 2.5 seconds of CDP plug-in. Otherwise, the port reverts back to SDP even though the D+/D– detection indicates CDP.

Upon the completion of input source type detection, the following registers are changed:

1. Input Current Limit(IINDPM) register is changed to set current limit
2. VBUS_STAT bits are updated to indicate the detected input source type

After detection completes, the host can over-write the IINDPM register to change the input current limit if needed.

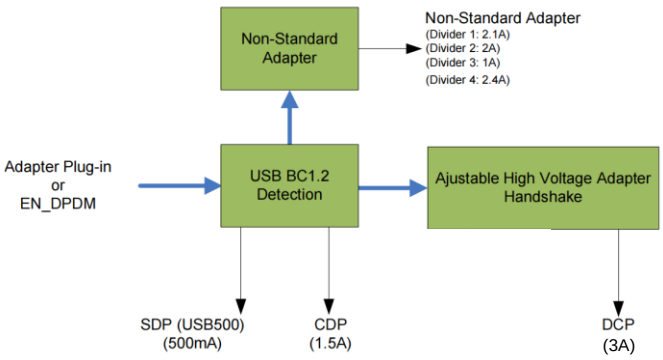


Figure 1. D+/D- Detection Flow

If DCP is detected (VBUS_STAT = 011), ET95611CX turns on $V_{D+D-_0p6V_SRC}$ on D+ if EN_DCP_BIAS is set to 1. Setting EN_DCP_BIAS to 0 while VBUS_STAT = 011 disables the $V_{D+D-_0p6V_SRC}$ on D+ pin, and setting EN_DCP_BIAS to 1 while VBUS_STAT = 011 enables the $V_{D+D-_0p6V_SRC}$ on D+ pin. The EN_HIZ bit has priority over EN_DCP_BIAS.

High Voltage Dedicated Charging Port (HVDCP) is used to negotiate 9V from the power source if BC1.2 DCP support is detected.

In order to remain in 9V HVDCP, ET95611CX must maintain a bias on D+ and D-, resulting in higher quiescent current. The host may remove this bias and associated quiescent current by setting EN_9V to 0 at any time. Setting EN_9V to 0 when an HVDCP adapter is providing 9V causes the adapter to revert to 5V DCP operation.

The non-standard detection is used to distinguish vendor specific adapters based on their unique dividers on the D+/D- pins. Comparators detect the voltage applied on each pin and determine the input current limit according to Table 1.

Table1. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D + THRESHOLD	D - THRESHOLD	INPUT CURRENT LIMIT (A)
Divider 1	V_{D+} within V_{D+D-_2P0}	V_{D-} within V_{D+D-_2P8}	1
Divider 2	V_{D+} within V_{D+D-_2P8}	V_{D-} within V_{D+D-_2P0}	2.1
Divider 3	V_{D+} within V_{D+D-_2P8}	V_{D-} within V_{D+D-_2P8}	2.4

Table2. Input Current Limit Setting from D+/D- Detection

D+/ D- DETECTION	INPUT CURRENT LIMIT (IINLIM)	VBUS_STAT
USB SDP (USB500)	500mA	0x1
USB CDP	1.5A	0x2
USB DCP	1.5A	0x3
Divider 1	1 A	0x5
Divider 2	2.1 A	0x5
Divider 3	2.4 A	0x5
HVDCP	1.5A	0x6
Unknown 5V Adapter	500mA	0x4

Input Voltage Limit Threshold Setting (VINDPM Threshold)

The ET95611CX support a wide range of input voltage limit (3.8V – 13.2V). Its POR default V_{INDPM} threshold is set at 4.6V. The ET95611CX also support dynamic V_{INDPM} tracking, which tracks the battery voltage to ensure a sufficient margin between input and battery voltages for proper operation of the buck converter. This function is enabled via the VINDPM_BAT_TRACK register bit. When enabled, the actual input voltage limit is the higher of the VINDPM register or $V_{INDPM_BAT_TRACK}$ (V_{BAT} + 400mV typical offset.)

Converter Power-Up

After the input current and voltage limits are set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, the BATFET turns off. Otherwise, the BATFET stays on to charge the

battery. Converter startup requires the following conditions:

- VBUS has passed poor source qualification
- VBUS > V_{BAT} + V_{SLEEPZ}
- V_{VBUS} < V_{VBUS_OVP}
- EN_HIZ = 0
- V_{SYS} < V_{SYS_OVP}
- T_J < T_{SHUT}

The ET95611CX provide soft start when the system rail is ramped up by setting I_{INDPM} to its lowest programmable value and stepping up through each available setting until reaching the value set by IINDPM register. Concurrently, the system short protection limits the output current to approximately 0.5A when the system rail is below V_{SYS_SHORT}.

The device uses a highly efficient 1.1MHz, fixed frequency pulse width modulated (PWM) step-down switching regulator. The internally compensated feedback loop keep tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The device switches to pulse frequency modulation (PFM) control at light load condition. The PFM_FWD_DIS and PFM_OTG_DIS bits can be used to disable the PFM operation in buck and boost respectively.

Boost Mode Operation From Battery

ET95611CX support boost converter operation to deliver power from the battery to VBUS. The output voltage and maximum current are set in the VOTG and IOTG registers, respectively. VBUS_STAT is set to 111 upon a successful entry into boost OTG. The boost operation is enabled when the following conditions are met:

1. V_{BAT} above V_{BAT_OTG}
2. V_{VBUS} less than $V_{BAT+VSLEEP}$
3. Boost mode operation is enabled (EN_OTG = 1)
4. $V_{TS_OTG_HOT}$ < V_{TS} < $V_{TS_OTG_COLD}$
5. V_{REGN} > V_{REGN_OK}
6. 30 ms delay after EN_OTG = 1
7. Boost mode regulation voltage in REG0x0C is greater than 105% of battery voltage.

Host Mode and Standalone Power Management

Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1, and an INT is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit would read as 1 upon the first read and then 0 upon subsequent reads. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 1-hour trickle charging safety timer, 2 hour pre-charging safety timer and the 12 hour fast charging safety timer. At the end of the 1 hour or 2 hour or 12 hour timer expired, the charging is stopped and the buck converter continues to operate to supply system load.

A write to any I^2C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog expires, the device returns to default mode. The ICHG value is divided in half when the watchdog timer expires, and a number of other fields are reset to their POR default values as shown in the notes column of the register tables in Section 8.6. When watchdog timer expires, WD_STAT and WD_FLAG is set to 1, and an INT is asserted low to alert the host (unless masked by WD_MASK).

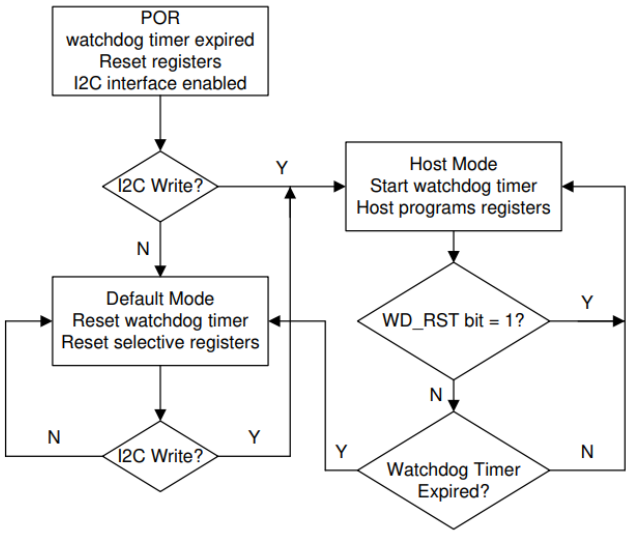


Figure 2. Watchdog Timer Flow Chart

Register Bit Reset

Beside a register reset by the watchdog timer in default mode, the register and the timer can be reset to the default value by writing the REG_RST bit to 1. The register bits, which can be reset by the REG_RST bit, are noted in the Register Map section. After the register reset, the REG_RST bit goes back from 1 to 0 automatically.

Power Path Management

The ET95611CX accommodate a wide range of input sources from a USB, wall adapter, wireless charger, to car charger. They provide automatic power path selection to supply the system from an input source, battery, or both.

Battery Charging Management

The ET95611CX charge a 1-cell Li-Ion battery with up to a 3A charge current. The 30mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit = 1 and CE pin is LOW), the ET95611CX autonomously complete a charging cycle without host involvement. The device default charging parameters are listed in Table 3. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I^2C.

Table3. Charging Parameter Default Setting

VREG	VRECHG	ITRICKLE	IPRECHG	ICHG	ITERM	TOPOFF TIMER
4.2V	VREG - 200mV	17mA	100mA	1040mA	100mA	Disabled

A new charge cycle starts when the following conditions are valid:

- Converter Power-Up
- EN_CHG=1
- CE pin is low
- No thermistor fault on TS
- No safety timer fault

The ET95611CX automatically terminate the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM or thermal regulation. When a fully charged battery is discharged below VRECHG, the device automatically starts a new charging cycle. After charging terminates, toggling CE pin or EN_CHG bit also initiates a new charging cycle.

The STAT output indicates the charging status. Refer to Charging Status Indicator for details of STAT pin operation. In addition, the status register (CHG_STAT) indicates the different charging phases: 00-charging disabled or terminated, 01-constant current, 10 constant voltage, 11-topoff charging.

Battery Charging Profile

The ET95611CX charge the battery in five phases: trickle charge, pre-charge, constant current, constant voltage and an optional top-off charging phase. At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

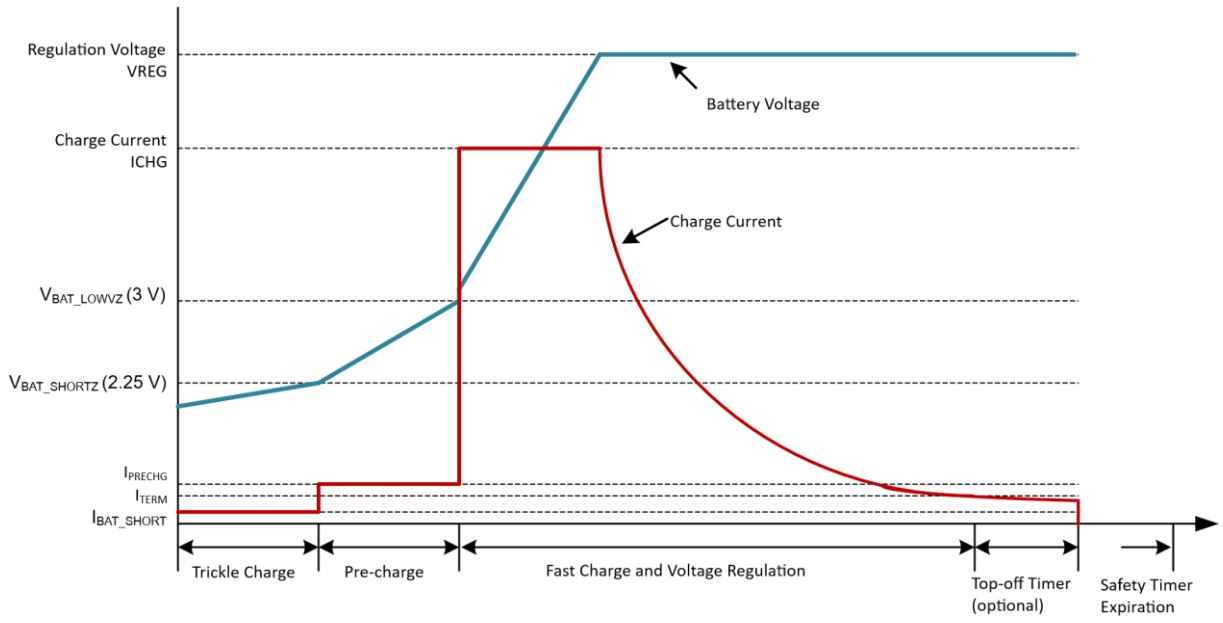


Figure 3. Battery Charging Profile

Charging Termination

The ET95611CX terminate a charge cycle when the battery voltage is above recharge threshold, the converter is in constant-voltage regulation and the current is below I_{TERM}. Because constant-voltage regulation is required for termination, the ET95611CX do not terminate while I_{INDPM}, V_{INDPM} or thermal regulation loops are active. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and the BATFET can turn on again to engage supplement mode. Termination can be permanently disabled by writing 0 to EN_TERM bit prior to charge termination.

At low termination currents, due to the comparator offset, the actual termination current may be 10mA to 20mA higher than the termination target. In order to compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. The top-off timer follows safety timer constraints, such that if the safety timers suspend, so does the top-off timer. Similarly, if the safety timers count at half-clock rate, so does the top-off timer. Refer to Charging Safety Timers for the list of conditions. The host can read CHG_STAT to find out the termination status.

Top-off timer gets reset by any of the following conditions:

1. Charging cycle stop and restart (toggle CE pin, toggle EN_CHG bit, charged battery falls below recharge threshold or adapter removed and replugged)
2. Termination status low to high
3. REG_RST register bit is set

The top-off timer settings are read in after is detected by the charger. Programming a top-off timer value after

termination has no effect unless a recharge cycle is initiated. CHG_FLAG is set to 1 when entering top-off timer segment and again when the top-off timer expires.

Thermistor Qualification

The ET95611CX provide a single thermistor input for battery temperature monitoring. The TS pin input of the battery temperature can be ignored by the charger if TS_IGNORE = 1. When the TS pin feedback is ignored, the charger considers the TS to always be valid for charging mode and OTG mode, and TS_STAT always reports 000. The TS pin may be left floating if TS_IGNORE is set to 1.

When TS_IGNORE=1, the TS_ADC channel is disabled, with TS_ADC_DIS forced to 1; Attempting to write to 0 is ignored.

When TS_IGNORE = 0, the charger adjusts the charging profile based on the TS pin feedback information according to the configurable profile described in Advanced Temperature Profile in Charge Mode. When the battery temperature crosses from one temperature range to another, TS_STAT is updated accordingly, and the charger sets the FLAG bit for the newly-entered temperature range. If TS_MASK is set to 0, any change to TS_STAT, including a transition to TS_NORMAL, generates an INT pulse.

Advanced Temperature Profile in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges. As battery technology continues to evolve, battery manufacturers have released temperature safety specifications that extend beyond the JEITA standard. The ET95611CX feature a highly flexible temperature-based charging profile to meet these advanced specifications while remaining backwards compatible with the original JEITA standard. Figure 4. shows the programmability for charger behavior under different battery temperature (TS) operating regions.

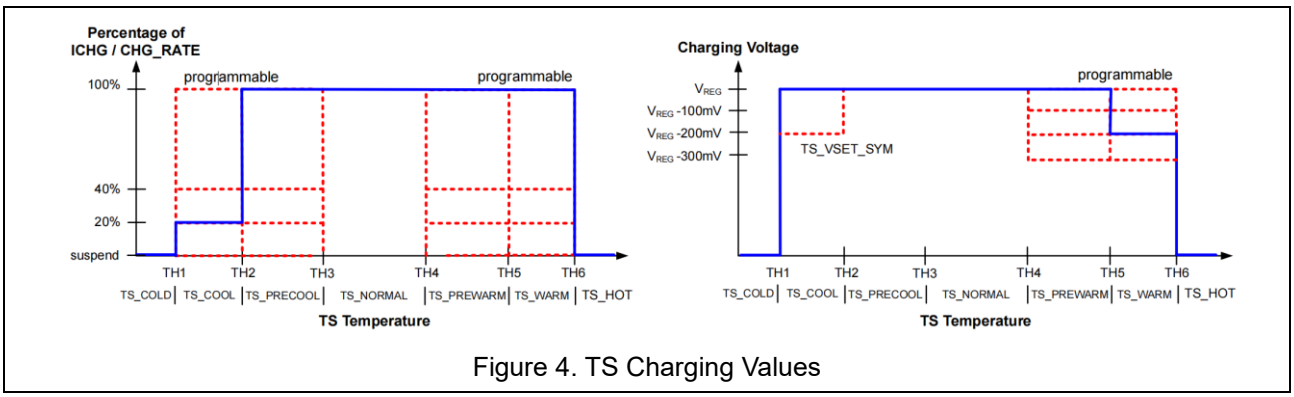


Figure 4. TS Charging Values

Charging safety timer is adjusted within the temperature zones to reflect changes to the charging current. When IPRECHG and ICHG are reduced to 20% or 40% in the cool or warm temperature zones, the charging safety timer counts at half rate. If charging is suspended, the safety timer is suspended, the STAT pin blinks and CHG_STAT is set to 00 (not charging or charge terminated.)

TS Pin Thermistor Configuration

The typical TS resistor network is illustrated below.

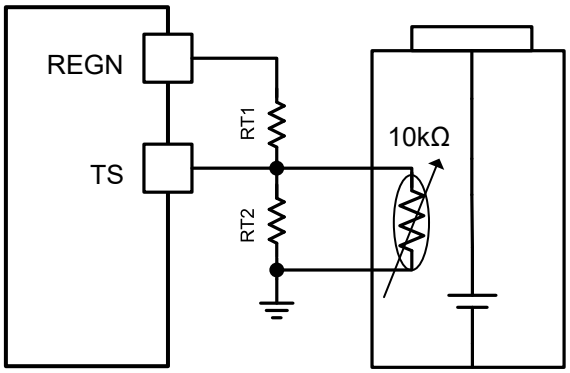


Figure 4. TS Resistor Network

The value of RT1 and RT2 are determined from the resistance of the thermistor at 0ºC and 60ºC (RTH_{0degC} and RTH_{60degC}) and the corresponding voltage thresholds V_{TS_0degC} and V_{TS_60degC} (expressed as percentage of REGN with value between 0 and 1). For the most accurate thermistor curve fitting, use the rising threshold for V_{TS_COLD} at 0ºC and the falling threshold for V_{TS_HOT} at 60ºC, regardless of the actual register settings for TS_TH1_TH2_TH3 and TS_TH4_TH5_TH6.

$$RT2 = \frac{RTH_{0degC} * RTH_{60degC} * (\frac{1}{V_{TS_0degC}} - \frac{1}{V_{TS_60degC}})}{RTH_{60degC} * \left(\frac{1}{V_{TS_{0degC}}} - 1\right) - RTH_{0degC} * \left(\frac{1}{V_{TS_{0degC}}} - 1\right)}$$

$$RT1 = \frac{\frac{1}{V_{TS_0degC}} - 1}{\frac{1}{R_{T2}} + \frac{1}{RTH_{0degC}}}$$

Assuming a 103AT NTC thermistor on the battery pack, the RT1 and RT2 are calculated to be 5.23kΩ and 30.1kΩ respectively.

Boost Mode Thermistor Monitor During Battery Discharge Mode

For battery protection during boost OTG, ET95611CX monitor the battery temperature to be within the TS_TH_OTG_COLD to TS_TH_OTG_HOT register settings. For a 103AT NTC thermistor with RT1 of 5.3kΩ and RT2 of 31.1kΩ, TS_TH_OTG_COLD default is -10°C and TS_TH_OTG_HOT default is 60°C. When temperature is outside of this range, the OTG mode is suspended with REGN remaining on. In addition, VBUS_STAT bits are set to 000, TS_STAT is set to 001 (TS_OTG_COLD) or 010 (TS_OTG_HOT), and TS_FLAG is set. Once the battery temperature returns to normal temperature, the boost OTG is restarted and TS_STAT returns to 000 (TS_NORMAL).

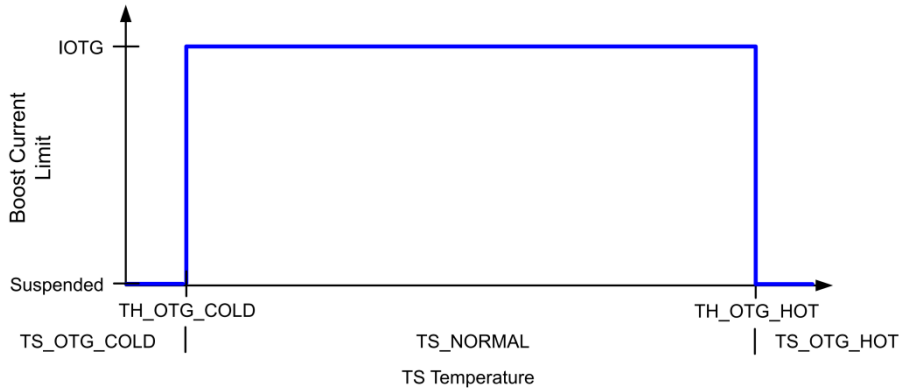


Figure 5. TS Pin Thermistor Sense Threshold in Boost Mode

Charging Safety Timer

The ET95611CX have three built-in safety timers to prevent extended charging cycle due to abnormal battery conditions. The fast charge safety timer and pre-charge safety timers are set through I^2C CHG_TMR and PRECHG_TMR fields, respectively. The trickle charge timer is fixed at 1 hour.

The trickle charging, pre-charging and fast charging safety timers can be disabled by setting EN_SAFETY_TMRS = 0. EN_SAFETY_TMRS can be enabled anytime regardless of which charging stage the charger is in. Each timer starts to count as soon as the following two conditions are simultaneously true: EN_SAFETY_TMRS = 1 and the corresponding charging stage is active.

When either the fast charging, trickle charging or pre-charging safety timer expires, the SAFETY_TMR_STAT and SAFETY_TMR_FLAG bits are set to 1.

Events that cause a reduction in charging current also cause the charging safety timer to count at half-clock rate if TMR2X_EN bit is set.

During faults which suspend charging, the charge, pre-charge and trickle safety timers are also suspended, regardless of the state of the TMR2X_EN bit. Once the fault goes away, charging resumes and the safety timer resumes from where it stopped.

The charging safety timer and the charging termination can be disabled at the same time. Under this condition, the charging keeps running until it is disabled by the host.

Integrated 14Bit ADC for Monitoring

The ET95611CX provide an integrated 14bit ADC for the host to monitor various system parameters.

To enable the ADC, the ADC_EN bit must be set to ‘1’. The ADC is disabled by default (ADC_EN = 0) to conserve power. The ADC is allowed to operate only in charging mode. When the charger enters HIZ mode, the ADC is temporarily suspended.

The ADC_DONE_STAT, ADC_DONE_FLAG bits are set when a conversion is complete in one-shot mode only. During continuous conversion mode, the ADC_DONE_STAT, ADC_DONE_FLAG bits have no meaning and remain at 0. In one-shot mode, the ADC_EN bit is set to 0 at the completion of the conversion, at the same time as the ADC_DONE_FLAG bit is set. In continuous mode, the ADC_EN bit remains at 1 until the user disables the ADC by setting it to 0.

Device Functional Modes

Narrow VDC Architecture

The ET95611CX uses the Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by VSYSMIN register setting. Even with a fully depleted battery, the system is regulated to the minimum system voltage. If charging is enabled, the BATFET operates in linear mode (LDO mode). The default minimum system voltage at POR is 3.52V.

As the battery voltage rises above the minimum system voltage, the BATFET is turned fully on. When battery charging is disabled and VBAT is above the minimum system voltage setting, or charging is terminated, the system is regulated 50mV (typical) above battery voltage.

Dynamic Power Management

To meet the USB maximum current limit and avoid overloading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When the input source is overloaded, either the current exceeds the input current limit (IINDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage by VSUPP, the device automatically enters the supplement mode where the BATFET turns on and the battery starts discharging so that the system is supported from both the input source and battery.

High Impedance Mode

The host may place the ET95611CX into high impedance mode by writing EN_HIZ = 1. In high impedance mode, RBFET (Q1), HSFET (Q2) and LSFET (Q3) are turned off. The RBFET and HSFET block current flow to and from VBUS, putting the VBUS pin into a high impedance state. The BATFET (Q4) is turned on to connect the BAT to SYS. During high impedance mode, REGN is disabled and the digital clock is slowed to conserve power.

Ship Mode

The host may place the ET95611CX into ship mode by setting BATFET_CTRL = 10. In ship mode, the BATFET is turned off to prevent the battery from powering the system, and the I^2C is disabled. Ship mode has slightly higher quiescent current than shutdown mode, but QON may be used to exit from ship mode. The ET95611CX is taken out of ship mode by either of these methods:

- Pulling the QON pin low for t_{SM_EXIT}
- $V_{VBUS} > V_{VBUS_UVLOZ}$ (adapter plug-in)

When the ET95611CX exit from ship mode, the registers are reset to their POR values.

Ship mode is only entered when the adapter is not present. Setting BATFET_CTRL = 10 while $V_{VBUS} > V_{VBUS_UVLOZ}$ (adapter present) either disables the BATFET or has no immediate effect depending on the setting of BATFET_CTRL_WVBUS.

When BATFET_CTRL_WVBUS is set to 0 and $V_{VBUS} > V_{VBUS_UVLO}$ (adapter present), setting BATFET_CTRL =

10 has no immediate effect. If the adapter is removed while BATFET_CTRL is set to 10, then the BATFET is disabled and the device enters ship mode. The BATFET turns off either after t_{BATFET_DLY} or when the adapter is removed, whichever comes later.

When BATFET_CTRL_WVBUS is set to 1 and $V_{VBUS} > V_{VBUS_UVLO}$ (adapter present), setting BATFET_CTRL = 10 turns off the BATFET after t_{BATFET_DLY}. The converter continues to run while the adapter is present, supplying SYS power from the adapter. If the adapter is removed while BATFET_CTRL is set to 10, the ET95611CX enters ship mode. Ship mode is entered either after t_{BATFET_DLY} or when the adapter is removed, whichever comes later.

System Power Reset

The BATFET functions as a load switch between battery and system when the converter is not running. By changing the state of BATFET from on to off, systems connected to SYS can be power cycled. Any of the following conditions initiates a system power reset:

- BATFET_CTRL_WVBUS = 1 and QON is pulled low for t_{QON_RST}
- BATFET_CTRL_WVBUS = 1 and BATFET_CTRL = 11
- BATFET_CTRL_WVBUS = 0 and $V_{VBUS} < V_{VBUS_UVLO}$ simultaneously with QON pulled low for t_{QON_RST}
- BATFET_CTRL_WVBUS = 0 and $V_{VBUS} < V_{VBUS_UVLO}$ and BATFET_CTRL = 11

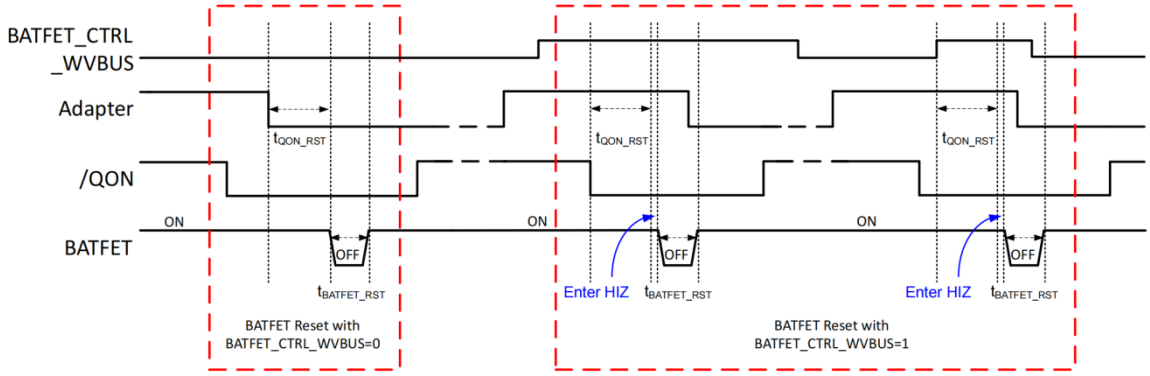


Figure 6.System Power Reset Timing

When BATFET_CTRL_WVBUS is set to 1, system power reset proceeds if either BATFET_CTRL is set to 11 or QON is pulled low for t_{QON_RST}, regardless of whether VBUS is present or not . There is a delay of t_{BATFET_DLY} before initiating the system power reset. If QON is pulled low, there is no delay after the t_{QON_RST} completes, regardless of BATFET_DLY setting.

The system power reset can be initiated from the battery only condition, from OTG mode or from the forward charging mode with adapter present. If the system power is reset when the charger is in boost OTG mode, the boost OTG mode is first stopped by setting EN_OTG = 0.

BATFET Control

The ET95611CX have an integrated, bi-directionally blocking BATFET that can be turned off to remove leakage current from the battery to the system. The BATFET is controlled by the BATFET_CTRL register bits, and supports shutdown mode, ship mode and system power reset.

Table 4. BATFET Control Modes

MODE	BATFET	I²C	ENTRY, NO ADAPTER	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS = 0	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS = 1	EXIT
Normal	On	Active	N/A	N/A	N/A	N/A
Ship mode	Off	Off	Writing BATFET_CTRL = 0 turns off BATFET after BATFET_DLY and enters ship mode.	Writing BATFET_CTRL = 10 has no effect while adapter is present. When both BATFET_DLY has expired and the adapter is removed, the device turns off BATFET and enters ship mode. Writing BATFET_CTRL = 00 before adapter is removed aborts ship mode.	Writing BATFET_CTRL = 10 turns off BATFET after BATFET_DLY. When both BATFET_DLY has expired and adapter is removed, the device enters ship mode. Writing BATFET_CTRL = 00 before adapter is removed turns BATFET on and aborts ship mode.	QON or adapter plug-in
System reset	On to Off to On	Active	Writing BATFET_CTRL = 11 initiates system reset after BATFET_DLY. Holding QON low for t_{QON_RST} initiates immediate reset (BATFET_DLY is not applied.)	Writing BATFET_CTRL = 11 is ignored and BATFET_CTRL resets to 00. Holding QON low for t_{QON_RST} is ignored.	Writing BATFET_CTRL = 11 initiates system reset after BATFET_DLY. Holding QON low for t_{QON_RST} initiates immediate reset. Converter is placed in HIZ during system reset and exits HIZ when system reset completes.	N/A

Status Outputs(STAT, INT)

Charging Status Indicator (STAT)

The ET95611CX indicates charging state on the open drain STAT pin. The STAT pin can drive an LED. The STAT pin function can be disabled via the DIS_STAT bit.

Table 5. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Not charging, no fault detected. (Includes charging complete, Charge Disabled, no adapter present, in OTG mode.)	HIGH
Charge suspend	Blinking at 1Hz

Interrupt to Host(INT)

In many applications, the host does not continually poll the charger status registers. Instead, the INT pin may be used to notify the host of a status change with a 256μs INT pulse. Upon receiving the interrupt pulse, the host may read the flag registers (Charger_Flag_X and FAULT_Flag_X) to determine the event that caused the interrupt, and for each flagged event, read the corresponding status registers (Charger_Status_X and FAULT_Status_X) to determine the current state. Once set to 1, the flag bits remain latched at 1 until they are read by the host, which clears them. The status bits, however, are updated whenever there is a change to status and always represent the current state of the system.

All of the INT events can be masked off to prevent INT pulses from being sent out when they occur, with the exception of the initial power-up interrupt. Interrupt events are masked by setting their mask bit in registers (Charger_Mask_X and FAULT_Mask_X). Events always cause the corresponding flag bit to be set to 1, regardless of whether or not the interrupt pulse has been masked.

Interrupts and Status, Flag and Mask Bits

The device incorporates an interrupt pin (INT) to inform a host microcontroller of status changes without requiring microcontroller polling. Each reported event has a status field, a flag bit and a mask bit. The status field reports the status at the time that it is read. The flag bit is latched and, once set to 1, will remain at 1 until the host reads the bit, which will clear it to 0. The mask bit determines whether or not an interrupt pulse will be generated when the flag bit is set.

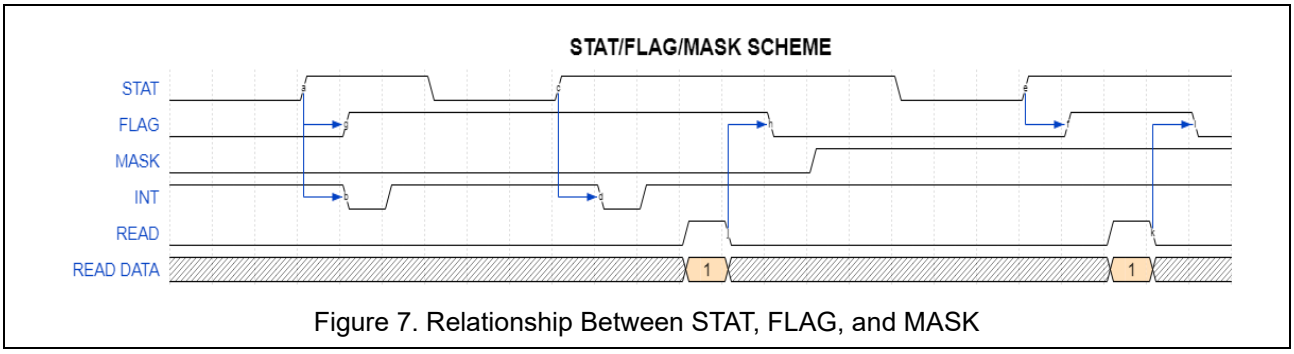


Figure 7. Relationship Between STAT, FLAG, and MASK

The flag bit is set upon certain transitions of the status field. These transitions also generate an INT pulse if the associated mask bit is set to 0. Because the INT is generated from the status field transition and not the flag bit, an INT pulse is sent to the host even if the associated flag is already set to 1 when the status transition occurs. Details of this behavior are shown in Figure 7.

The default behavior is to generate a 256μs INT pulse when any flag bit is set to 1. These pulses may be masked out on a flag-by-flag basis by setting a flag's mask bit to 1. Setting the mask bit does not affect the

transition of the flag bit from 0 to 1, only the generation of the 256μs INT pulse.

Protections

Voltage and Current Monitoring in Battery Only and HIZ Modes

The ET95611CX monitors a reduced set of voltages and currents when operating from battery without an adapter or when operating from battery in high impedance mode.

Battery Under-voltage Lockout

In battery-only mode, the ET95611CX disables the BATFET if V_{BAT} falls below V_{BAT_UVLO}, separating the system from the battery. I^2C is disabled as well. Upon exit from the under-voltage lockout condition when either V_{BAT} rises above V_{BAT_UVLOZ} or V_{VBUS} rises above V_{VBUS_UVLOZ}, I^2C will be re-enabled and the registers are reset to their POR values.

Battery Over-current Protection

The ET95611CX has a two-level battery over-current protection. The I_{BAT_PK} threshold is set by I_{BAT_PK} and provides a fast (100μs) protection for the battery discharging. I_{BATFET_OCP} provides a slower (50ms), fixed threshold protection for the BATFET. If the battery discharge current becomes higher than either threshold for its protection timer, the BAT_FAULT_STAT and BAT_FAULT_FLAG fault register bits are set to 1, and the BATFET enters hiccup mode with 100ms off-time and ~1% on-time. The BAT_FAULT_STAT will return to 0 once the BATFET is disabled for the hiccup mode. Once the BATFET is turned back on, the I_{BAT_PK} and I_{BATFET_OCP} thresholds are re-evaluated. In boost OTG mode, if the battery discharging current is higher than either I_{BAT_PK} or I_{BATFET_OCP} for their respective protection timers, the charger exits OTG mode by clearing the EN_OTG bit.

Voltage and Current Monitoring in Buck Mode

Input Over-voltage

If VBUS voltage rises above V_{VBUS_OVP}, the converter stops switching to protect the internal power MOSFETs and I_{PMID_LOAD} discharge current is applied to bring down VBUS voltage. VBUS_FAULT_FLAG and VBUS_FAULT_STAT are set to 1. When VBUS falls back below V_{VBUS_OVPZ}, VBUS_OVP_STAT will transition to 0 and the converter will resume switching.

System Over-voltage Protection (SYSOVP)

When V_{SYS} rises above the V_{SYS_OVP} threshold (around 250mV above VBAT when not charging) in forward converter operation, the converter stops switching to limit voltage overshoot and applies I_{SYS_LOAD} to pull down the system voltage. VSYS_FAULT_FLAG and VSYS_FAULT_STAT are set to 1. Once VSYS drops below V_{SYS_OVP}, the converter resumes switching, the 15mA discharge current is removed and VSYS_FAULT_STAT transitions to 0.

Forward Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak over-current protection in the switching MOSFETs. In forward mode, if the current through Q2 exceeds I_{HSFET_OCP}, the converter will immediately turn off the high-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

Battery Over-voltage Protection (BATOVP)

When V_{BAT} transitions above V_{BAT_OVP}, the ET95611CX disables charging by disabling the BATFET and applies I_{BAT_LOAD} current source to discharge excess BAT voltage. If battery voltage remains above the threshold , BAT_FAULT_FLAG is set to 1 and BAT_FAULT_STAT transitions to 1. Once V_{BAT} falls below V_{BAT_OVPZ}, charging resumes and BAT_FAULT_STAT transitions back to 0.

Sleep and Poor Source Comparators

The sleep comparator is used to suspend the converter if the adapter voltage is insufficient to maintain buck converter operation while charging the battery. If V_{VBUS} falls below V_{BAT} + V_{SLEEP} , the converter stops switching, VBUS_FAULT_STAT and VBUS_FAULT_FLAG are set to 1. If V_{VBUS} rises back above V_{BAT} + V_{SLEEPZ}, the converter restarts.

If V_{VBUS} falls below $V_{POORSRC}$, the converter stops switching and the VBUS_STAT transitions to 000 and the device transitions to battery-only mode. If V_{VBUS} rises above $V_{POORSRC}$, it is a new adapter attach, and poor source qualification will be run in addition to D+/D- detection if enabled. VBUS_STAT will be determined by the adapter attach sequence as outlined in Device Power Up from Input Source.

Voltage and Current Monitoring in Boost Mode

ET95611CX closely monitors VBUS, SYS and BAT voltages, as well as VBUS, BAT and LSFET currents to ensure safe boost mode operation.

Boost Mode Over-voltage Protection

During OTG operation, ET95611CX uses two comparators to sense output over-voltage at VBUS and PMID. If either VBUS or PMID voltage rises above their OVP threshholds, the converter stops switching and attempts to discharge the voltage.

If the OVP condition persists (200μs), OTG_FAULT_FLAG is set to 1, OTG_FAULT_STAT transitions to 1 and the converter powers down into a fault condition.

Boost Mode Duty Cycle Protection

After an initial startup blanking period, ET95611CX monitors the PMID voltage during boost OTG mode to ensure that PMID voltage remains sufficiently above V_{SYS} to maintain the minimum duty cycle. If V_{PMID} falls below V_{BOOST_DUTY} (105% V_{SYS} typical), the converter stops and enters hiccup mode.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

Boost Mode PMID Under-voltage Protection

During boost OTG mode, ET95611CX converter monitors PMID for under-voltage. If the PMID voltage falls below V_{OTG_UVP}, the converter stops and enters hiccup mode.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

Boost Mode Battery Under-voltage

If V_{BAT} falls below V_{BAT_OTGZ} during OTG mode, the charger exits OTG mode by setting EN_OTG = 0, and BAT_FAULT_STAT and BAT_FAULT_FLAG are set to 1. Setting EN_OTG = 1 while $V_{BAT} < V_{BAT_OTG}$ will not enter OTG and the EN_OTG bit will be cleared to 0. When the battery is charged above V_{BAT_OTG}, OTG mode may be entered by setting EN_OTG = 1.

Boost Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak over-current protection in the switching MOSFETs. In OTG mode, if the current through Q3 exceeds I_{LSFET_OCP}, the converter will immediately turn off the low-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

Boost Mode SYS Short

If V_{SYS} falls below V_{SYS_SHORT} in boost OTG mode, ET95611CX immediately stops the boost converter, enters hiccup mode, and sets SYS_FAULT_FLAG to 1.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

Thermal Regulation and Thermal Shutdown

Thermal Protection in Buck Mode

The ET95611CX monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in buck mode. When the internal junction temperature exceeds the T_{REG} thermal regulation limit (T_{REG} register configuration), the device lowers the charging current. During thermal regulation, the safety timer runs at half the clock rate, and the TREG_FLAG and TREG_STAT bits are set to 1. Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC junction temperature exceeds T_{SHUT}. The fault bit TSHUT_FLAG is set to 1 and TSHUT_STAT transitions to 1. The BATFET and converter are re-enabled when IC temperature is T_{SHUT_HYS} below T_{SHUT}, and T_{SHUT_STAT} transitions to 0.

Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds T_{SHUT}, the boost mode is disabled by setting EN_OTG bit low and BATFET is turned off, and TSHUT_FLAG is set to 1. When IC junction temperature is below T_{SHUT} - T_{SHUT_HYS}, the BATFET is enabled automatically to allow system to restore and the host can re-enable EN_OTG bit to recover.

Thermal Protection in Battery-Only Mode

The ET95611CX monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in battery-only mode. The device has thermal shutdown to turn off the BATFET when IC junction temperature exceeds T_{SHUT}. The fault bit TSHUT_FLAG is set to 1 and TSHUT_STAT transitions to 1. The BATFET is re-enabled when IC temperature is T_{SHUT_HYS} below T_{SHUT}, and TSHUT_STAT transitions to 0.

Programming

Serial Interface

The ET95611CX uses an I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I²C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL).

The device has 7-bit I²C address 0x6B, receiving control inputs from a host device such as a micro-controller or digital signal processor through register addresses 0x02 - 0x38. The host device initiates all transfers and the charger responds. Register reads outside of these addresses return 0xFF. When the bus is free, both SDA and SCL lines are HIGH.

The I²C interface supports standard mode (up to 100kbits/s), fast mode (up to 400kbits/s) and fast mode plus (up to 1Mbits/s.) These lines are pulled up to a reference voltage via pull-up resistor. The device I²C detection thresholds support a communication reference voltage from 1.2V to 5V.

Due to the ultra low IQ when the device operates in low power mode, it is necessary ensure a minimum of 90μs between a START command and any subsequent START command on the I²C bus. The recommended minimum tbuf (bus free time between a STOP and START condition) depends on the I²C mode:

- Standard mode (100 kbits/s):
  - No additional requirements
- Fast mode (400 kbits/s):
  - Increase I²C t_{buf} to at least 68 μs
  - If using repeated start commands, ensure I²C tsu:STA is at least 68 μs
- Fast mode plus (1 Mbits/s):
  - Increase I²C t^{buf} to at least 81 μs
  - If using repeated start commands, ensure I²C tsu:STA is at least 81 μs

These recommendations assume a successful I²C transaction. It is also necessary to ensure a minimum 90μs time between two START commands in the case of a NACK.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

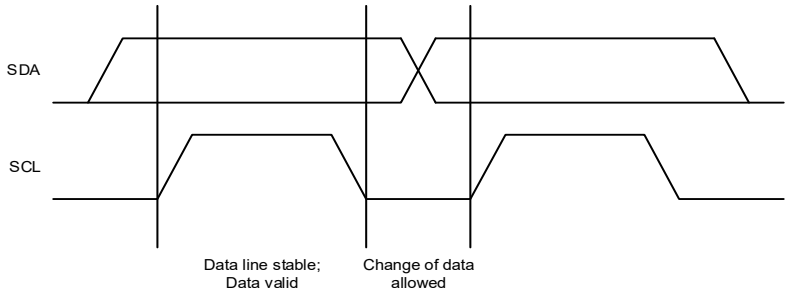


Figure 8. Bit Transfer on the I²C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

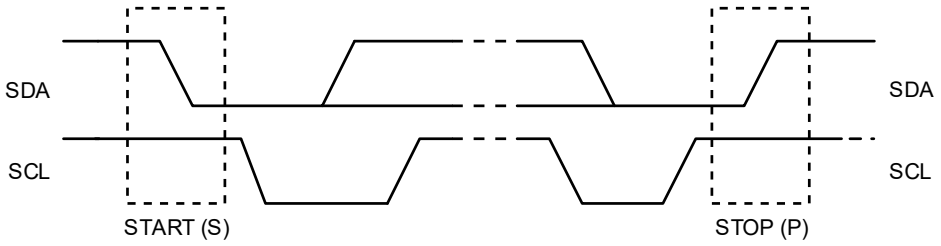


Figure9. TS START and STOP Conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the host into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and releases the SCL line.

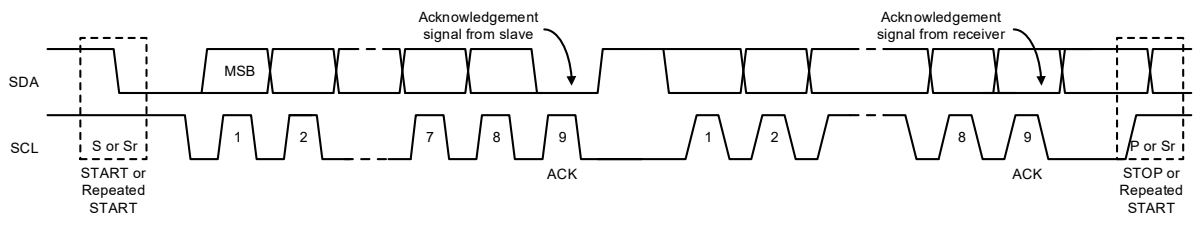


Figure10. Data Transfer on the I²C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after each transmitted byte. The ACK bit allows the target to signal the host that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the host.

The host releases the SDA line during the acknowledge clock pulse so the target can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The host can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).The device 7bit address is defined as 1101 011 (0x6B).

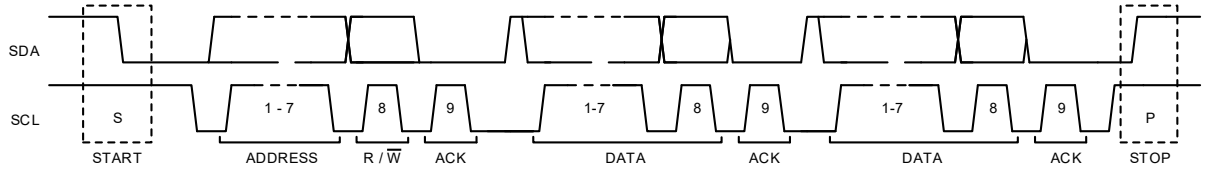


Figure11. Complete Data Transfer

Single Read and Write

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

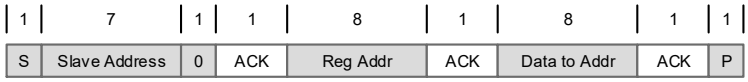


Figure12. Single Write

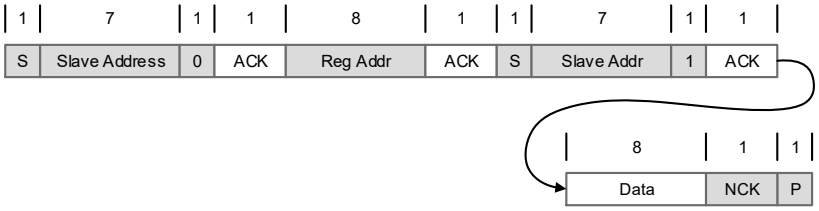


Figure13. Single Read

Multi-Read and Multi-Write

The charger device supports multi-byte read and multi-byte write of all registers. These multi-byte operations are allowed to cross register boundaries. For instance, the entire register map may be read in a single operation with a 39-byte read that starts at register address 0x01.

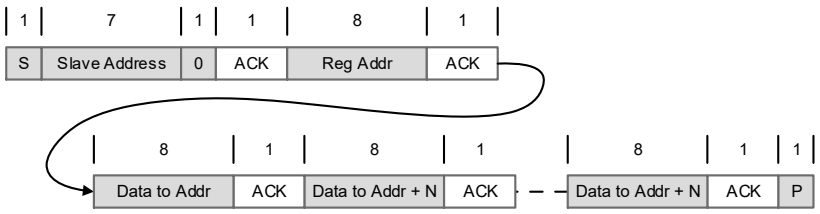


Figure14. Multi-Write

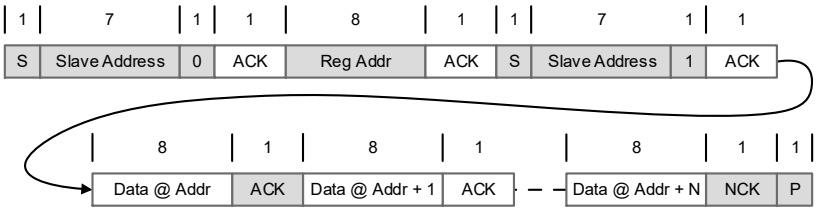


Figure15. Multi-Read

Register Maps

I²C Slave Address: 6BH (1101011B + R/W)

Register Programming

The ET95611CX contain 8bit and 16bit registers. When writing to 16bit registers, I²C transactions follow the little endian format, starting at the address of the least significant byte and writing both register bytes in a single 16bit transaction.

ET95611CX Registers

Table 6 lists the memory-mapped registers for the ET95611CX registers. All register offset addresses not listed in Table 6 should be considered as reserved locations and the register contents should not be modified.

Table 6. ET95611CX Registers

Address	Acronym	Register Name
2h	REG0x02_Charge_Current_Limit	Charge Current Limit
4h	REG0x04_Charge_Voltage_Limit	Charge Voltage Limit
6h	REG0x06_Input_Current_Limit	Input Current Limit
8h	REG0x08_Input_Voltage_Limit	Input Voltage Limit
Ah	REG0x0A_IOTG_regulation	IOTG regulation
Ch	REG0x0C_VOTG_regulation	VOTG regulation
Eh	REG0x0E_Minimal_System_Voltage	Minimal System Voltage
10h	REG0x10_Pre-charge_Control	Pre-charge Control
12h	REG0x12_Termination_Control	Termination Control
14h	REG0x14_Charge_Control_0	Charge Control 0
15h	REG0x15_Charge_Timer_Control	Charge Timer Control
16h	REG0x16_Charger_Control_1	Charger Control 1
17h	REG0x17_Charger_Control_2	Charger Control 2
18h	REG0x18_Charger_Control_3	Charger Control 3
19h	REG0x19_Charger_Control_4	Charger Control 4
1Ah	REG0x1A_NTC_Control_0	NTC Control 0
1Bh	REG0x1B_NTC_Control_1	NTC Control 1
1Ch	REG0x1C_NTC_Control_2	NTC Control 2
1Dh	REG0x1D_Charger_Status_0	Charger Status 0
1Eh	REG0x1E_Charger_Status_1	Charger Status 1
1Fh	REG0x1F_FAULT_Status_0	FAULT Status 0
20h	REG0x20_Charger_Flag_0	Charger Flag 0
21h	REG0x21_Charger_Flag_1	Charger Flag 1

Table 6. ET95611CX Registers(Continued)

Address	Acronym	Register Name
22h	REG0x22_FAULT_Flag_0	FAULT Flag 0
23h	REG0x23_Charger_Mask_0	Charger Mask 0
24h	REG0x24_Charger_Mask_1	Charger Mask 1
25h	REG0x25_FAULT_Mask_0	FAULT Mask 0
26h	REG0x26_ADC_Control	ADC Control
27h	REG0x26_ADC_Control	ADC Function Disable 0
28h	REG0x28_IBUS_ADC	IBUS ADC
2Ah	REG0x2A_IBAT_ADC	IBAT ADC
2Ch	REG0x2C_VBUS_ADC	VBUS ADC
2Eh	REG0x2E_VPMID_ADC	VPMID ADC
30h	REG0x30_VBAT_ADC	VBAT ADC
32h	REG0x32_VSYS_ADC	VSYS ADC
34h	REG0x34_TS_ADC	TS ADC
36h	REG0x36_TDIE_ADC	TDIE ADC
38h	REG0x38_Part_Information	Part Information

Complex bit access types are encoded to fit into small table cells. Table 7 shows the codes that are used for access types in this section.

Table 7. ET95611CX Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

REG0x02 (address = 02h) [reset = 0340h]

REG0x02 Charge_Current_Limit Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RESERVED				ICHG			
R-0h				R/W-Dh			
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ICHG		RESERVED					
R/W-Dh		R-0h					

REG0x02 Charge_Current_Limit Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved
11:6	ICHG	R/W	0Dh	Charge Current Regulation Limit: This 16bit register follows the little-endian convention. ICHG[5:2] falls in REG0x03[3:0], and ICHG[1:0] falls in REG0x02[7:6]. POR: 1040mA (0Dh) Range: 80mA-3040mA (01h-26h) Clamped Low Clamped High Bit Step: 80mA (01h) NOTE: When Q4_FULLON=1, this register has a minimum value of 160mA WATCHDOG Timer Expiration sets ICHG to 1/2 its previous value.
5:0	RESERVED	R	0h	Reserved

REG0x04 (address = 04h) [reset = 0D20h]

REG0x04 Charge_Voltage_Limit Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RESERVED				VREG			
R-0h				R/W-1A4h			
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
VREG					RESERVED		
R/W-1A4h					R-0h		

REG0x04 Charge_Voltage_Limit Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved
11:3	VREG	R/W	1A4h	Battery Voltage Regulation Limit: This 16bit register follows the little-endian convention. VREG[8:5] falls in REG0x05[3:0], and VREG[4:0] falls in REG0x04[7:3]. POR: 4200mV (1A4h) Range: 3840mV - 4800mV (180h-1E0h) Clamped Low Clamped High Bit Step: 10mV
2:0	RESERVED	R	0h	Reserved

REG0x06 (address = 06h) [reset = 0960h]

REG0x06 Input_Current_Limit Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RESERVED				IINDPM			
R-0h				R/W-A0h			
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IINDPM				RESERVED			
R/W-96h				R-0h			

REG0x06 Input_Current_Limit Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved
11:4	IINDPM	R/W	96h	Input Current Regulation Limit: This 16bit register follows the little-endian convention. IINDPM[7:4] falls in REG0x07[3:0], and IINDPM[3:0] falls in REG0x06[7:4]. ET95611CX: Based on D+/D- detection results: USB SDP = 500mA USB CDP = 1.5A USB DCP = 1.5A USB HVDCP = 1.5A Unknown Adapter = 500mA Non-Standard Adapter = 1A/2.1A/2.4A POR: 3000mA (A0h) Range: 100mA-3000mA (5h-96h) Clamped Low Clamped High Bit Step: 20mA When the adapter is removed, IINDPM is reset to its POR value of 3.0A.
3:0	RESERVED	R	0h	Reserved

REG0x08 (address = 08h) [reset = 0E60h]

REG0x08 Input_Voltage_Limit Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RESERVED		VINDPM					
R-0h		R/W-73h					
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
VINDPM			RESERVED				
R/W-73h			R-0h				

REG0x08 Input_Voltage_Limit Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0h	Reserved
13:5	VINDPM	R/W	73h	Absolute Input Voltage Regulation Limit: This 16bit register follows the little-endian convention. VINDPM[8:3] falls in REG0x09[5:0], and VINDPM[2:0] falls in REG0x08[7:5]. POR: 4600mV (73h) Range: 3800mV-13200mV (5Fh-14Ah) Clamped Low Clamped High Bit Step: 40mV
4:0	RESERVED	R	0h	Reserved

REG0x0A (address = 0Ah) [reset = 0320h]

REG0x0A IOTG_regulation Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RESERVED				IOTG			
R-0h				R/W-32h			
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IOTG				RESERVED			
R/W-32h				R-0h			

REG0x0A IOTG_regulation Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved
11:4	IOTG	R/W	32h	OTG mode current regulation limit: This 16bit register follows the little-endian convention. IOTG[7:4] falls in REG0x0B[3:0], and IOTG[3:0] falls in REG0x0A[7:4]. POR: 1000mA (32h) Range: 100mA-2100mA (5h-69h) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0h	Reserved

REG0x0C (address = 0Ch) [reset = 0FC0h]

REG0x0C VOTG_regulation Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RESERVED			VOTG				
R-0h			R/W-3Fh				
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
VOTG		RESERVED					
R/W-3Fh		R-0h					

REG0x0C VOTG_regulation Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0h	Reserved
12:6	VOTG	R/W	3Fh	OTG mode regulation voltage: This 16bit register follows the little-endian convention. VOTG[6:2] falls in REG0x0D[4:0], and VOTG[1:0] falls in REG0x0C[7:6]. POR: 5040mV (3Fh) Range: 3840mV- 9040mV (30h-71h) Clamped Low Clamped High Bit Step: 80mV
5:0	RESERVED	R	0h	Reserved

REG0x0E (address = 0Eh) [reset = 0B00h]

REG0x0E Minimal_System_Voltage Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RESERVED				VSYSMIN			
R-0h				R/W-2Ch			
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
VSYSMIN		RESERVED					
R/W-2Ch		R-0h					

REG0x0E Minimal_System_Voltage Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved
11:6	VSYSMIN	R/W	2Ch	Minimal System Voltage: This 16bit register follows the little-endian convention. VSYSMIN[5:2] falls in REG0x0F[3:0], and VSYSMIN[1:0] falls in REG0x0E[7:6]. POR: 3520mV (2Ch) Range: 2560mV-3840mV (20h-30h) Clamped Low Clamped High Bit Step: 80mV
5:0	RESERVED	R	0h	Reserved

REG0x10 (address = 10h) [reset = 0050h]

REG0x10 Pre-charge_Control Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RESERVED							IPRECHG
R-0h							R/W-5h
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IPRECHG				RESERVED			
R/W-5h				R-0h			

REG0x10 Pre-charge_Control Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R	0h	Reserved
8:4	IPRECHG	R/W	05h	Pre-charge current regulation limit: This 16bit register follows the little-endian convention. IPRECHG[4] falls in REG0x11[0], and IPRECHG[3:0] falls in REG0x10[7:4] POR: 100mA (05h) Range: 100mA - 620mA (05h-1Fh) Clamped Low Bit Step: 20mA (1h) NOTE: When Q4_FULLON=1, this register has a minimum value of 80mA
3:0	RESERVED	R	0h	Reserved

REG0x12 (address = 12h) [reset = 0050h]

REG0x12 Termination_Control Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RESERVED							ITERM
R-0h							R/W-0Ah
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ITERM					RESERVED		
R/W-0Ah					R-0h		

REG0x12 Termination_Control Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R	0h	Reserved
8:3	ITERM	R/W	0Ah	Termination Current Threshold: This 16bit register follows the little-endian convention. ITERM[5] falls in REG0x13[0], and ITERM[4:0] falls in REG0x12[7:3]. POR: 100mA (Ah) Range: 60mA - 620mA (6h-3Eh) Clamped Low Bit Step: 10mA (1h) NOTE: When Q4_FULLON=1, this register has a minimum value of 120mA, so Reset value becomes120mA in this case
2:0	RESERVED	R	0h	Reserved

REG0x14 (address = 14h) [reset = 06h]

REG0x14 Charge_Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Q1_FULLON	Q4_FULLON	ITRICKLE	TOPOFF_TMR		EN_TERM	VINDPM_BAT_TRACK	VRECHG
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-1h	R/W-1h	R/W-0h

REG0x14 Charge_Control Field Descriptions

Bit	Field	Type	Reset	Description
7	Q1_FULLON	R/W	0h	Forces RBFET (Q1) into low resistance state (30mΩ) , regardless of IINDPM setting. 0h = RBFET RDSON determined by IINDPM setting (default) 1h = RBFET RDSON is always 30mΩ
6	Q4_FULLON	R/W	0h	Forces BATFET (Q4) into low resistance state (20mΩ), regardless of ICHG setting. (Only applies when VBAT > VSYSMIN. Otherwise BATFET operates in linear mode.) 0h = BATFET RDSON determined by charge current (default) 1h = BATFET RDSON is always 20mΩ
5	ITRICKLE	R/W	0h	Trickle charging current setting: 0b = 17mA (default) 1b = 65mA
4:3	TOPOFF_TMR	R/W	0h	Top-off timer control: 0h = Disabled (default) 1h = 15mins 2h = 30mins 3h = 45mins
2	EN_TERM	R/W	1h	Enable termination 0h = Disable 1h = Enable (default)
1	VINDPM_BAT_TRACK	R/W	1h	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of the VINDPM register value and VBAT + VINDPM_BAT_TRACK. 0h = Disable function (VINDPM set by register) 1h = VBAT + 400mV (default)
0	VRECHG	R/W	0h	Battery Recharge Threshold Offset (Below VREG) 0h = 100mV (default) 1h = 200mV Note: Suggest set to 200mV(1h)

REG0x15 (address = 15h) [reset = 5Ch]

REG0x15 Charge_Timer_Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DIS_STAT	EN_AUTO_INDET	FORCE_INDET	EN_DCP_BIAS	TMR2X_EN	EN_SAFETY_TMRS	PRECHG_TMR	CHG_TMR
R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

REG0x15 Charge_Timer_Control Field Descriptions

Bit	Field	Type	Reset	Description
7	DIS_STAT	R/W	0h	Disable the STAT pin output 0h = Enable (default) 1h = Disable
6	EN_AUTO_INDET	R/W	1h	Automatic D+/D- Detection Enable 0h = Disable DPDM detection when VBUS is plugged-in 1h = Enable DPDM detection when VBUS is plugged-in (default)
5	FORCE_INDET	R/W	0h	Force D+/D- detection 0h = Do not force DPDM detection (default) 1h = Force DPDM algorithm, when DPDM detection is done, this bit is reset to 0
4	EN_DCP_BIAS	R/W	1h	Enable 600mV bias on D+ pin whenever DCP is detected by BC1.2 detection algorithm (VBUS_STAT = 011b.) 0h = Disable 600mV bias on D+ pin 1h = Enable 600mV bias on D+ pin if DCP detected
3	TMR2X_EN	R/W	1h	2X charging timer control 0h = Trickle charge, pre-charge and fast charge timer not slowed by 2X during input DPM or thermal regulation. 1h = Trickle charge, pre-charge and fast charge timer slowed by 2X during input DPM or thermal regulation (default)
2	EN_SAFETY_TMRS	R/W	1h	Enable fast charge, pre-charge and trickle charge timers 0h = Disable 1h = Enable (default)
1	PRECHG_TMR	R/W	0h	Pre-charge safety timer setting 0h = 2hrs (default) 1h = 0.5hrs

REG0x15 Charge_Timer_Control Field Descriptions(Continued)

Bit	Field	Type	Reset	Description
0	CHG_TMR	R/W	0h	Fast charge safety timer setting 0h = 12hrs (default) 1h = 24hrs

REG0x16 (address = 16h) [reset = A1h]

REG0x16 Charger_Control_1 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN_AUTO_IBATDIS	RESERVED	EN_CHG	EN_HIZ	FORCE_PMID_DIS	WD_RST	WATCHDOG	
R/W-1h	R-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	

REG0x16 Charger_Control_1 Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_AUTO_IBATDIS	R/W	1h	Enable the auto battery discharging during the battery OVP fault. 0h = The charger does NOT apply a discharging current on BAT during battery OVP triggered 1h = The charger does apply a discharging current on BAT during battery OVP triggered (default)
6	RESERVED	R	0h	Reserved
5	EN_CHG	R/W	1h	Charger enable configuration 0h = Charge Disable 1h = Charge Enable (default)
4	EN_HIZ	R/W	0h	Enable HIZ mode. 0h = Disable (default) 1h = Enable
3	RESERVED	R	0h	Reserved
2	WD_RST	R/W	0h	I^2C watch dog timer reset 0h = Normal (default) 1h = Reset (this bit goes back to 0 after timer reset)
1:0	WATCHDOG	R/W	1h	Watchdog timer setting 0h = Disable ; 1h = 50s (default); 2h = 100s ; 3h = 200s

REG0x17 (address = 17h) [reset = 4Fh]

REG0x17 Charger_Control_2 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REG_RST	TREG	SET_CONV_FREQ		SET_CONV_STRN		RESERVED	VBUS_OVP
R/W-0h	R/W-1h	R/W-0h		R/W-3h		R-0h	R/W-1h

REG0x17 Charger_Control_2 Field Descriptions

Bit	Field	Type	Reset	Description
7	REG_RST	R/W	0h	Reset registers to default values and reset timer Value resets to 0 after reset completes. 0b = Not reset (default) 1h = Reset
6	TREG	R/W	1h	Thermal regulation thresholds. 0h = 60°C 1h = 120°C (default)
5:4	SET_CONV_FREQ	R/W	0h	Adjust switching frequency of the converter 0h = Nominal, 1.1MHz (default) 1h = -10%, 0.99MHz 2h = +10%, 1.21MHz 3h = RESERVED
3:2	SET_CONV_STRN	R/W	3h	Adjust the high side and low side drive strength of the converter to adjust efficiency versus EMI. 0h = weak 1h = normal 2h = RESERVED 3h = strong
1	RESERVED	R	0h	Reserved
0	VBUS_OVP	R/W	1h	Sets VBUS over-voltage protection threshold 0h = 6.4V 1h = 13V

REG0x18 (address = 18h) [reset = 04h]

REG0x18 Charger_Control_3 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED	EN_OTG	PFM_OTG_DIS	PFM_FWD_DIS	BATFET_CTRL_WVBUS	BATFET_DLY	BATFET_CTRL	
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	

REG0x18 Charger_Control_3 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	EN_OTG	R/W	0h	OTG mode control 0b = OTG Disable (default) 1b = OTG Enable
5	PFM_OTG_DIS	R/W	0h	Disable PFM in OTG boost mode 0h = Enable (Default) 1h = Disable
4	PFM_FWD_DIS	R/W	0h	Disable PFM in forward buck mode 0h = Enable (Default) 1h = Disable
3	BATFET_CTRL_WVBUS	R/W	0h	Optionally allows BATFET off or system power reset with adapter present. 0h = Allow BATFET off or system power reset only if VBUS < VVBUS_UVLO. (default) 1h = Allow BATFET off or system power reset whether or not VBUS < VVBUS_UVLO.
2	BATFET_DLY	R/W	1h	Delay time added to the taking action in bits [1:0] of the BATFET_CTRL 0h = Add 20ms delay time 1h = Add 10s delay time (default)
1:0	BATFET_CTRL	R/W	0h	BATFET control The control logic of the BATFET to force the device enter different modes. 0h = Normal (default) 1h = Shutdown Mode 2h = Ship Mode 3h = System Power Reset

REG0x19 (address = 19h) [reset = C0h]

REG0x19 Charger_Control_4 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IBAT_PK		VBAT_UVLO	VBAT_OTG_MIN	EN_9V	RESERVED	CHG_RATE	
R/W-3h		R/W-0h	R/W-0h	R/W-0h	R	R/W-0h	

REG0x19 Charger_Control_4 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	IBAT_PK	R/W	3h	Battery discharging peak current protection threshold setting 0h = RESERVED 1h = RESERVED 2h = 6A 3h = 12A (default)
5	VBAT_UVLO	R/W	0h	Select the VBAT_UVLO falling threshold and VBAT_SHORT threshold 0h = VBAT_UVLO 2.2V, VBAT_SHORT 2.05V (default) 1h = VBAT_UVLO 1.8V, VBAT_SHORT 1.85V
4	VBAT_OTG_MIN	R/W	0h	Select the minimal battery voltage to start the OTG mode 0h = 3V rising / 2.8V falling (default) 1h = 2.6V rising / 2.4V falling
3	EN_9V	R/W	0h	Enable 9V adapter detection 0b = Disabled (default) 1b = Enabled
2	RESERVED	R	0h	Reserved
1:0	CHG_RATE	R/W	0h	The charge rate definition for the fast charge stage. The charging current fold back value is equal to ICHG register setting times the fold back ratio, then divided by the charge rate. 0h = 1C (default) , 1h = 2C 2h = 4C , 3h = 6C

REG0x1A (address = 1Ah) [reset = 3Dh]

REG0x1A NTC_Control_0 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TS_IGNORE	TS_TH_OTG_HOT		TS_TH_OTG_COLD	TS_ISET_WARM		TS_ISET_COOL	
R/W-0h	R/W-1h		R/W-1h	R/W-3h		R/W-1h	

REG0x1A NTC_Control_0 Field Descriptions

Bit	Field	Type	Reset	Description
7	TS_IGNORE	R/W	0h	Ignore the TS feedback: the charger considers the TS is always good to allow charging and OTG modes, TS_STAT reports TS_NORMAL condition. 0h = Not ignore (Default) 1h = Ignore
6:5	TS_TH_OTG_HOT	R/W	1h	OTG Mode TS_HOT rising temperature threshold to transition from normal operation into suspended OTG mode when a 103AT NTC thermistor is used, RT1=5.23kΩ and RT2=30.1kΩ. 0h = 55°C 1h = 60°C (default) 2h = 65°C 3h = Disable
4	TS_TH_OTG_COLD	R/W	1h	OTG Mode TS_COLD falling temperature threshold to transition from normal operation into suspended OTG mode when a 103AT NTC thermistor is used, RT1=5.23kΩ and RT2=30.1kΩ. 0h = -20°C 1h = -10°C (default)
3:2	TS_ISET_WARM	R/W	3h	TS_WARM Current Setting 0h = Charge Suspend 1h = Set ICHG to 20% 2h = Set ICHG to 40% 3h = ICHG unchanged (default)
1:0	TS_ISET_COOL	R/W	1h	TS_COOL Current Setting 0h = Charge Suspend 1h = Set ICHG to 20% (default) 2h = Set ICHG to 40% 3h = ICHG unchanged

REG0x1B (address = 1Bh) [reset = 25h]

REG0x1B NTC_Control_1 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TS_TH1_TH2_TH3			TS_TH4_TH5_TH6			TS_VSET_WARM	
R/W-1h			R/W-1h			R/W-1h	

REG0x1B NTC_Control_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	TS_TH1_TH2_TH3	R/W	1h	TH1, TH2 and TH3 comparator falling temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ. 0h = TH1 is 0°C, TH2 is 5°C, TH3 is 15°C 1h = TH1 is 0°C, TH2 is 10°C, TH3 is 15°C (default) 2h = TH1 is 0°C, TH2 is 15°C, TH3 is 20°C 3h = TH1 is 0°C, TH2 is 20°C, TH3 20°C 4h = TH1 is -5°C, TH2 is 5°C, TH3 is 15°C 5h = TH1 is -5°C, TH2 is 10°C, TH3 is 15°C 6h = TH1 is -5°C, TH2 is 10°C, TH3 is 20°C 7h = TH1 is 0°C, TH2 is 10°C, TH3 is 20°C
4:2	TS_TH4_TH5_TH6	R/W	1h	TH4, TH5 and TH6 comparator rising temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ. 0h = TH4 is 35°C, TH5 is 40°C, TH6 is 60°C 1h = TH4 is 35°C, TH5 is 45°C, TH6 is 60°C (default) 2h = TH4 is 35°C, TH5 is 50°C, TH6 is 60°C 3h = TH4 is 40°C, TH5 is 55°C, TH6 is 60°C 4h = TH4 is 35°C, TH5 is 40°C, TH6 is 50°C 5h = TH4 is 35°C, TH5 is 45°C, TH6 is 50°C 6h = TH4 is 40°C, TH5 is 45°C, TH6 is 60°C 7h = TH4 is 40°C, TH5 is 50°C, TH6 is 60°C
1:0	TS_VSET_WARM	R/W	1h	TS_WARM Voltage Setting 0h = Set VREG to VREG-300mV 1h = Set VREG to VREG-200mV (default) 2h = Set VREG to VREG-100mV 3h = VREG unchanged

REG0x1C (address = 1Ch) [reset = 3Fh]

REG0x1C NTC_Control_2 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED	TS_VSET_SYM	TS_VSET_PREWARM		TS_ISET_PREWARM		TS_ISET_PRECOOL	
R-0h	R/W-0h	R/W-3h		R/W-3h		R/W-3h	

REG0x1C NTC_Control_2 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	TS_VSET_SYM	R/W	0h	When this bit is set to 0, the voltage regulation for TS_PRECOOL and TS_COOL is unchanged. When this bit is set to 1, TS_PRECOOL uses the TS_VSET_PREWARM setting of TS_PREWARM and TS_COOL uses the TS_VSET_WARM setting of TS_WARM . 0h = VREG unchanged (default) 1h = TS_COOLx matches TS_WARMx
5:4	TS_VSET_ PREWARM	R/W	3h	Advanced temperature profile voltage setting for TS_PREWARM (TH4 - TH5) 0h = Set VREG to VREG-300mV 1h = Set VREG to VREG-200mV 2h = Set VREG to VREG-100mV 3h = VREG unchanged (default)
3:2	TS_ISET_ PREWARM	R/W	3h	Advanced temperature profile current setting for TS_PREWARM zone(TH4 - TH5) 0h = Charge Suspend 1h = Set ICHG to 20% 2h = Set ICHG to 40% 3h = ICHG unchanged (default)
1:0	TS_ISET_PRECOOL	R/W	3h	Advanced temperature profile current setting for TS_PRECOOL zone (TH2 - TH3) 0h = Charge Suspend 1h = Set ICHG to 20% 2h = Set ICHG to 40% 3h = ICHG unchanged (default)

REG0x1D (address = 1Dh) [reset = 00h]

REG0x1D Charger_Status_0 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED	ADC_DONE_STAT	TREG_STAT	VSYS_STAT	IINDPM_STAT	VINDPM_STAT	SAFETY_TMR_STAT	WD_STAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

REG0x1D Charger_Status_0 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	ADC_DONE_STAT	R	0h	ADC Conversion Status (in one-shot mode only) Note: Always reads 0 in continuous mode 0h = Conversion not complete 1h = Conversion complete
5	TREG_STAT	R	0h	IC Thermal regulation status 0h = Normal 1h = Device in thermal regulation
4	VSYS_STAT	R	0h	VSYS Regulation Status (forward mode) 0h = Not in VSYSMIN regulation (BAT>VSYSMIN) 1h = In VSYSMIN regulation (BAT<VSYSMIN)
3	IINDPM_STAT	R	0h	In forward mode, indicates that either IINDPM regulation is active In OTG mode, indicates that IOTG regulation is active 0h = Normal 1h = In IINDPM regulation or IOTG regulation
2	VINDPM_STAT	R	0h	VINDPM status (forward mode) or VOTG status (OTG mode, backup mode) 0h = Normal 1h = In VINDPM regulation or VOTG regulation
1	SAFETY_TMR_STAT	R	0h	Fast charge, trickle charge and pre-charge timer status 0h = Normal 1h = Safety timer expired
0	WD_STAT	R	0h	I^2C watch dog timer status 0h = Normal 1h = WD timer expired

REG0x1E (address = 1Eh) [reset = 00h]

REG0x1E Charger_Status_1 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED			CHG_STAT		VBUS_STAT		
R-0h			R-0h		R-0h		

REG0x1E Charger_Status_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4:3	CHG_STAT	R	0h	Charge Status bits 0h = Not Charging or Charge Terminated 1h = Trickle Charge, Pre-charge or Fast charge (CC mode) 2h = Taper Charge (CV mode) 3h = Top-off Timer Active Charging
2:0	VBUS_STAT	R	0h	VBUS status bits: 000b = No qualified adapter, or EN_AUTO_INDET = 0. 001b = USB SDP Adapter (500mA) 010b = USB CDP Adapter (1.5A) 011b = USB DCP Adapter (1.5A) 100b = Unknown Adapter (500mA) 101b = Non-Standard Adapter (1A/2.1A/2.4A) 110b = HVDCP adapter (1.5A) 111b = In boost OTG mode

REG0x1F (address = 1Fh) [reset = 00h]

REG0x1F FAULT_Status_0 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VBUS_FAULT_STAT	BAT_FAULT_STAT	SYS_FAULT_STAT	OTG_FAULT_STAT	TSHUT_STAT	TS_STAT		
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		

REG0x1F FAULT_Status_0 Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FAULT_STAT	R	0h	VBUS fault status, VBUS OVP and sleep comparator 0h = Normal 1h = Device not switching due to over voltage protection or sleep comparator
6	BAT_FAULT_STAT	R	0h	BAT fault status, IBAT OCP and VBAT OVP 0h = Normal 1h = Device in battery over current protection or battery over-voltage protection
5	SYS_FAULT_STAT	R	0h	VSYS under voltage and over voltage status 0h = Normal 1h = SYS in SYS short circuit or over voltage
4	OTG_FAULT_STAT	R	0h	Reverse-current or under-voltage or over-voltage fault detected at PMID or VBUS during boost OTG 0h = Normal 1h = Reverse-current fault or PMID or VBUS in over voltage or under voltage during OTG
3	TSHUT_STAT	R	0h	IC temperature shutdown status 0h = Normal 1h = Device in thermal shutdown protection
2:0	TS_STAT	R	0h	The TS temperature zone. 0h = TS_NORMAL 1h = TS_COLD or TS_OTG_COLD or TS resistor string power rail is not available. 2h = TS_HOT or TS_OTG_HOT 3h = TS_COOL 4h = TS_WARM 5h = TS_PRECOOL 6h = TS_PREWARM 7h = TS pin bias reference fault

REG0x20 (address = 20h) [reset = 00h]

REG0x20 Charger_Flag_0 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED	ADC_DONE _FLAG	TREG_FLAG	VSYS_FLAG	IINDPM _FLAG	VINDPM _FLAG	SAFETY_TM R_FLA G	WD_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

REG0x20 Charger_Flag_0 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	ADC_DONE_FLAG	R	0h	ADC conversion flag (only in one-shot mode) 0h = Conversion not completed 1h = Conversion completed
5	TREG_FLAG	R	0h	IC Thermal regulation flag 0h = Normal 1h = TREG signal rising threshold detected
4	VSYS_FLAG	R	0h	VSYS min regulation flag 0h = Normal 1h = Entered or existed VSYS min regulation
3	IINDPM_FLAG	R	0h	Indicates that either the IINDPM regulation loop, ILIM pin regulation or IOTG regulation loop has been entered. 0h = Normal 1h = IINDPM, ILIM or IOTG regulation signal rising edge detected
2	VINDPM_FLAG	R	0h	VINDPM or VOTG flag 0h = Normal 1h = VINDPM or VOTG regulation signal rising edge detected
1	SAFETY_TMR_FLA G	R	0h	VINDPM or VOTG flag 0h = Normal 1h = VINDPM or VOTG regulation signal rising edge detected
0	WD_FLAG	R	0h	I^2C watchdog timer flag 0h = Normal 1h = WD timer signal rising edge detected

REG0x21 (address = 21h) [reset = 00h]

REG0x21 Charger_Flag_1 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED				CHG_FLAG	RESERVED		VBUS_FLAG
R-0h				R-0h	R-0h		R-0h

REG0x21 Charger_Flag_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	CHG_FLAG	R	0h	Charge status flag 0h = Normal 1h = Charge status changed
2:1	RESERVED	R	0h	Reserved
0	VBUS_FLAG	R	0h	VBUS status flag 0h = Normal 1h = VBUS status changed

REG0x22 (address = 22h) [reset = 00h]

REG0x22 FAULT_Flag_0 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VBUS_FAULT_FLAG	BAT_FAULT_FLAG	SYS_FAULT_FLAG	OTG_FAULT_FLAG	TSHUT_FLAG	RESERVED		TS_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		R-0h

REG0x22 FAULT_Flag_0 Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FAULT_FLAG	R	0h	VBUS over-voltage or sleep flag 0h = Normal 1h = Entered VBUS OVP or sleep
6	BAT_FAULT_FLAG	R	0h	IBAT over-current and VBAT over-voltage flag 0h = Normal 1h = Entered battery discharged OCP or VBAT OVP
5	SYS_FAULT_FLAG	R	0h	VSYS over voltage and SYS short flag 0h = Normal 1h = Stopped switching due to system over-voltage or SYS short fault
4	OTG_FAULT_FLAG	R	0h	OTG PMID and VBUS reverse-current, under voltage and over voltage flag 0h = Normal 1h = Stopped OTG due to reverse-current fault, PMID under voltage or over voltage fault

REG0x22 FAULT_Flag_0 Field Descriptions(Continued)

Bit	Field	Type	Reset	Description
3	TSHUT_FLAG	R	0h	IC thermal shutdown flag 0h = Normal 1h = TS shutdown signal rising threshold detected
2	RESERVED	R	0h	Reserved
1	TS_FLAG	R	0h	TS status flag 0h = Normal 1h = A change to TS status was detected

REG0x23 (address = 23h) [reset = 00h]

REG0x23 Charger_Mask_0 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED	ADC_DONE_MASK	TREG_MASK	VSYS_MASK	IINDPM_MASK	VINDPM_MASK	SAFETY_TMR_MASK	WD_MASK
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

REG0x23 Charger_Mask_0 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	ADC_DONE_MASK	R/W	0h	ADC conversion mask flag (only in one-shot mode) 0h = ADC conversion done does produce INT pulse 1h = ADC conversion done does not produce INT pulse
5	TREG_MASK	R/W	0h	IC thermal regulation mask flag 0h = Entering TREG does produce INT 1h = Entering TREG does not produce INT
4	VSYS_MASK	R/W	0h	VSYS min regulation mask flag 0h = Enter or exit VSYSMIN regulation does produce INT pulse 1h = Enter or exit VSYSMIN regulation does not produce INT pulse
3	IINDPM_MASK	R/W	0h	IINDPM, ILIM or IOTG mask 0h = Enter IINDPM, ILIM or IOTG does produce INT pulse 1h = Enter IINDPM, ILIM or IOTG does not produce INT pulse

REG0x23 Charger_Mask_0 Field Descriptions(Continued)

Bit	Field	Type	Reset	Description
2	VINDPM_MASK	R/W	0h	VINDPM or VOTG mask 0h = Enter VINDPM or VOTG does produce INT pulse 1h = Enter VINDPM or VOTG does not produce INT pulse
1	SAFETY_TMR_MASK	R/W	0h	Fast charge, trickle charge and pre-charge timer mask flag 0h = Fast charge, trickle charge or pre-charge timer expiration does produce INT 0h = Fast charge, trickle charge or pre-charge timer expiration does not produce INT
0	WD_MASK	R/W	0h	I^2C watch dog timer mask 0h = I^2C watch dog timer expired does produce INT pulse 1h = I^2C watch dog timer expired does not produce INT pulse

REG0x24 (address = 24h) [reset = 00h]

REG0x24 Charger_Mask_1 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED				CHG_MASK	RESERVED		VBUS_MASK
R-0h				R/W-0h	R-0h		R/W-0h

REG0x24 Charger_Mask_1 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	CHG_MASK	R/W	0h	Charge status mask flag 0h = Charging status change does produce INT 1h = Charging status change does not produce INT
2:1	RESERVED	R	0h	Reserved
0	VBUS_MASK	R/W	0h	VBUS status mask flag 0h = VBUS status change does produce INT 1h = VBUS status change does not produce INT

REG0x25 (address = 25h) [reset = 00h]

REG0x25 FAULT_Mask_0 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VBUS_FAULT_MASK	BAT_FAULT_MASK	SYS_FAULT_MASK	OTG_FAULT_MASK	TSHUT_MASK	RESERVED		TS_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h

REG0x25 FAULT_Mask_0 Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FAULT_MASK	R/W	0h	VBUS over-voltage and sleep comparator mask flag 0h = Entering VBUS OVP or sleep does produce INT 1h = Entering VBUS OVP or sleep does not produce INT
6	BAT_FAULT_MASK	R/W	0h	IBAT over current and VBAT overvoltage mask flag 0h = IBAT OCP fault or VBAT OVP fault does produce INT 1h = Neither IBAT OCP fault nor VBAT OVP fault produces INT
5	SYS_FAULT_MASK	R/W	0h	SYS over voltage and SYS short mask 0h = System over-voltage or SYS short fault does produce INT 1h = Neither system over voltage nor SYS short fault produces INT
4	OTG_FAULT_MASK	R/W	0h	OTG VBUS and PMID reverse-current, under voltage and over voltage mask 0h = OTG VBUS or PMID reverse-current, under voltage fault or over voltage fault does produce INT 1h = Neither reverse-current fault, OTG PMID or VBUS under voltage nor over voltage fault produces INT
3	TSHUT_MASK	R/W	0h	IC thermal shutdown mask flag 0h = TSHUT does produce INT 1h = TSHUT does not produce INT
2:1	RESERVED	R	0h	Reserved
0	TS_MASK	R/W	0h	Temperature charging profile interrupt mask 0h = A change to TS temperature zone does produce INT 1h = A change to the TS temperature zone does not produce INT

REG0x26 (address = 26h) [reset = 30h]

REG0x26 ADC_Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_EN	ADC_RATE	ADC_SAMPLE		RESERVED	RESERVED	RESERVED	
R/W-0h	R/W-0h	R/W-3h		R-0h	R-0h	R-0h	

REG0x26 ADC_Control Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC_EN	R/W	0h	ADC Control The registers POR to all 0s, then after that always retain the last measurement, and never clear. 0h = Disable (default) 1h = Enable
6	ADC_RATE	R/W	0h	ADC conversion rate control 0h = Continuous conversion (default) 1h = One shot conversion
5:4	ADC_SAMPLE	R/W	3h	ADC sample speed 0h = 11bit effective resolution 1h = 12bit effective resolution 2h = 13bit effective resolution 3h = 14bit effective resolution (default)
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1:0	RESERVED	R	0h	Reserved

REG0x27 (address = 27h) [reset = 00h]

REG0x27 ADC_Function_Disable_0 Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IBUS_ADC_DIS	IBAT_ADC_DIS	VBUS_ADC_DIS	VBAT_ADC_DIS	VSYS_ADC_DIS	TS_ADC_DIS	TDIE_ADC_DIS	VPMID_ADC_DIS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

REG0x27 ADC_Function_Disable_0 Field Descriptions

Bit	Field	Type	Reset	Description
7	IBUS_ADC_DIS	R/W	0h	IBUS ADC control 0h = Enable (Default) 1h = Disable
6	IBAT_ADC_DIS	R/W	0h	IBAT ADC control 0h = Enable (Default) 1h = Disable
5	VBUS_ADC_DIS	R/W	0h	VBUS ADC control 0h = Enable (Default) 1h = Disable
4	VBAT_ADC_DIS	R/W	0h	VBAT ADC control 0h = Enable (Default) 1h = Disable
3	VSYS_ADC_DIS	R/W	0h	VSYS ADC control 0h = Enable (Default) 1h = Disable
2	TS_ADC_DIS	R/W	0h	TS ADC control 0h = Enable (Default) 1h = Disable
1	TDIE_ADC_DIS	R/W	0h	TDIE ADC control 0h = Enable (Default) 1h = Disable
0	VPMID_ADC_DIS	R/W	0h	VPMID ADC control 0h = Enable (Default) 1h = Disable

REG0x28 (address = 28h) [reset = 0000h]

REG0x28 IBUS_ADC Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
IBUS_ADC							
R-0h							
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IBUS_ADC						RESERVED	
R-0h						R-0h	

REG0x28 IBUS_ADC Field Descriptions

Bit	Field	Type	Reset	Description
15:2	IBUS_ADC	R	0h	IBUS ADC reading Reported in 2s Complement. When the current is flowing from VBUS to PMID, IBUS ADC reports positive value, and when the current is flowing from PMID to VBUS, IBUS ADC reports negative value. POR: 0mA (0h) Format: 2s Complement Range: -4000mA-4000mA Clamped Low Clamped High Bit Step: 1mA
1:0	RESERVED	R	0h	Reserved

REG0x2A (address = 2Ah) [reset = 0000h]

REG0x2A IBAT_ADC Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
IBAT_ADC							
R-0h							
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IBAT_ADC						RESERVED	
R-0h						R-0h	

REG0x2A IBAT_ADC Field Descriptions

Bit	Field	Type	Reset	Description
15:2	IBAT_ADC	R	0h	IBAT ADC reading Reported in 2s Complement. The IBAT ADC reports positive value for the battery charging current, and negative value for the battery discharging current. The IBAT ADC resets to zero when EN_CHG=0. POR: 0mA (0h) Format: 2s Complement Range: -7500mA-3000mA Clamped Low Clamped High Bit Step: 2mA The IBAT ADC current can only be positive or zero in forward mode, and negative or zero in battery-only mode. If polarity of battery current changes from charging to discharging or vice-versa during the ADC measurement.
1:0	RESERVED	R	0h	Reserved

REG0x2C (address = 2Ch) [reset = 0000h]

REG0x2C VBUS_ADC Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
VBUS_ADC							
R-0h							
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
VBUS_ADC						RESERVED	
R-0h						R-0h	

REG0x2C VBUS_ADC Field Descriptions

Bit	Field	Type	Reset	Description
15:2	VBUS_ADC	R	0h	VBUS ADC reading POR: 0mV (0h) Format:2s Complement Range: 0mV-10000mV Clamped High Bit Step: 3.00mV
1:0	RESERVED	R	0h	Reserved

REG0x2E (address = 2Eh) [reset = 0000h]

REG0x2E VPMID_ADC Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
VPMID_ADC							
R-0h							
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
VPMID_ADC						RESERVED	
R-0h						R-0h	

REG0x2E VPMID_ADC Field Descriptions

Bit	Field	Type	Reset	Description
15:2	VPMID_ADC	R	0h	VPMID ADC reading POR: 0mV (0h) Format:2s Complement Range: 0mV-10000mV Clamped High Bit Step: 3.00mV
1:0	RESERVED	R	0h	Reserved

REG0x30 (address = 30h) [reset = 0000h]

REG0x30 VBAT_ADC Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
VBAT_ADC							
R-0h							
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
VBAT_ADC						RESERVED	
R-0h						R-0h	

REG0x30 VBAT_ADC Field Descriptions

Bit	Field	Type	Reset	Description
15:2	VBAT_ADC	R	0h	VBAT ADC reading POR: 0mV (0h) Format:2s Complement Range: 0mV-5572mV Clamped High Bit Step: 1mV
1:0	RESERVED	R	0h	Reserved

REG0x32 (address = 32h) [reset = 0000h]

REG0x32 VSYS_ADC Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
VSYS_ADC							
R-0h							
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
VSYS_ADC						RESERVED	
R-0h						R-0h	

REG0x32 VSYS_ADC Field Descriptions

Bit	Field	Type	Reset	Description
15:2	VSYS_ADC	R	0h	VSYS ADC reading POR: 0mV (0h) Format:2s Complement Range: 0mV-5572mV Clamped High Bit Step: 1mV
1:0	RESERVED	R	0h	Reserved

REG0x34 (address = 34h) [reset = 0000h]

REG0x34 TS_ADC Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RESERVED						TS_ADC	
R-0h						R-0h	
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
TS_ADC							
R-0h							

REG0x34 TS_ADC Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R	0h	Reserved
9:0	TS_ADC	R	0h	TS ADC reading as TS pin voltage in percentage of bias reference. Valid with TS pin bias reference active. POR: 0%(0h) Range: 0% - 100% (0h-3FFh) Clamped High Bit Step: 0.097656%

REG0x36 (address = 36h) [reset = 0000h]

REG0x36 TDIE_ADC Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
TDIE_ADC							
R-0h							
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
TDIE_ADC			RESERVED				
R-0h			R-0h				

REG0x36 TDIE_ADC Field Descriptions

Bit	Field	Type	Reset	Description
15:5	TDIE_ADC	R	0h	TDIE ADC reading Reported in 2s Complement. POR: 0°C(0h) Format: 2s Complement Range: -40°C - 140°C (FB0h-118h) Clamped Low Clamped High Bit Step: 0.5°C
4:0	RESERVED	R	0h	Reserved

REG0x38 (address = 38h) [reset = 02h]

REG0x38 Part_Information Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RESERVED		PN			DEV_REV		
R-0h		R-0h			R-2h		

REG0x38 Part_Information Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:3	PN	R	0h	Device Part number All the other options are reserved ET95611CX
2:0	DEV_REV	R	2h	Device Revision

Application and Implementation

Application Information

A typical application consists of the device configured as an I²C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphone and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

Typical Application Circuit

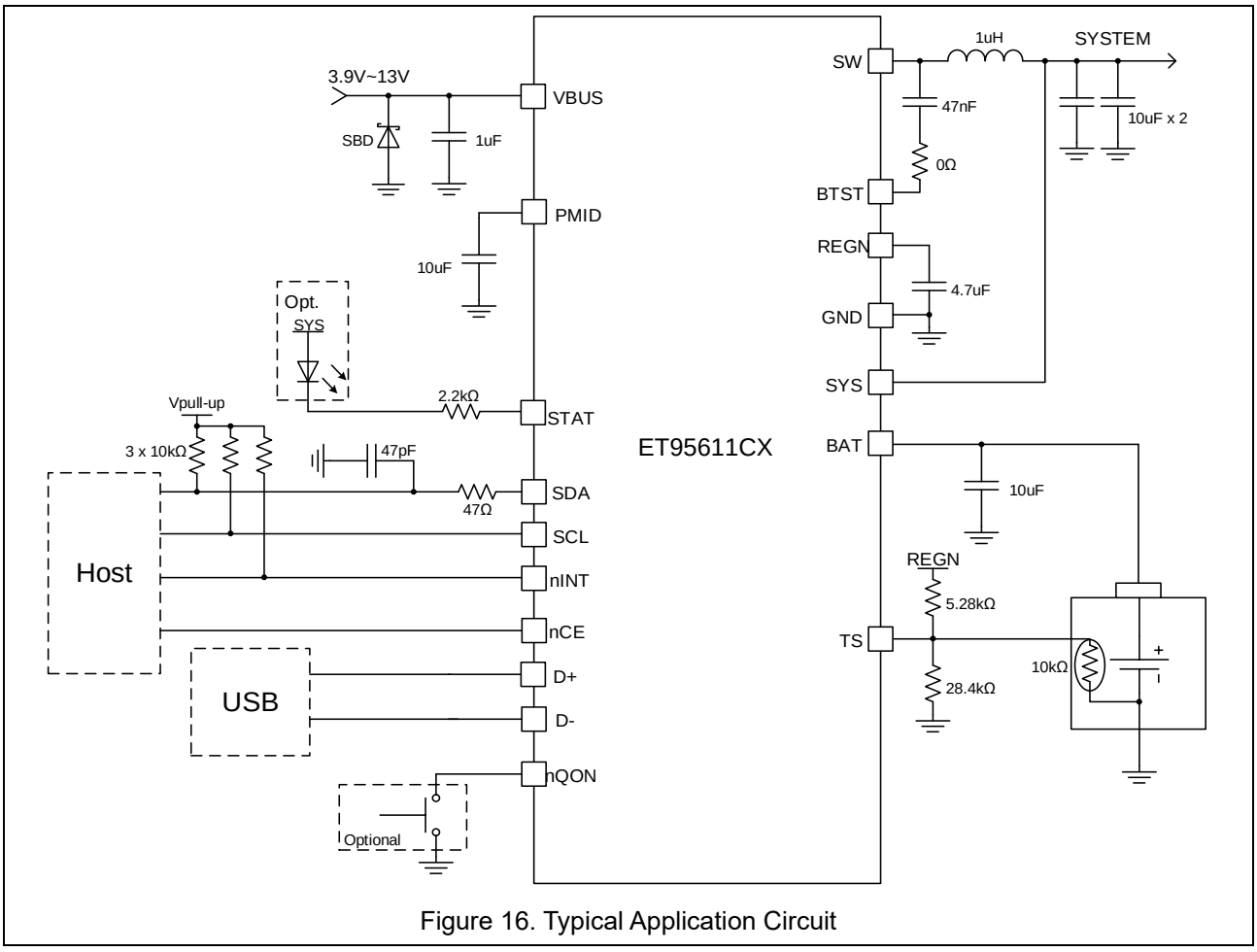


Figure 16. Typical Application Circuit

Design Requirements

Table8. Design Requirement

PARAMETER	VALUE
VBUS range	3.9V - 13V
Input current limit	3000mA
Fast charge current	3000mA
Minimum system voltage	3520mV
Battery regulation voltage	4200mV

Design Requirements

Inductor Selection

The 1.1MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2) \times I_{RIPPLE}$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{fs \times L}$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

Input Capacitor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current IC in occurs where the duty cycle is closest to 50% and can be estimated using:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)}$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25V or higher capacitor is preferred for 15V input voltage. Capacitance of 10μF is suggested for typical of 3A charging current.

Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. The formula shows the output capacitor RMS current I_{COUT} calculation:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}}$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_{SYS} = \frac{\Delta V_{SYS}}{8 L C_{SYS} f^2_{SW}} \left(1 - \frac{V_{SYS}}{V_{BUS}}\right)$$

At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensation optimized for ≥10μF ceramic output capacitance. The preferred ceramic capacitor is 10V rating, X7R or X5R.

Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9V and 13.0V input with at least 100mA current rating connected to VBUS or a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT.

Layout

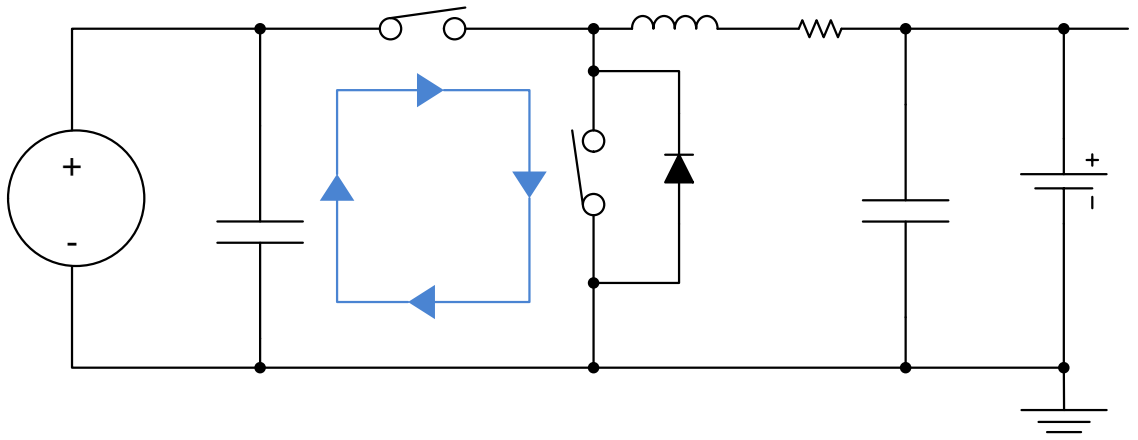
Layout Guidelines

The switching node rise and fall times should be minimized for lowest switching loss. Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. For lowest switching noise during forward/charge mode, place the decoupling capacitor CPMID1 and then bulk capacitor CPMID2 positive terminals as close as possible to PMID pin. Place the capacitor ground terminal close to the GND pin using the shortest copper trace connection or GND plane on the same layer as the IC.
2. For lowest switching noise during reverse/OTG mode, place the CSYS1 and CSYS2 output capacitors' positive terminals near the SYS pin. The capacitors' ground terminals must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC.
3. Since REGN powers the internal gate drivers, place the CREGN capacitor positive terminal close to REGN pin to minimize switching noise. The capacitor's ground terminal must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC.
4. Place the CVBUS and CBAT capacitors positive terminals as close to the VBUS and BAT pins as possible. The capacitors' ground terminals must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC.
5. Place the inductor input pin near the positive terminal of the SYS pin capacitors. Due to the PMID capacitor placement requirements, the inductor's switching node terminal must be via'd down with multiple via's to a second internal layer with a wide trace that returns to the SW pin with multiple vias. Using multiple vias ensures that the via's additional resistance is negligible compared to the inductor's dc resistance and therefore does not impact efficiency. The vias additional series inductance is negligible compared to the inductor's inductance.
6. Place the BTST capacitor on the opposite side from the IC using vias to connect to the BTST pin and SW node.
7. A separate analog GND plane for non-power related resistors and capacitors is not required if those components are placed away from the power components traces and planes.
8. Ensure that the I2C SDA and SCL lines are routed away from the SW node.

Additionally, it is important that the PCB footprint and solder mask for the ET95611CX cover the entire length of each of the pins. GND, SW, PMID, SYS and BAT pins extend further into the package than the other pins. Using the entire length of these pins reduces parasitic resistance and increases thermal conductivity from the package into the board.

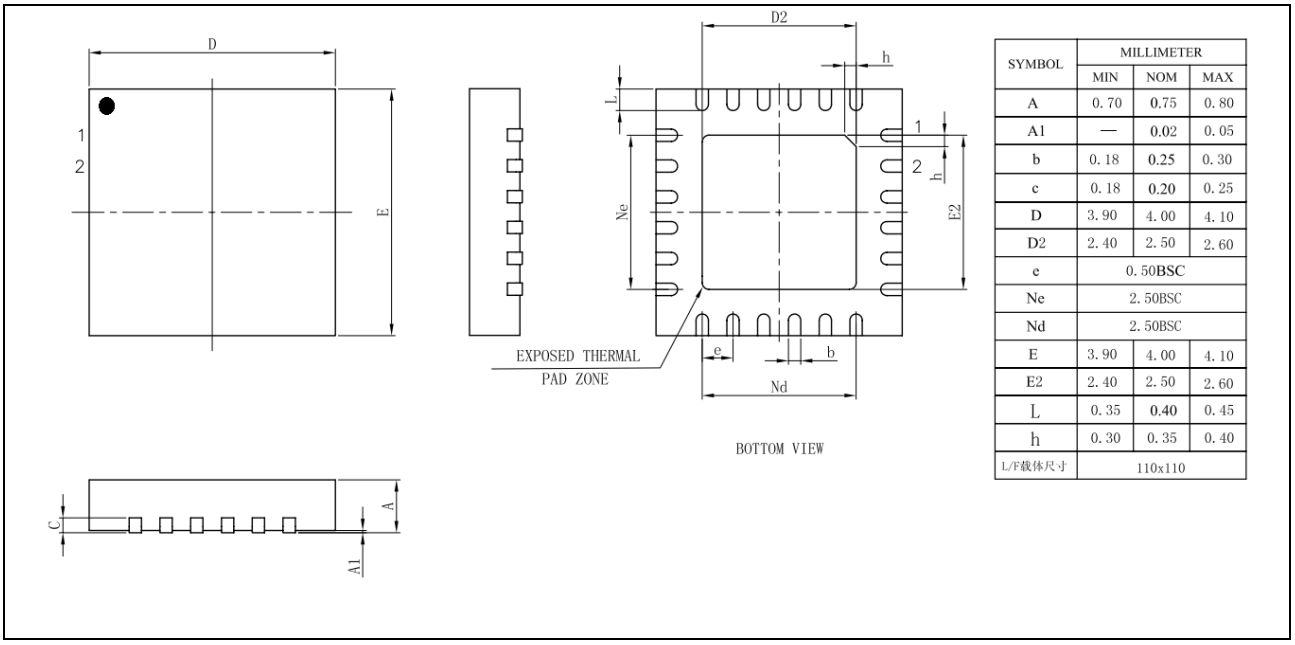
Layout Example



High Frequency Current Path

Package Dimension

QFN24



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸	110x110		

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026.03.06	Original Version	Chenzx	Xiayj	Liujy
1.1	2026.03.16	Update EC spec	Chenzx	Xiayj	Liujy
1.2	2026.04.16	Update EC spec	Chenzx	Xiayj	Liujy
1.3	2026.06.24	Update Function Description	Chenzx	Xiayj	Liujy