USB Type-C Analog Audio Switch with Protection Function

General Description

ET74802 is a high performance USB Type-C port multimedia switch which supports analog audio headsets. ET74802 allows the sharing of a common USB Type-C port to pass USB2.0 signal, analog audio, sideband use wires and analog microphone signal. ET74802 also supports high voltage on SBU port and USB port on USB Type-C receptacle side.

Features

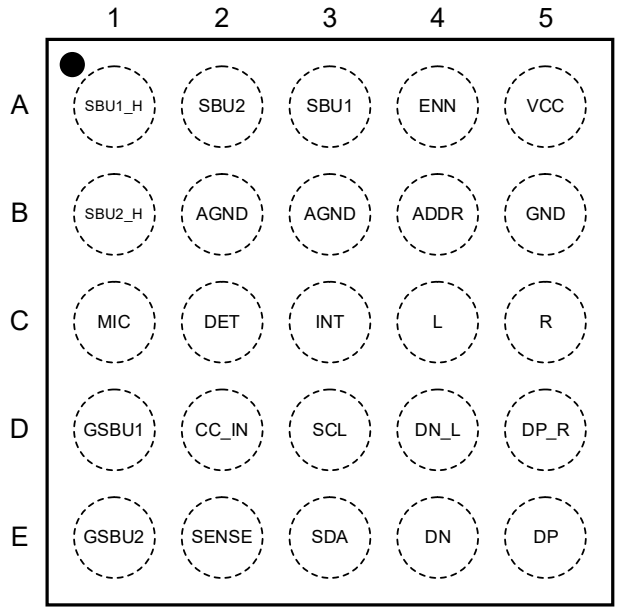
- Power Supply of V_{CC} is from 2.7 V to 5.5 V
- USB High Speed (480Mbps) Switch
  - -3dB bandwidth up to 750MHz
  - R_{ON} Typical is 3Ω
- Audio Switch
  - Negative Rail Capability is range of -3V~ +3V
  - THD+N = -110dB (@ $1V_{RMS}$, f=20Hz to 20 kHz, 32Ω R_{LOAD})
  - R_{ON} Typical is 0.8Ω
- High Voltage Protection
  - 20 V DC Tolerance on Connector Side Pins
  - Over Voltage Protection : V_{TH} = 5V (Typ)
- OMTP and CTIA Pin Out Support
- Support Audio Sense Path
- Part No. and Package

Part NO.	Package	Packing Option	MSL
ET74802	WLCSP25 (1.974mm × 1.974mm)	Tape and Reel ,3K	Level 1

Applications

- Smart Phone
- Tablet
- Notebook PC
- Media Player

Pin Configuration

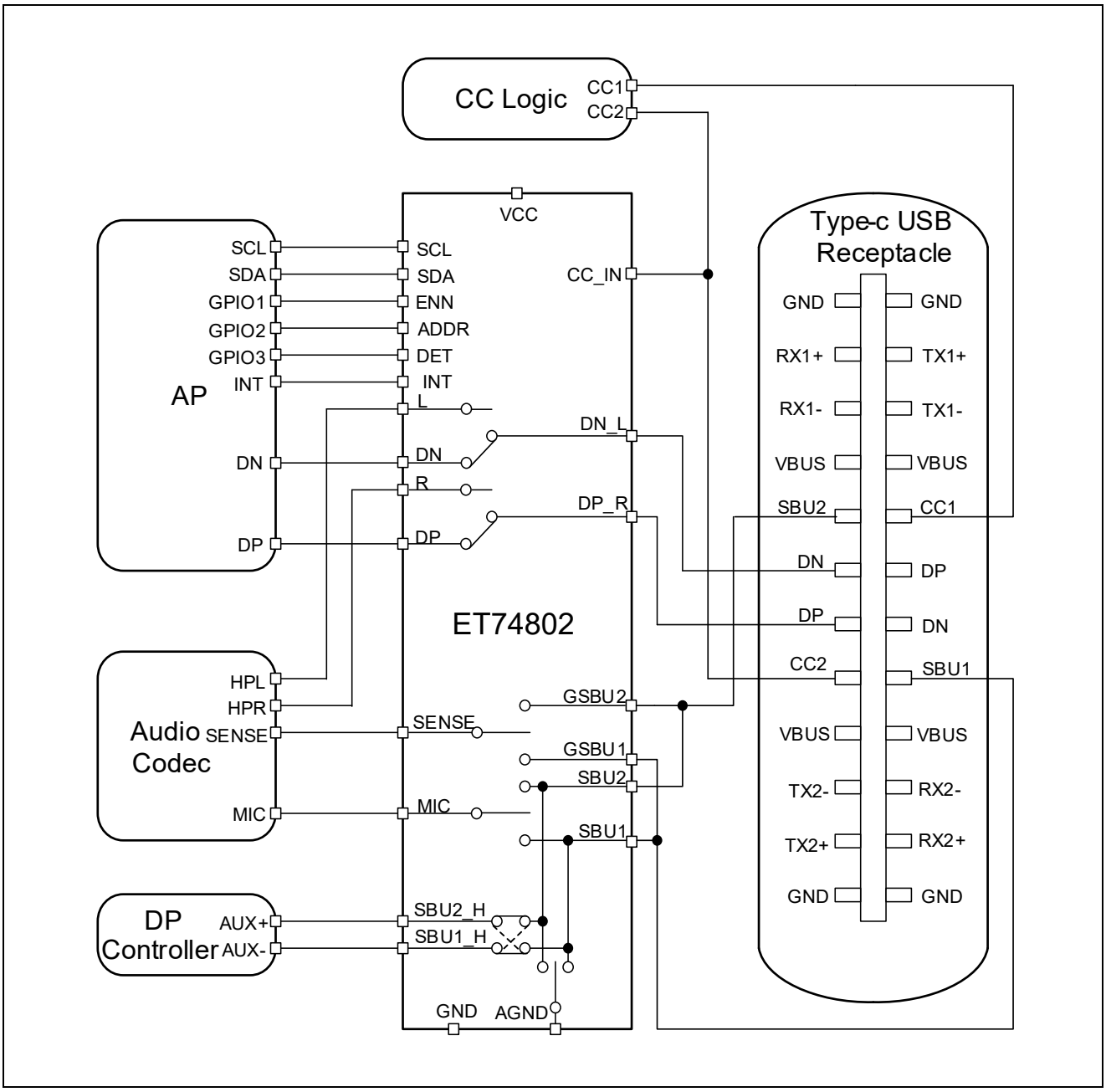


TOP VIEW

Pin Function

Pin No.		Name	Type	Pin Function
1	A5	VCC	Power	Power Supply (2.7 to 5.5 V)
2	B5	GND	Ground	Ground
3	D5	DP_R	I/O	USB/Audio Common Connector
4	D4	DN_L	I/O	USB/Audio Common Connector
5	E5	DP	I/O	USB2.0 Data (D+)
6	E4	DN	I/O	USB2.0 Data (D–)
7	C5	R	I/O	Audio – Right Channel
8	C4	L	I/O	Audio – Left Channel
9	A3	SBU1	I/O	Sideband Use Wire 1
10	A2	SBU2	I/O	Sideband Use Wire 2
11	C1	MIC	I/O	Analog audio Microphone Signal
12	B2	AGND	Ground	Audio Signal Ground
13	B3	AGND	Ground	Audio Signal Ground
14	E2	SENSE	I/O	Audio Ground Reference Output
15	C3	INT	O	I^2C Interrupt Output, Active Low (Open Drain)
16	D2	CC_IN	I	Audio Accessory Attachment Detection Input
17	D1	GSBU1	I/O	Audio Sense Path 1 to Headset Jack GND
18	E1	GSBU2	I/O	Audio Sense Path 2 to Headset Jack GND
19	C2	DET	O	Push-pull Output. When CC_IN>1.5V, DET is Low; CC_IN<1.2V, DET is High. When Audio switch off, DET is low.
20	D3	SCL	I	I^2C Clock
21	E3	SDA	I/O	I^2C Data
22	B1	SBU2_H	I/O	Host Side Sideband Use Wire 2
23	A1	SBU1_H	I/O	Host Side Sideband Use Wire 1
24	A4	ENN	I	Chip Enable, Active, Internal Pull-down by 2MΩ
25	B4	ADDR	I	I^2C Slave Address Pin

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage from V_{CC}	-0.5	6.5	V
V_{CC_IN}	CC_IN to GND	-0.5	20	V
V_{SW_C}	DP_R to GND, DN_L to GND	-3.6	20	V
V_{SW_USB}	DP to GND, DN to GND	-0.5	6.5	V
V_{SW_AUDIO}	L to GND, R to GND	-3.6	6.5	V
$V_{SBU/GSBU}$	SBU1 to GND, SBU2 to GND, GSBU1 to GND, GSBU2 to GND	-0.5	20	V
V_{SBU_H}	SBU1_H to GND, SBU2_H to GND	-0.5	6.5	V
$V_{I/O}$	SENSE, MIC, DET, INT, to GND	-0.5	6.5	V
V_{CNTRL}	Control Input Voltage (SDA, SCL, ENN, ADDR)	-0.5	6.5	V
I_{SW_AUDIO}	Switch I/O Current, Audio Path	-250	250	mA
I_{SW_USB}	Switch I/O Current, USB Path	100		mA
I_{SW_MIC}	Switch I/O Current, MIC to SBU1 or SBU2	50		mA
I_{SW_SBU}	Switch I/O Current, SBUx to SBUx_H	50		mA
I_{SW_SENSE}	Switch I/O Current, SENSE to GSBU1 or GSBU2	100		mA
I_{SW_AGND}	Switch I/O Current, AGND to SBU1 or SBU2	500		mA
I_{IK}	DC Input Diode Current	50		mA
V_{ESD}	Human Body Model (Connector Side Pins: SBU1, SBU2, DP_R, DN_L, GSBU1, GSBU2, CC_IN)	±4000		V
	Human Body Model (Host Side Pins: The Rest Pins)	±2000		V
	Charged Device Model	±2000		V
T_J	Junction Temperature	-40	125	°C
T_{STG}	Storage Temperature	-65	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Recommend Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Power					
V_{CC}	Supply Voltage	2.7	-	5.5	V
USB Switch					
V_{SW_USB}	DP to GND, DN to GND, DP_R to GND, DN_L to GND	0	-	4.5	V
Audio Switch					
V_{SW_AUDIO}	DP_R to GND, DN_L to GND, L to GND, R to GND	-3.6	-	3.6	V
MIC Switch					
V_{SBU_MIC}	SBU1 to GND, SBU2 to GND, MIC to GND	0	-	3.6	V
SENSE Switch					
V_{GSBU_SEN}	GSBU1 to GND, GSBU2 to GND, SENSE to GND	0	-	3.6	V
SBU to SBUx_H Switch					
V_{SBU}	SBU1 to GND, SBU2 to GND, SBU1_H to GND, SBU2_H to GND	0	-	3.6	V
CC_IN Pin					
V_{CC_IN}	CC_IN to GND	0	-	5.5	V
Control Voltage (ENN/SDA/SCL)					
V_{IH}	Input Voltage High	1.1	-	V_{CC}	V
V_{IL}	Input Voltage Low	0	-	0.5	V
Operating Temperature					
T_A	Ambient Operating Temperature	-40	+25	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC Electrical Characteristics

All typical values are at V_{CC} = 4.5V and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
I_{CC}	Supply Current	USB switches on, SBUx to SBUx_H switches on	V_{CC} = 3.3V	-	40	65	uA
			V_{CC} = 4.5V	-	45	75	
		Audio switches on, MIC switch on and Audio GND switch on	V_{CC} = 3.3V	-	40	65	
			V_{CC} = 4.5V	-	45	75	
I_{CCZ}	Quiescent Current	ENN = L, 04H'b7 = 0	V_{CC} = 3.3V	-	0.2	5	
			V_{CC} = 4.5V	-	0.3	6	
USB/AUDIO Common Pins : DP/R, DN_L							
I_{OZ}	Off Leakage Current of DP_R and DN_L	DN_L, DP_R = -3V to 3.6V	V_{CC} = 3.3V	-3.0	-	3.0	uA
			V_{CC} = 4.5V	-3.0	-	3.0	
I_{OFF}	Power-Off Leakage Current of DP_R and DN_L	DN_L, DP_R = 0 V to 3.6 V	Power off	-3.0	-	3.0	uA
V_{OV_TRIP}	Input OVP Lockout	Rising edge	V_{CC} =2.7V to 5.5V	4.7	5.0	5.3	V
V_{OV_HYS}	Input OVP Hysteresis			-	0.3	-	V
Audio Switch							
I_{ON}	On Leakage Current of Audio Switch	DN_L, DP_R = -3V to 3.0V, DP, DN, R, L = Float	V_{CC} = 3.3V	-3.0	-	3.0	uA
			V_{CC} = 4.5V	-3.0	-	3.0	
I_{OFF}	Power-Off Leakage Current of L and R	L, R = 0V to 3V, DP_R, DN_L = Float	Power off	-3.0	0.01	3.0	uA
R_{ON_AUDIO}	Audio Switch On Resistance	I_{SW} = 100mA, V_{SW} = -3V to 3V	V_{CC} = 2.7V to 5.5V	-	0.8	1.2	Ω
R_{SHUNT}	Pull-down Resistor on R/L Pin when Audio Switch is Off	L = R = 3V		6	10	14	kΩ
USB Switch							
I_{ON}	On Leakage Current of USB Switch	DN_L, DP_R = 0V to 3.6V, DP, DN, R, L = Float	V_{CC} = 3.3V	-3.0	-	3.0	uA
			V_{CC} = 4.5V	-3.0	-	3.0	
I_{OZ}	Off Leakage Current of DP and DN	DN, DP = 0V to 3.6V	V_{CC} = 2.7V to 5.5V	-3.0	0.01	3.0	uA
I_{OFF}	Power-Off Leakage Current of DP and DN	DN, DP = 0V to 3.6V	Power off	-3.0	0.01	3.0	uA
R_{ON_USB}	USB Switch On Resistance	I_{SW} = 8mA, V_{SW} = 0.4V	V_{CC} =2.7V to 5.5V	-	3.0	5.0	Ω

DC Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
SENSE Switch							
I_{ON}	Leakage Current of Sense Path	GSBUx = 0V to 1V, SENSE is floating	V_{CC} = 3.3V	-3.0	-	3.0	uA
			V_{CC} = 4.5V	-3.0	-	3.0	
R_{ON_SENSE}	SENSE Switch On Resistance	I_{OUT} = 100mA, V_{SW} = 1V	V_{CC} = 2.7V to 5.5V	-	260	500	mΩ
I_{OZ}	Off Leakage Current of SENSE	SENSE = 0V to 1V		-3.0	0.01	3.0	uA
	Off Leakage Current of GSBUx	GSBUx = 0V to 3.6V		-3.0	-	3.0	uA
I_{OFF}	Power-Off Leakage Current of SENSE	SENSE = 0V to 1V	Power off	-1.0	0.01	1.0	uA
	Power-Off Leakage Current of GSBUx	GSBUx = 0V to 3.6V		-3.0	-	3.0	
V_{OV_TRIP}	Input OVP Lockout on GSBUx	Rising edge	V_{CC} = 2.7V to 5.5V	4.6	4.9	5.2	V
V_{OV_HYS}	Input OVP Hysteresis of GSBUx			-	0.3	-	V
SBUx Pins							
I_{OZ}	Off Leakage Current of SBUx	SBUx = 0V to 3.6V	V_{CC} = 3.3V	-3.0	-	3.0	uA
			V_{CC} = 4.5V	-3.0	-	3.0	
I_{OFF}	Power-Off Leakage Current Port SBUx	SBUx = 0V to 3.6V	Power off	-3.0	0.01	3.0	uA
V_{OV_TRIP}	Input OVP Lockout	Rising edge	V_{CC} = 2.7V to 5.5V	4.6	4.9	5.2	V
V_{OV_HYS}	Input OVP Hysteresis			-	0.3	-	V
MIC Switch							
I_{ON}	On Leakage Current of MIC Switch	SBUx = 0V to 3.6V, MIC is floating	V_{CC} = 3.3V	-3.0	-	3.0	uA
			V_{CC} = 4.5V	-3.0	-	3.0	
I_{OZ}	Off Leakage Current of MIC	MIC = 0V to 3.6V	V_{CC} = 2.7V to 5.5V	-3.0	0.01	3.0	uA
I_{OFF}	Power Off Leakage Current of MIC	MIC = 0V to 3.6V	Power off	-1.0	0.01	1.0	uA
R_{ON_MIC}	MIC Switch On Resistance	I_{SW} = 30mA, V_{SW} = 0V to 3.6V	V_{CC} = 2.7V to 5.5V	-	2.5	4	Ω
SBUx_H Switch							
I_{ON}	On Leakage Current of SBUx_H Switch	SBUx = 0V to 4V, SBUx_H is floating	V_{CC} = 3.3V	-3.0	-	3.0	uA
			V_{CC} = 4.5V	-3.0	-	3.0	
I_{OZ}	Off Leakage of SBUx_H	SBUx_H =0 V to 3.6 V	V_{CC} =2.7V to 5.5V	-3.0	0.01	3.0	uA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
I_{OFF}	Power Off Leakage Current of SBUx_H	SBUx_H = 0V to 3.6V	Power off	-1.0	0.01	1.0	uA
$R_{ON_SBUx_H}$	SBUx_H Switch On Resistance	I_{SW} = 30mA, V_{SW} = 0V to 3.6V	V_{CC} = 2.7V to 5.5V	-	2.2	3.5	Ω
Audio Ground Switch Pin: AGND TO SBUX							
R_{ON_AGND}	AGND Switch On Resistance	I_{SOURCE} = 100mA on SBUx	V_{CC} = 2.7V to 5.5V	-	50	100	mΩ
CC_IN Pin							
V_{TH_L}	Input Low Threshold		V_{CC} = 2.7V to 5.5V	1.1	1.2	1.3	V
V_{TH_H}	Input High Threshold			1.4	1.5	1.6	V
I_{IL}	Input Leakage of CC_IN	CC_IN = 0V to 5.5V		0	-	1.0	uA
INT, DET Pins							
V_{OH}	Output High Voltage for DET Pin	I_O = -1mA	V_{CC} = 2.7V to 5.5V	1.5	1.75	2.0	V
V_{OL}	Output Low Voltage for DET and INT Pins	I_O = 1mA		-	-	0.4	V
ADDR Pin							
V_{IH}	Input voltage High		V_{CC} = 2.7V to 5.5V	0.9	-	-	V
V_{IL}	Input voltage Low			-	-	0.4	V
I_{IL}	Input Leakage of ADDR	ADDR = 2V		-1.0	0.01	1.0	uA
ENN Pin							
V_{IH}	Input Voltage High		V_{CC} = 2.7V to 5.5V	0.9	-	-	V
V_{IL}	Input Voltage Low			-	-	0.4	V
R_{PD}	Internal Pull-Down Resistor			330	470	610	kΩ
SDA, SCL Pins							
V_{IL_I2C}	Low-Level Input Voltage		V_{CC} = 2.7V to 5.5V	-	-	0.4	V
V_{IH_I2C}	High-Level Input Voltage			1.1	-	-	V
I_{I2C}	Input Current of SDA and SCL Pins	SCL/SDA = 0V to 3.6V		-	0.01	-	uA
V_{OL_SDA}	Output Voltage Low	I_{OL} = 2mA		-	-	0.4	V
I_{OL_SDA}	Low-Level Output Current	V_{OL_SDA} = 0.2V	V_{CC} = 2.7V to 5.5V	10	-	-	mA

AC Electrical Characteristics

All typical values are at V_{CC} = 4.5V and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
Audio Switch							
t_{delay}	Audio Switch Turn On Delay Time	DP_R = DN_L = 1V, R_L = 32Ω	V_{CC} =4.5V	-	120	-	us
t_{rise}	Audio Switch Turn On Rising Time (1)			-	240	-	us
t_{OFF}	Audio Switch Turn Off Time			-	20	-	us
X_{TALK}	Cross Talk (Adjacent)	f = 1kHz, R_L = 50Ω, V_{SW} = $1V_{RMS}$		-	-100	-	dB
V_{ISO}	Off Isolation	f = 1 kHz, R_L = 50Ω, C_L = 0pF,V_{SW} = $1V_{RMS}$		-	-100	-	dB
BW	-3dB Bandwidth	R_L = 50Ω		-	550	-	MHz
THD+N	Total Harmonic Distortion + Noise Performance with A-weighting Filter	R_L = 600Ω, f = 20Hz~20kHz, V_{SW} = $2V_{RMS}$		-	-110	-	dB
		R_L = 32Ω, f = 20Hz~20kHz, V_{SW} = $1V_{RMS}$		-	-110	-	
		R_L = 16Ω, f = 20Hz~20kHz, V_{SW} = $0.5V_{RMS}$		-	-108	-	
USB Switch							
t_{ON}	USB Switch Turn-on Time	DP_R = DN_L = 1.5V, R_L = 50Ω	V_{CC}=4.5V	-	70	-	us
t_{OFF}	USB Switch Turn -off Time			-	20	-	us
BW	-3 dB Bandwidth	R_L = 50Ω		-	750	-	MHz
V_{ISO}	Off Isolation between DP, DN and Common Node Pins	f = 1kHz, R_L = 50Ω, C_L = 0pF, V_{SW} = $1V_{RMS}$		-	-100	-	dB
t_{OVP}	DP_R and DN_L pins OVP Response Time	V_{SW} = 3.5V to 5.5V		-	0.8	1.5	us

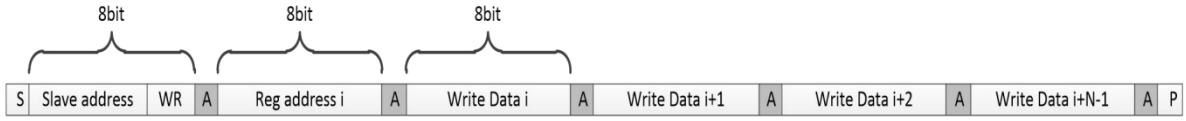
AC Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
MIC/AUDIO GROUND Switch							
t_{delay_MIC}	MIC Switch Turn On Delay Time	SBUx = 1V, R_L = 50Ω	V_{CC} =4.5V	-	100	-	us
t_{rise_MIC}	MIC Switch Turn On Rising Time (1)			-	250	-	us
t_{delay_AGND}	AGND Switch Turn On Time	SBUx pulled up to 0.5V by 16Ω		-	100	-	us
t_{rise_AGND}	AGND Switch Turn On Rising Time (1)			-	2.5	-	ms
t_{OFF_MIC}	MIC Switch Turn Off Time	SBUx = 2.5V, R_L = 50Ω		-	20	-	us
t_{OFF_AGND}	AGND Switch Turn Off Time	SBUx pulled up to 0.5V by 16Ω		-	20	-	us
BW	-3 dB Bandwidth	R_L = 50Ω		-	60	-	MHz
SBUx_H Switch							
t_{ON}	SBUx_H Switch Turn On Time	SBUx = 2.5V, R_L = 50Ω	V_{CC} =4.5V	-	150	-	us
t_{OFF}	SBUx_H Switch Turn Off Time			-	20	-	us
t_{OVP}	SBUx Pins OVP ResponseTime	V_{SW} = 3.5V to 5.5V		-	0.6	1.2	us
BW	-3 dB Bandwidth	R_L = 50Ω		-	60	-	MHz
SENSE Switch							
t_{delay}	Sense Switch Turn On Delay Time	GSBUx = 1V, R_L = 50Ω	V_{CC} =4.5V	-	100	-	us
t_{rise}	Sense Switch Turn On Rising Time (1)			-	250	-	us
t_{OFF}	Sense Switch Turn Off Time			-	20	-	us
t_{OVP}	GSBUx Pins OVP Response Time	V_{SW} =3.5V to 5.5V		-	0.6	1.2	us
BW	-3 dB Bandwidth	R_L = 50Ω		-	150	-	MHz
DET Delay							
t_{delay_DET}	DET Response Delay Time	Transition from 0 to 1.8V	V_{CC} =4.5V	-	5	-	us
		Transition from 1.8V to 0V		-	0.2	-	

Functional Description

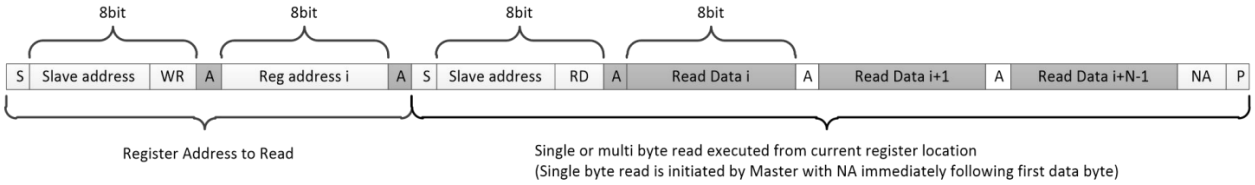
I²C Interface

The ET74802 includes a full I²C slave controller which fully complies with the I²C specification version 2.1 requirements. ET74802 works as a slave and is compatible with the following data transfer modes as defined in the I2C Bus Specification: Standard mode (100kbps), Fast mode (400kbps), Fast mode plus (1000kbps) and High-speed mode (up to 3.4Mbps in write mode). The interface adds flexibility to the device by making most functions and parameters programmable through the I2C host.



Note: Single Byte read is initiated by Master with P immediately following first data byte.

Figure 2. I²C Write Example



Note: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed.

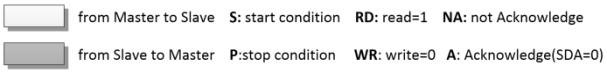


Figure 3. I²C Read Example

Over-Voltage Protection

The ET74802 features over-voltage protection (OVP) on receptacle side pins that switch off the internal signal routing path if the input voltage exceeds the OVP threshold. If OVP is occurred, interrupt signal can be send by INT signal and FLAG data will provide information that which pin had OVP event.

Headset Detection

ET74802 integrates headset unplug detection function by detecting the CC_IN voltage. The function is always active when device is enabling [(4)]. DET will be high when CC_IN is Low (CC_IN < 1.2V). When CC_IN is High (CC_IN > 1.5V), DET will be released to low.

	Device Disable	Device Enable
CC_IN < V_{TH_L} = 1.2 V	DET = 0	DET = 1
CC_IN > V_{TH_H} = 1.5 V	DET = 0	DET = 0

Note4. DET pin is in Push/Pull Configuration as default . If you don't use this detection function , leave it floating.

MIC Switch Auto-off Function

The function is active during control bit 0x12h bit[2] = 1. When CC_IN is high (CC_IN > 1.5 V) and L, R, Audio ground switches are under on status, MIC switch will be off and receptacle side pin will be connected to ground for 50us first. Then it shows high-Z status under MIC switch is set to on status.

Audio Ground Detection and Configuration

The function is active when control bit 0x12h bit[0] = 1 and R, L AGND switches are set to be on status. For Type-C interface analog headset, the audio ground could be SBU1 pin or SBU2 pin. The function will provide autonomous detection and configuration to route MIC and audio ground signal accordingly.

During detection and configuration, the R, L, Sense, MIC and Audio ground switch will be off. After detection and configuration, R and L switches will turn on according to switch configuration and timing setting. MIC, Sense and Audio ground will turn on according to detection results and timing control setting.

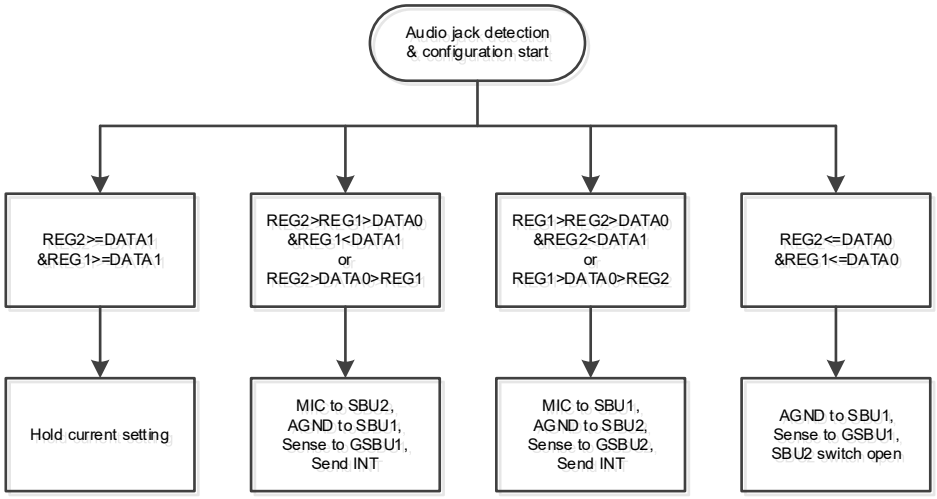


Figure 4. Audio Ground Detection and Configuration

Resistance Detection

The function is active during control bit 0x12h bit[1] = 1.

It will monitor the resistance between receptacle side pins and ground. During resistance detection, the switch which is monitored will be off. The detection result will be saved in the resistance flag register.

The measurement could be from 1kΩ to 2.56MΩ which is controlled by internal register. The detection interval can be set at 100ms, 1s or 10s by register 0x16h.

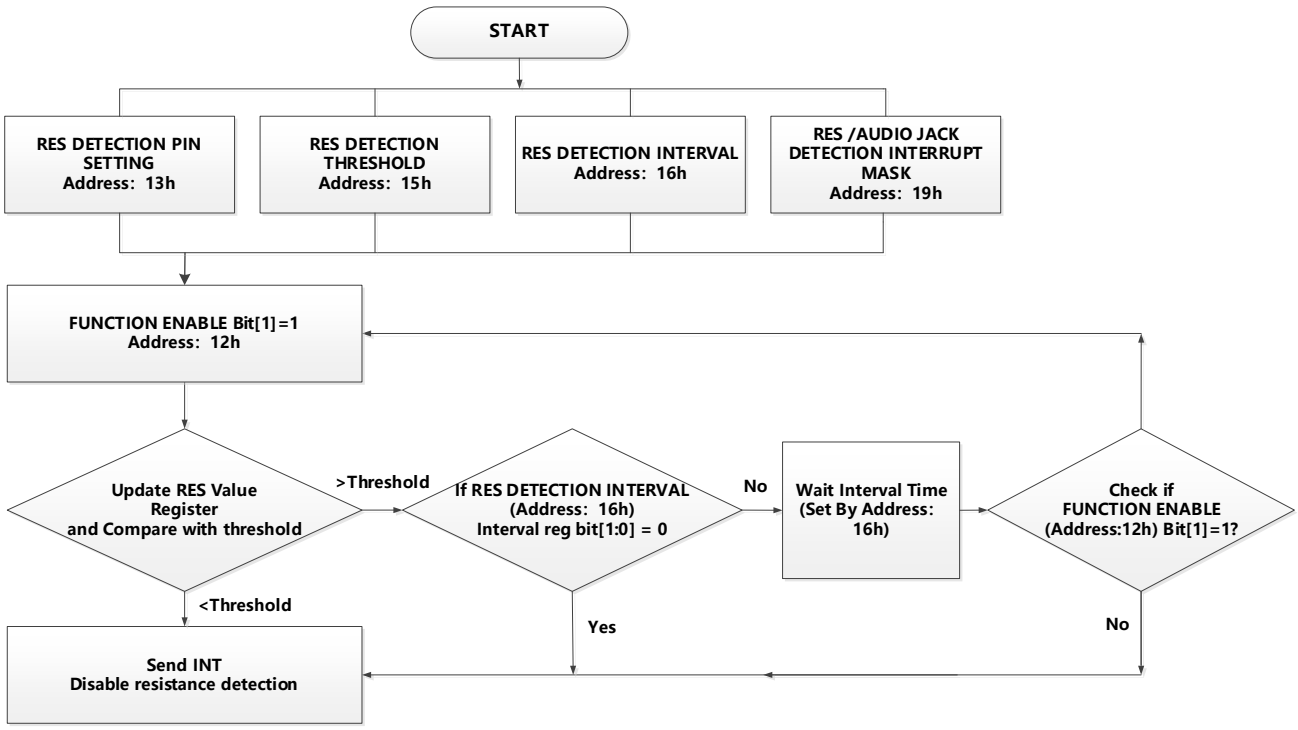


Figure 5. Resistance Detection

Manual Switch Control

The function is active during control bit 0x12h bit[4] = 1 and 0x04h = FF. It will provide manual control for device. During this configuration, ADDR and INT pins will be set as logic control input.

Power	ENN	ADDR	INT	SENSE Switch	Headset Detection	USB Switch	Audio Switch	MIC/ Audio GND Switch	SBU by Pass Switch
OFF	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	1	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	0	0	0	OFF	OFF	ON DP_R to DP DN_L to DN	OFF	OFF	ON SBU1 to SBU1_H SBU2 to SBU2_H
ON	0	0	1	OFF	OFF	ON DP_R to DP DN_L to DN	OFF	OFF	ON SBU1 to SBU2_H SBU2 to SBU1_H
ON	0	1	0	GSBU2 to SENSE	ON	OFF	DP_R to R DN_L to L	SBU1 to MIC SBU2 to AGND	OFF
ON	0	1	1	GSBU1 to SENSE	ON	OFF	DP_R to R DN_L to L	SBU2 to MIC SBU1 to AGND	OFF

Register Information

Register Maps

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	Device ID	R	0x59	0	1	0	1	1	0	0	1
01H	OVP Interrupt Mask	R/W	0x00	Reserved	Mask OVP Interrupt	Mask DP_R OVP	Mask DN_L OVP	Mask SBU1 OVP	Mask SBU2 OVP	Mask GSBU1 OVP	Mask GSBU2 OVP
02H	OVP Interrupt Flag	R/C	0x00	Reserved		DP_R	DN_L	SBU1	SBU2	GSBU1	GSBU2
03H	OVP Status	R	0x00	Reserved		DP_R OVP	DN_L OVP	SBU1 OVP	SBU2 OVP	GSBU1 OVP	GSBU2 OVP
04H	Switch Settings Enable	R/W	0x98	Device control	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	AGND to SBUx
05H	Switch Select	R/W	0x18	Reserved	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	AGND to SBUx
06H	Switch Status0	R	0x05	Reserved		Sense Switch Status		DP_R Switch Status		DN_L Switch Status	
07H	Switch Status1	R	0x00	Reserved		SBU2 Switch Status			SBU1 Switch Status		
08H	Audio Switch L Channel Turn On Control	R/W	0x01	Audio Switch Left Channel Slow Control [7:0]							
09H	Audio Switch R Channel Turn On Control	R/W	0x01	Audio Switch Right Channel Slow Control [7:0]							
0AH	MIC Switch Turn On Control	R/W	0x01	MIC Switch Channel Slow Control [7:0]							
0BH	Sense Switch Turn On Control	R/W	0x01	Sense Switch Channel Slow Control [7:0]							

Register Maps(Continued)

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0CH	AGND Switch turn on Control	R/W	0x01	Audio Ground Switch Channel Slow Control [7:0]							
0DH	Timing Delay Between R/L Switch Enable	R/W	0x00	Timing Delay Between R Switch Enable and L Switch Enable Control [7:0]							
0EH	Timing Delay Between MIC/L Switch Enable	R/W	0x00	Timing Delay between MIC Switch Enable and L Switch Enable Control [7:0]							
0FH	Timing Delay Between Sense/L Switch Enable	R/W	0x00	Timing Delay between Sense Switch Enable and L Switch Enable Control [7:0]							
10H	Timing Delay Between AGND/L Switch Enable	R/W	0x00	Timing Delay between Audio Ground Switch Enable and L Switch Enable Control [7:0]							
11H	Audio Accessory Status	R	0x01	Reserved						CC_IN	DET
12H	Function Enable	R/W	0x08	Reserved	DET I/O Control	RES	GIPO Control	Slow Turn−on Control	MIC Auto Control	RES Detection: Auto Clear	Audio Jack Detection: Auto Clear
13H	RES Detection Pin Select	R/W	0x00	Reserved					Detection Pin Select [2:0]		
14H	RES Detection Value	R	0xFF	R Detection Value [7:0]							

Register Maps(Continued)

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
15H	RES Detection Interrupt Threshold	R/W	0x16	RES Detection Interrupt Resistance Threshold [7:0]							
16H	RES Detection Interval	R/W	0X00	Reserved						Detection Interval [1:0]	
17H	Audio Jack Status	R	0x01	Reserved				4-pole, SBU2 MIC	4-pole, SBU1 MIC	3-pole	No audio
18H	Detection Interrupt	R/C	0x00	Reserved					Audio Detection Done	RES Detection Occurred	RES Detection Done
19H	Detection Interrupt Mask	R/W	0x00	Reserved					Audio Detection Done Mask	RES Detection Occurred Mask	RES Detection Done Mask
1AH	Audio Detection RGE1	R	0xFF	Audio Detection Value REG1 [7:0]							
1BH	Audio Detection RGE2	R	0xFF	Audio Detection Value REG2 [7:0]							
1CH	MIC Threshold DATA0	R/W	0x20	MIC Threshold Value DATA0 [7:0]							
1DH	MIC Threshold DATA1	R/W	0xFF	MIC Threshold Value DATA1 [7:0]							
1EH	I^2C Reset	W/C	0x00	Reserved							I^2C Reset
1FH	Current Source Setting	R/W	0x07	Reserved				Current Source Setting [3:0]			

Register specification

I²C Slave Address

ADDR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR=L	1	0	0	0	0	1	0	R/W
ADDR=H	1	0	0	0	0	1	1	R/W

00H: Device ID

Address: 0x00h

Reset Value: 0x59

Type:Read

Bits	Name	Description
7:6	Vendor ID	Vendor ID
5:3	Version ID	Device Version ID
2:0	Revision ID	Revision History ID

01H: OVP Interrupt Mask

Address: 0x01h

Reset Value: 0x00

Type:Read/Write

Bits	Name	Description
7	Reserved	Do Not Use
6	OVP Interrupt mask control	OVP Interrupt function Enable/Disable 0: Controlled by [5:0] bit 1: Mask all connector side pins OVP interrupt
5	DP_R OVP Interrupt mask control	0: Don't mask DP_R OVP interrupt 1: Mask DP_R OVP interrupt
4	DN_L OVP Interrupt mask control	0: Don't mask DN_L OVP interrupt 1: Mask DN_L OVP interrupt
3	SBU1 OVP Interrupt mask control	0: Don't mask SBU1 OVP interrupt 1: Mask SBU1 OVP interrupt
2	SBU2 OVP Interrupt mask control	0: Don't mask SBU2 OVP interrupt 1: Mask SBU2 OVP interrupt
1	GSBU1 OVP Interrupt mask control	0: Don't mask GSBU1 OVP interrupt 1: Mask GSBU1 OVP interrupt
0	GSBU2 OVP Interrupt mask control	0: Don't mask GSBU2 OVP interrupt 1: Mask GSBU2 OVP interrupt

02H: OVP Interrupt Flag

Address: 0x02h

Reset Value: 0x00

Type:Read Clear

Bits	Name	Description
[7:6]	Reserved	Do Not Use
5	DP_R OVP	0: DP_R OVP event has not occurred 1: DP_R OVP event has occurred
4	DN_L OVP	0: DN_L OVP event has not occurred 1: DN_L OVP event has occurred
3	SBU1 OVP	0: SBU1 OVP event has not occurred 1: SBU1 OVP event has occurred
2	SBU2 OVP	0: SBU2 OVP event has not occurred 1: SBU2 OVP event has occurred
1	GSBU1 OVP	0: GSBU1 OVP event has not occurred 1: GSBU1 OVP event has occurred
0	GSBU2 OVP	0: GSBU2 OVP event has not occurred 1: GSBU2 OVP event has occurred

03H: OVP Status

Address: 0x03h

Reset Value: 0x00

Type:Read

Bits	Name	Description
[7:6]	Reserved	Do Not Use
5	OVP on DP_R PIN	0: DP_R OVP event has not occurred 1: DP_R OVP event has occurred
4	OVP on DN_L PIN	0: DN_L OVP event has not occurred 1: DN_L OVP event has occurred
3	OVP on SBU1 PIN	0: SBU1 OVP event has not occurred 1: SBU1 OVP event has occurred
2	OVP on SBU2 PIN	0: SBU2 OVP event has not occurred 1: SBU2 OVP event has occurred
1	OVP on GSBU1 PIN	0: GSBU1 OVP event has not occurred 1: GSBU1 OVP event has occurred
0	OVP on GSBU2 PIN	0: GSBU2 OVP event has not occurred 1: GSBU2 OVP event has occurred

04H: Switch Enable

Address: 0x04h

Reset Value: 0x98

Type:Read/Write

Bits	Name	Description
7	Device Enable	0: Device Disable (L/R pull-down by 10kΩ and other switch nodes will be high-Z for positive input) 1: Device Enable
6	SBU1_H to SBUx switches	0: Switch Disable (SBU1_H will be high-Z for positive input) 1: Switch Enable
5	SBU2_H to SBUx switches	0: Switch Disable (SBU2_H will be high-Z for positive input) 1: Switch Enable
4	DN_L to DN or L switches	0: Switch Disable (DN_L, DN will be high-Z for positive input and L is pulled-down by 10kΩ) 1: Switch Enable
3	DP_R to DP or R switches	0: Switch Disable (DP_R, DP will be high-Z for positive input and R is pulled-down by 10kΩ) 1: Switch Enable
2	Sense to GSBUx switches	0: Switch Disable (Sense, GSBU1, GSBU2 will be high-Z for positive input) 1: Switch Enable
1	MIC to SBUx switches	0: Switch Disable (MIC will be high-Z for positive input) 1: Switch Enable
0	AGND to SBUx switches	0: Switch Disable (AGND will be high-Z for positive input) 1: Switch Enable

05H: Switch Select

Address: 0x05h

Reset Value: 0x18

Type:Read/Write

Bits	Name	Description
7	Reserved	Do Not Use
6	SBU1_H switches	0: SBU1_H to SBU1 switch ON 1: SBU1_H to SBU2 switch ON
5	SBU2_H switches	0: SBU2_H to SBU2 switch ON 1: SBU2_H to SBU1 switch ON
4	DN_L to DN or L switches	0: DN_L to L switch ON 1: DN_L to DN switch ON
3	DP_R to DP or R switches	0: DP_R to R switch ON 1: DP_R to DP switch ON
2	Sense to GSBUx switches	0: Sense to GSBU1 switch ON 1: Sense to GSBU2 switch ON
1	MIC to SBUx switches	0: MIC to SBU2 switch ON 1: MIC to SBU1 switch ON
0	AGND to SBUx switches	0: AGND to SBU1 switch ON 1: AGND to SBU2 switch ON

06H: Switch Status 0

Address: 0x06h

Reset Value: 0x05

Type:Read

Bits	Name	Description
[7:6]	Reserved	Do Not Use
[5:4]	Sense Switch Status	00: Sense Switch is Open/Not Connected 01: Sense to GSBU1 switch ON 10: Sense to GSBU2 switch ON 11: Not Valid
[3:2]	DP_R Switch Status	00: DP_R Switch is Open/Not Connected 01: DP_R to DP switch ON 10: DP_R to R switch ON 11: Not Valid
[1:0]	DN_L switch Status	00: DN_L Switch is Open/Not Connected 01: DN_L to DN switch ON 10: DN_L to L switch ON 11: Not Valid

07H: Switch Status 1

Address: 0x07h

Reset Value: 0x00

Type:Read

Bits	Name	Description
[7:6]	Reserved	Do Not Use
[5:3]	SBU2 Switch Status	000: SBU2 switch is Open/Not Connected 001: SBU2 to MIC switch ON 010: SBU2 to AGND switch ON 011: SBU2 to SBU1_H switch ON 100: SBU2 to SBU2_H switch ON 101: SBU2 to both SBU1_H and SBU2_H switch ON 110~111: Not Valid
[2:0]	SBU1 Switch Status	000: SBU1 switch is Open/Not Connected 001: SBU1 to MIC switch ON 010: SBU1 to AGND switch ON 011: SBU1 to SBU1_H switch ON 100: SBU1 to SBU2_H switch ON 101: SBU1 to both SBU1_H and SBU2_H switch ON 110~111: Not Valid

08H: Audio Switch Left Channel Slow Turn-on

Address: 0x08h

Reset Value: 0x01

Type:Read/Write

Bits	Name	Description
[7:0]	Switch turn on rising time setting	11111111: 32768us
		……
		00000001: 256us
		00000000: 128us

09H: Audio Switch Right Channel Slow Turn-on

Address: 0x09h

Reset Value: 0x01

Type:Read/Write

Bits	Name	Description
[7:0]	Switch turn on rising time setting	11111111: 32768us
		……
		00000001: 256us
		00000000: 128us

0AH: MIC Switch Slow Turn-on

Address: 0x0Ah

Reset Value: 0x01

Type:Read/Write

Bits	Name	Description
[7:0]	Switch turn on rising time setting	11111111: 32768us
		……
		00000001: 256us
		00000000: 128us

0BH: SENSE Switch Slow Turn-on

Address: 0x0Bh

Reset Value: 0x01

Type:Read/Write

Bits	Name	Description
[7:0]	Switch turn on rising time setting	11111111: 32768us
		……
		00000001: 256us
		00000000: 128us

0CH: AGND Switch Slow Turn-on

Address: 0x0Ch

Reset Value: 0x01

Type:Read/Write

Bits	Name	Description
[7:0]	Switch turn on rising time setting	11111111: 196608us
		……
		00000001: 1536us
		00000000: 768us

0DH: Timing Delay Between R Switch and L Switch Enable

Address: 0x0Dh

Reset Value: 0x00

Type:Read/Write

Bits	Name	Description
[7:0]	Delay timing setting	00001001-11111111: 128μs x (Bits-1), 11111111: 32512us
		00001000: 896us
		00000111: 700us
		……
		00000001: 100us
		00000000: 0us

0EH: Timing Delay Between MIC Switch and L Switch Enable

Address: 0x0Eh

Reset Value: 0x00

Type:Read/Write

Bits	Name	Description
[7:0]	Delay timing setting	00001001-11111111: 128μs x (Bits-1), 11111111: 32512us
		00001000: 896us
		00000111: 700us
		……
		00000001: 100us
		00000000: 0us

0FH: Timing Delay Between SENSE Switch and L Switch Enable

Address: 0x0Fh

Reset Value: 0x00

Type:Read/Write

Bits	Name	Description
[7:0]	Delay timing setting	00001001-11111111: 128μs x (Bits-1), 11111111: 32512us
		00001000: 896us
		00000111: 700us
		……
		00000001: 100us
		00000000: 0us

10H: Timing Delay Between AGND Switch and L Switch Enable

Address: 0x10h

Reset Value: 0x00

Type:Read/Write

Bits	Name	Description
[7:0]	Delay timing setting	00001001-11111111: 128μs x (Bits-1), 11111111: 32512us
		00001000: 896us
		00000111: 700us
		……
		00000001: 100us
		00000000: 0us

11H: Audio Accessory Status

Address: 0x11h

Reset Value: 0x01

Type:Read

Bits	Name	Description
[7:2]	Reserved	Do Not Use
1	CC_IN	0: CC_IN < 1.2 V 1: CC_IN > 1.5 V
0	DET	0: DET output is low 1: DET output is high

12H: Function Enable

Address: 0x12h

Reset Value: 0x08

Type:Read/Write

Bits	Name	Description
7	Reserved	Do Not Use
6	DET I/O Control	1: DET pin is Open/Drain Output 0: DET pin is Push/Pull Output
5	RES detection range setting	1: 10kΩ to 2560kΩ 0: 1kΩ to 256kΩ
4	GPIO control enable	1: Enable 0: Disable
3	Slow turn on control enable	1: Enable 0: Disable
2	MIC auto break out Control enable	1: Enable 0: Disable
1	RES detection enable	1: Enable (will be changed to 0 after resistance detection)

		0: Disable
0	Audio jack detection and configuration enable	1: Enable (will be changed to 0 after audio jack detection and configuration) 0: Disable

13H: RES Detection Pin Setting

Address: 0x13h

Reset Value: 0x00

Type:Read/Write

Bits	Name	Description
[7:3]	Reserved	Do Not Use
[2:0]	Pin selection	000: CC_IN 001: DP_R 010: DN_L 011: SBU1 100: SBU2 101~111: Not Valid

14H: RES Value

Address: 0x14h

Reset Value: 0xFF

Type:Read

Bits	Name	Description
[7:0]	Detected resistance value	00000000b: R < 1kΩ ..... 11111111b: R > 256kΩ

15H: RES Detection Threshold

Address: 0x15h

Reset Value: 0x16

Type:Read/Write

Bits	Name	Description
[7:0]	RES detection threshold	Selection by 1kΩ per step if Reg 12h [5] = 0 Selection by 10kΩ per step if Reg 12h [5] = 1 Default Value = 22kΩ 0000_0000: 1kΩ /10kΩ ..... 0001_0110: 22kΩ/220kΩ Default Value ..... 1111_1111: 256kΩ / 2560kΩ

16H: RES Detection Interval

Address: 0x16h

Reset Value: 0x00

Type:Read/Write

Bits	Name	Description
[7:2]	Reserved	Do Not Use
[1:0]	RES detection interval	00: Single 01: 100ms 10: 1s 11: 10s

17H: Audio Jack Status

Address: 0x17h

Reset Value: 0x01

Type:Read

Bits	Name	Description
[7:4]	Reserved	Do Not Use
3	4 pole	1: 4 Pole (SBU2 to MIC, SBU1 to AGND) 0: others
2	4 pole	1: 4 Pole (SBU1 to MIC, SBU2 to AGND) 0: others
1	3 pole	1: 3 Pole 0: others
0	No audio accessory	1: No audio accessory 0: Audio accessory attached

18H: RES Detection/Audio Jack Detection Interrupt Flag

Address: 0x18h

Reset Value: 0x00

Type:Read Clear

Bits	Name	Description
[7:3]	Reserved	Do Not Use
2	Audio jack detection and configuration	0: Audio jack detection and configuration has not occurred 1: Audio jack detection and configuration has occurred
1	Low resistance occurred	0: Low resistance has not occurred 1: Low resistance has occurred
0	Resistance detection done	0: Low resistance has not occurred 1: Low resistance has occurred

19H: RES Detection/Audio Jack Detection Interrupt Mask

Address: 0x19h

Reset Value: 0x00

Type:Read/Write

Bits	Name	Description
[7:3]	Reserved	Do Not Use
2	Audio jack detection and configuration mask	1: Mask Audio jack detection and configuration has occurred interrupt
1	Low resistance occurred	1: Low resistance has occurred interrupt
0	Low resistance detection	1: Low resistance detection has occurred interrupt

1AH: Audio Jack Detection REG1 Value

Address: 0x1Ah

Reset Value: 0xFF

Type:Read

Bits	Name	Description
[7:0]	Audio jack detection value	Resistance between SBU1 to SBU2

1BH: Audio Jack Detection REG2 Value

Address: 0x1Bh

Reset Value: 0xFF

Type:Read

Bits	Name	Description
[7:0]	Audio jack detection value	Resistance between SBU2 to SBU1

1CH: MIC Detection Threshold DATA0

Address: 0x1Ch

Reset Value: 0x20

Type:Read/Write

Bits	Name	Description
[7:0]	MIC detection threshold DATA0	MIC detection threshold DATA0 0010_0000: 300mV

1DH: MIC Detection Threshold DATA1

Address: 0x1Dh

Reset Value: 0xFF

Type:Read/Write

Bits	Name	Description
[7:0]	MIC detection threshold DATA1	MIC detection threshold DATA1 1111_1111: 2.4V

1EH: I²C Reset

Address: 0x1Eh

Reset Value: 0x00

Type: Write/Clear

Bits	Name	Description
[7:1]	Reserved	Do Not Use
0	I²C reset	0: Default 1: I²C reset

1FH: Audio Jack Detection Current Setting

Address: 0x1Fh

Reset Value: 0x07

Type: Read/Write

Bits	Name	Description
[7:4]	Reserved	Do Not Use
[3:0]	Current Source Setting	0000: Not Valid 0001: 100uA .... 0111: 700uA(Default Value) 1000: 800uA 1111: 1500uA

Test Diagrams

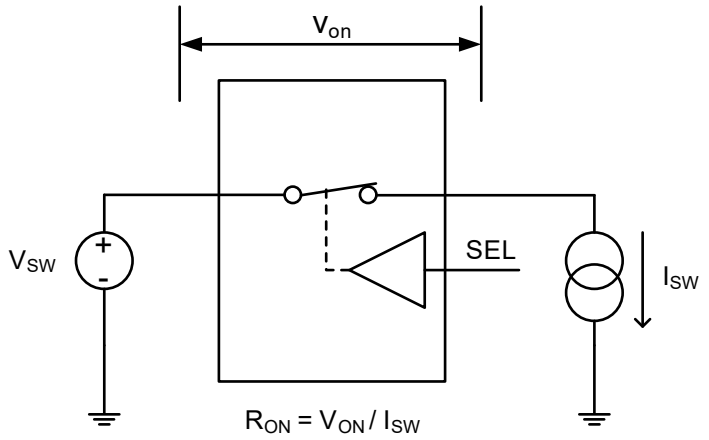


Figure6. on resistance $R_{ON}= V_{ON}/I_{SW}$

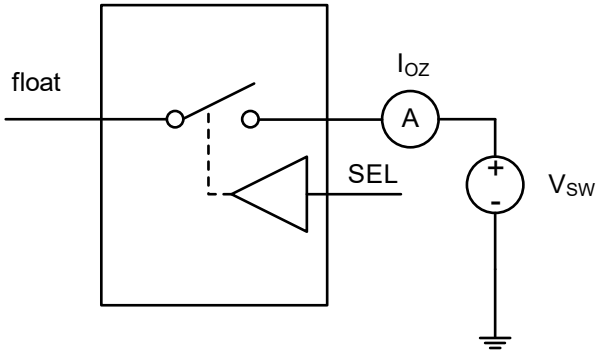


Figure7. off leakage(I_{OZ})

Note: each switch port is tested separately

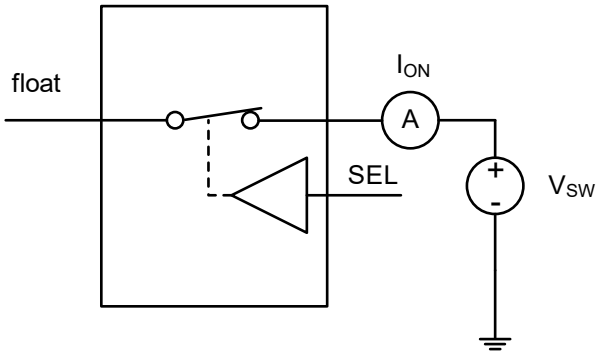


Figure8. on leakage

Test Diagrams(Continued)

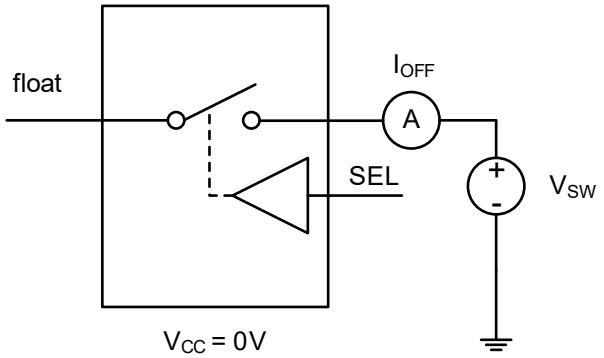


Figure9. power off leakage(I_{OFF})

Note: each switch port is tested separately

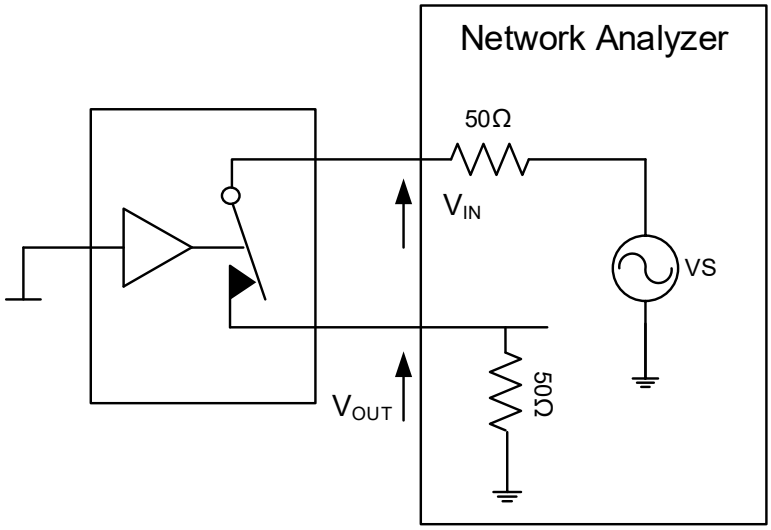
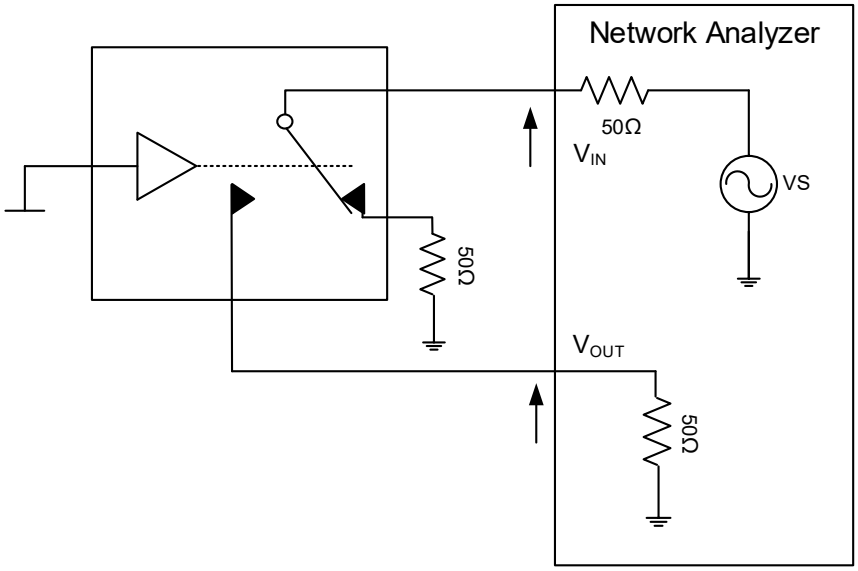


Figure10. Bandwidth



Off-Isolation=20 Log(V_{OUT}/V_{IN})

Figure11. Channel Off Isolation

Test Diagrams(Continued)

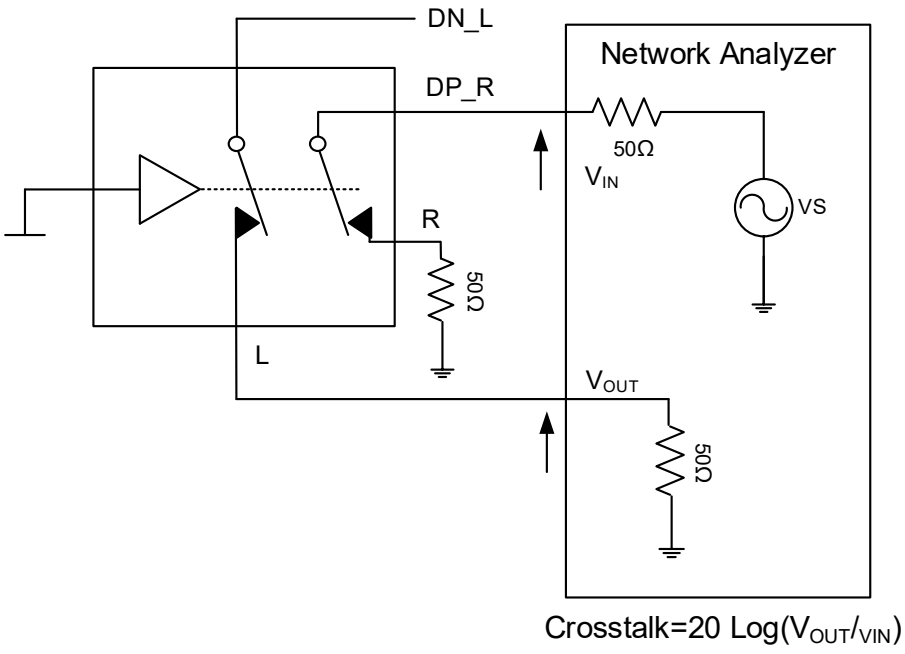


Figure12. Adjacent Channel Crosstalk

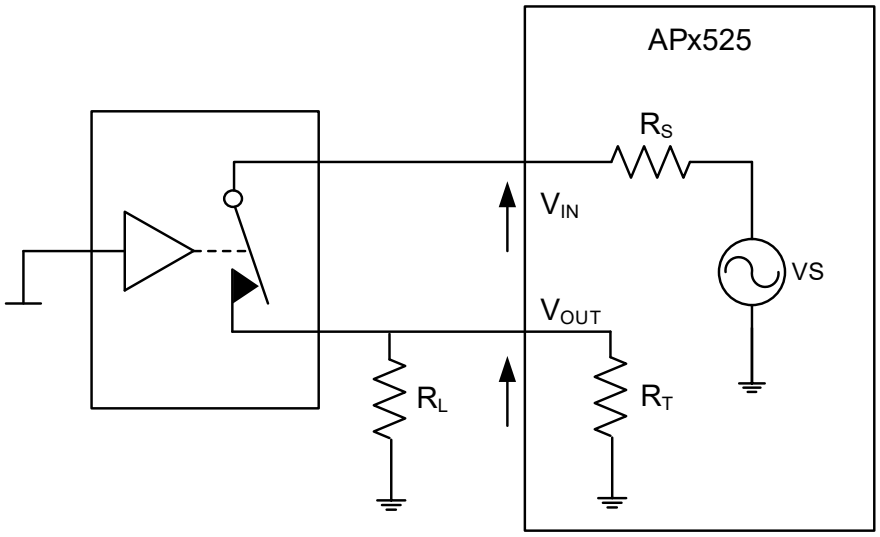
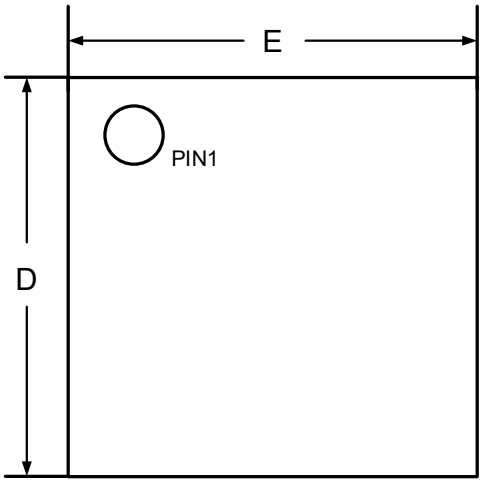
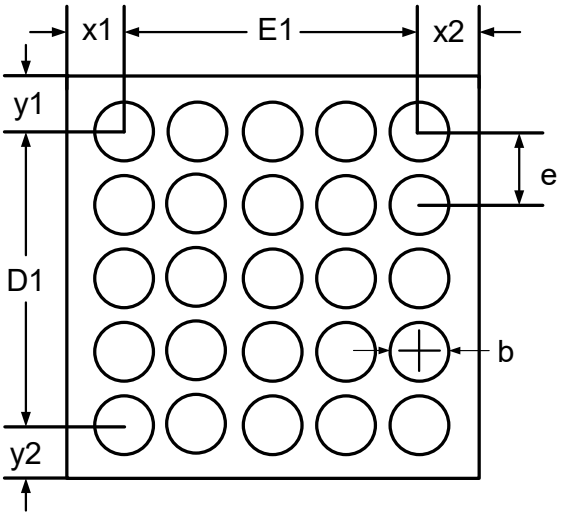


Figure13. Total Harmonic Distortion(THD+N)

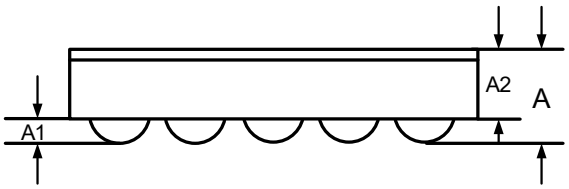
Package Dimension



TOP VIEW



BOTTOM VIEW

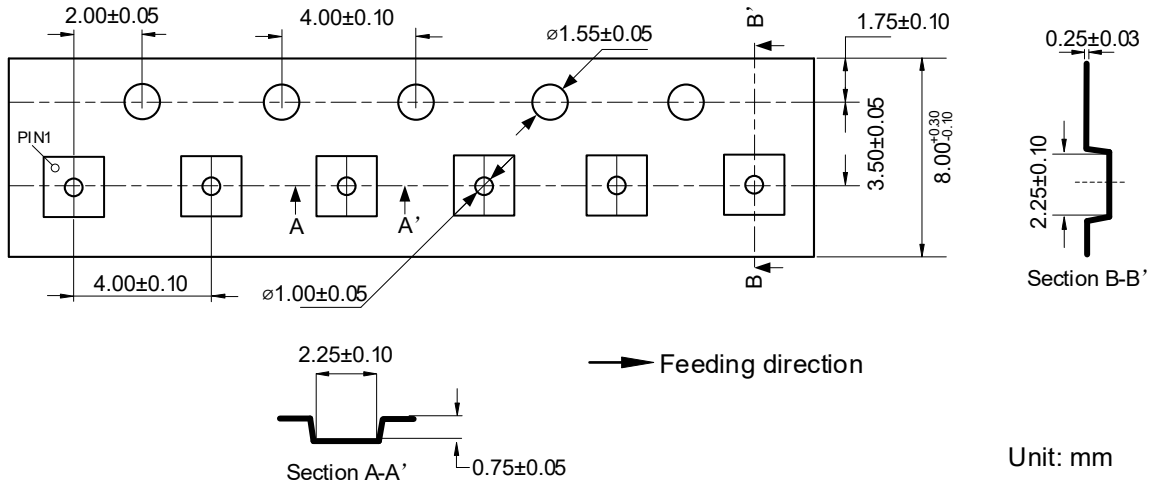


SIDE VIEW

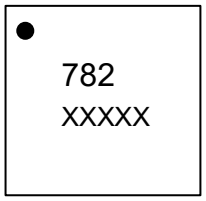
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

Symbol	Min	Nom	Max
A	0.538	0.576	0.614
A1	0.178	0.198	0.218
A2	0.360	0.378	0.396
D	1.948	1.974	2.000
D1	1.600 BSC		
E	1.948	1.974	2.000
E1	1.600 BSC		
b	0.245	0.265	0.285
e	0.400 BSC		
x1	0.187 REF		
x2	0.187 REF		
y1	0.187 REF		
y2	0.187 REF		

Tape Information



Marking Information



782 - Part Number

XXXXX - Tracking Number

Note：X (Tracking Number) is variable, according to the wafer lot number.

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-07-31	Original Version	Qinpl	Luhao	Liujy
1.1	2026-07-07	Update Package Dimension	Qinpl	Luhao	Liujy
1.2	2026-07-31	Update EC Table	Qinpl	Luhao	Liujy
1.2.1	2026-08-12	Add Tape and Mark Information	Qinpl	Luhao	Liujy