Dual-Rail Ultra-Low Dropout 1.5A LDO

General Description

The ET5A518ZB is CMOS-based low-dropout, low-power linear regulators, offering 1500mA with NMOS pass transistor and a separate bias supply voltage(V_{BIAS}). The device provides very stable, accurate output voltage with low noise, high ripple rejection and low supply current suitable for space constrained, noise sensitive application.

Features

- Wide V_{IN} Voltage Range: V_{OUT} + V_{DROP} to 5.5V & < V_{BIAS}
- Wide V_{BIAS} Voltage Range: 3.2V to 5.5V
- Fixed Output Voltage: 1.8V
- Very Low V_{BIAS} Input Current: 60μA
- Ultra-Low Dropout: 150mV at 1.5A@V_{OUT} = 1.8V
- Built-in Over-current Protection and Thermal Shutdown Circuit
- Built-in Auto-discharging Circuit
- Built-in Under Voltage Lock-out
- Part No. and Package Information

Part No.	Package	MSL
ET5A518ZB	WLCSP6 (1.2mm × 0.8mm × 0.35mm, 0.4pitch)	1

Applications

- Telecom Industrial and Consumer Equipment
- FPGA, DSP and Logic Power Supplies
- Switching Power Supply Post Regulation
- Specific Start−up Time or Sequencing Requirement Applications

Pin Configuration

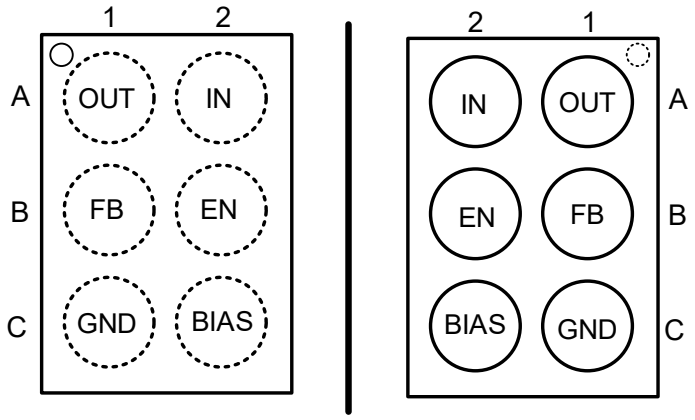


Figure1. Pin Configuration

Pin Function

Pin Name	Symbol	Pin Description
A1	OUT	The Power Output of the Device. A 22μF (typ.) ceramic capacitor is recommended at this pin.
A2	IN	Input Voltage Pin. Large bulk capacitance should be placed closely to this pin. A 10μF (typ.) ceramic capacitor is recommended at this pin.
B1	FB	Output Voltage Sensing Input. Connect to Output on the PCB to output the voltage corresponding to the part version.
B2	EN	Enable Input.
C1	GND	Ground Pin.
C2	BIAS	Input Voltage for Controlling Circuit. A 1μF (typ.) ceramic capacitor is recommended at this pin.

Block Diagram

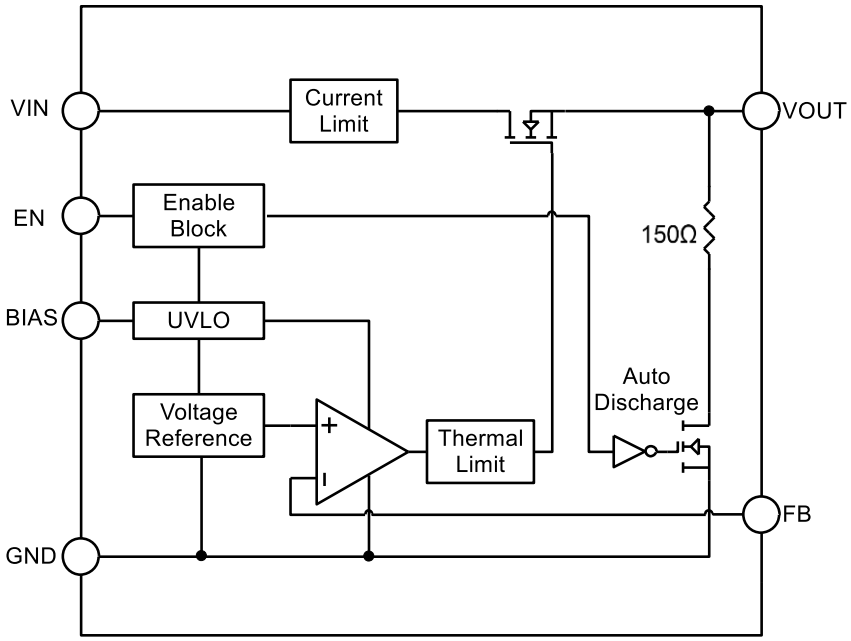


Figure2. Block Diagram

Functional Description

The ET5A518ZB dual−rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability. V_{IN} to V_{OUT} operating voltage difference can be very low compared with standard PMOS regulators in very low V_{IN} applications.

The ET5A518ZB offers smooth start-up.

Input and Output Capacitor

The device is designed to be stable for ceramic output capacitors with 4.7μF effective capacitance, greater ceramic capacitor is selected to get good dynamic performance. The device is also stable with multiple capacitors in parallel. In applications where no low input supplies impedance available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as example), the recommended C_{IN} = 10μF and C_{BIAS} = 1μF or greater.

Enable Pin Operation

The ET5A518ZB is turned on by setting the EN pin to “H”. The threshold limits are covered in the electrical characteristics table in this datasheet. When the EN pin is not used, connect the EN pin with V_{BIAS} to keep the LDO in operating mode.

Current Limit Protection

When output current of V_{OUT} pin is higher than current limit threshold or the V_{OUT} pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool down. When the junction temperature reduces to approximately 140°C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Auto Discharging

When the EN pin set to “L”, the output circuit will be disable immediately, and the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of V_{OUT} in very short time.

Power Up/Down Sequence Control

The recommended power on sequence of ET5A518ZB is to power on V_{SYS} first, then power on input power V_{IN}, then set V_{EN} to high level, and then enable LDO. The corresponding power off sequence is to turn off LDO. First, set V_{EN} to low level, then power off input power V_{IN}, and finally power off V_{SYS}.

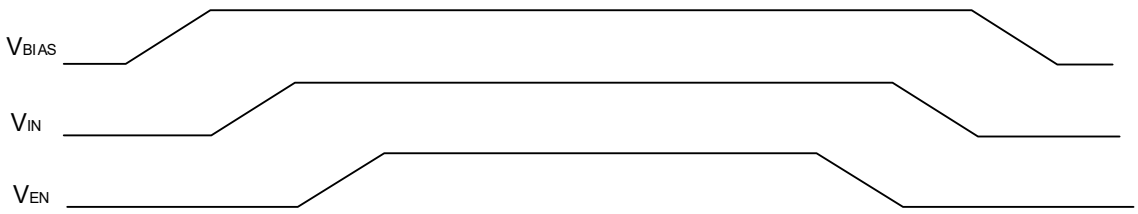


Figure3. Power Up/Down Switching Waveform

Absolute Maximum Ratings

Symbol	Item		Rating	Unit
V_{IN}	Input Voltage(IN Pin) (1)		-0.3 to 6.0	V
V_{BIAS}	Input Voltage (BIAS Pin) (1)		-0.3 to 6.0	V
V_{EN}	Input Voltage (EN Pin)		-0.3 to 6.0	V
V_{FB}	Input Voltage (FB Pin)		-0.3 to 6.0	V
V_{OUT}	Output Voltage(OUT Pin)		-0.3 to 6.0	V
I_{OUT_MAX}	Maximum Load Current		1500	mA
P_{D_MAX}	Maximum Power Consumption(PCB: 5cm × 5cm, 2layer, 1OZ)		1500	mW
T_{J_MAX}	Maximum Junction Temperature		-40 to 150	ºC
T_{STG}	Storage Temperature Range		-65 to 150	ºC
T_L	Lead Temperature (Soldering, 10 sec)		260	ºC
$R_{\theta JA}$	Thermal Resistance, Junction-to-Air		66.6	ºC/W
V_{ESD}	ESD Classification	Human Body Model (2)	±2000	V
		Charged Device Model (3)	±1500	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	IN Input Voltage	$V_{OUT}+V_{DROP}$ to 5.5 &$V_{IN}<V_{BIAS}$	V
V_{BIAS}	BIAS Input Voltage	3.2 to 5.5	V
I_{OUT}	Output Current	0 to 1500	mA
T_A	Operating Ambient Temperature	-40 to 85	ºC
T_J	Operating Junction Temperature	-40 to 125	ºC
C_{IN}	Effective Input Ceramic Capacitor Value	2.2 to 22	μF
C_{BIAS}	Effective Input Ceramic Capacitor Value	0.22 to 4.7	μF
C_{OUT}	Effective Output Ceramic Capacitor Value	4.7 to 33	μF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

Electrical Characteristics

(Unless otherwise noted, V_{IN} = 2.1V, V_{BIAS} = 3.4V, I_{OUT} = 1mA, C_{IN} = 10μF, C_{OUT} = 22μF, C_{BIAS} = 1μF, T_A = -40~85°C. Typical values are at T_A =25ºC)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}[1]	Input Voltage Range		V_{OUT} + V_{DROP}		5.5 & < V_{BIAS}	V
V_{BIAS}	V_{BIAS} Voltage Range		3.2		5.5	V
V_{UVLO}	Under-voltage lock-out	V_{BIAS} Rising		1.80		V
V_{UVLO_H}		Hysteresis		0.26		V
I_{Q_ON}	V_{BIAS} Current	Active Mode: V_{EN} = V_{BIAS}	40	60	100	μA
I_{Q_OFF}		V_{EN} = 0V		1.0	3	μA
V_{OUT}	Output Voltage	T_A = 25ºC	1.782	1.8	1.818	V
		T_A = -40 to 85ºC	1.764	1.8	1.836	V
V_{DROP}[2]	Dropout Voltage	I_{OUT} = 500mA		40	60	mV
		I_{OUT} = 1000mA		90	140	
		I_{OUT} = 1500mA		150	220	
I_{LIM}	Current Limit	V_{IN} = 2.1V, T_A = 25ºC	1.8	2.5	3.8	A
I_{SHORT}	Short Current Limit	V_{OUT} = 0V	400	700	1100	mA
Reg_{LOAD}	Load Regulation	1mA ≤ I_{OUT} ≤ 1500mA		2	25	mV
Reg_{LINE}	V_{IN} Line Regulation	2.1V ≤ V_{IN} ≤ 5V		0.01	0.1	%/V
	V_{BIAS} Line Regulation	3.4V < V_{BIAS} < 5.5V		0.01	0.1	%/V
PSRR[3]	Ripple Rejection	V_{IN} to V_{OUT}, f = 1kHz, V_{IN} = 2.3V, Ripple 0.2Vp-p, I_{OUT} = 30mA	60	70		dB
		V_{BIAS} to V_{OUT}, f = 1kHz, V_{IN} = 2.3V, Ripple 0.2Vp-p, I_{OUT} = 30mA	55	60		
e_N[3]	Output Noise	V_{IN} = 2.3V, f = 10Hz to 100kHz, I_{OUT} = 1mA	70	100	180	$μV_{RMS}$
I_{EN}	EN Pull-down Current	V_{EN} = 5.5V, V_{BIAS} = 5.5V		0.9	3	μA
V_{ENH}	EN Input Voltage High		0.9		5.5	V
V_{ENL}	EN Input Voltage Low		0		0.4	V
R_{DIS}	Output Resistance of Auto Discharge at Off State	V_{EN} = 0V	85	150	250	Ω

Electrical Characteristics (Continued)

(Unless otherwise noted, V_{IN} = 2.1V, V_{BIAS} = 3.4V, I_{OUT} = 1mA, C_{IN} = 10μF, C_{OUT} = 22μF, C_{BIAS} = 1μF, T_A = -40~85°C. Typical values are at. T_A = 25ºC)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{TRLD}(3)	Load transient	I_{OUT} = 1mA to 1500mA in 10us V_{IN} = 2.1V, T_A = 25ºC		70	150	mV
		I_{OUT} = 1500mA to 1mA in 10us V_{IN} = 2.1V, T_A = 25ºC		50	130	mV
T_{ON}	Turn-On Time	From Assertion of V_{EN} to V_{OUT} = 90%$V_{OUT(NOM)}$, T_A = 25ºC	150	360	720	μs
T_{TSD}(3)	Thermal shutdown threshold	T_J Rising	145	160	175	ºC
T_{HYS}(3)	Thermal shutdown hysteresis	T_J Falling from Shutdown	15	20	30	ºC

Note1: The maximum input voltage should take into account the maximum power consumption (PD(max)). The calculation formula is as follows:

$$\mathbf{PD(max) = (V_{IN}(max) - V_{OUT}) \times I_{OUT}}$$

The maximum power consumption of the circuit is 1500mW.

$$\mathbf{V_{IN(max)} = 1500mW / I_{OUT} + V_{OUT}}$$

For example:

V_{OUT} = 1.8V, I_{OUT} = 1500mA, the maximum input voltage is

$$\mathbf{V_{IN}(Max) = 1500mW / 1500mA + 1.8V = 2.8V}$$

Note2: V_{DROP} FT test method: test the V_{OUT} voltage at V_{OUT} + $V_{DROPMAX}$ with output current.

Note3: Guaranteed by design and characterization. not a FT item.

Application Circuit

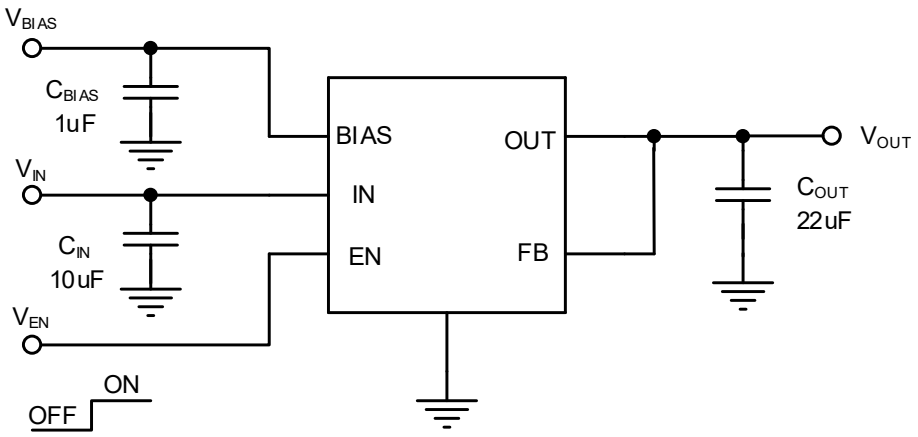
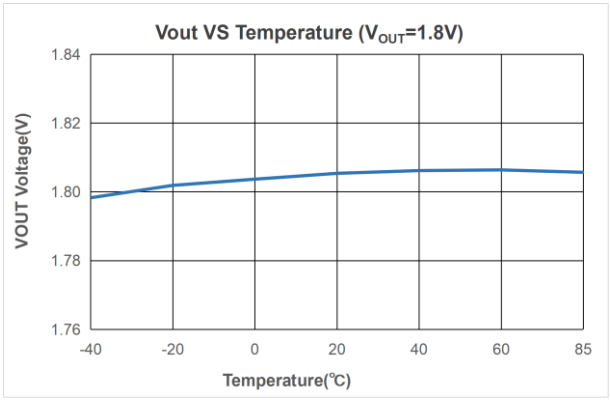


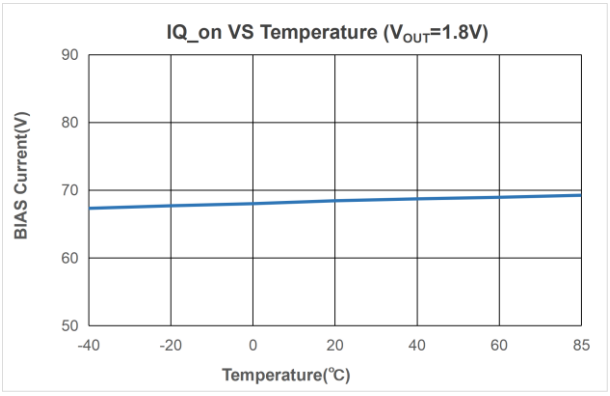
Figure4. Application Circuit

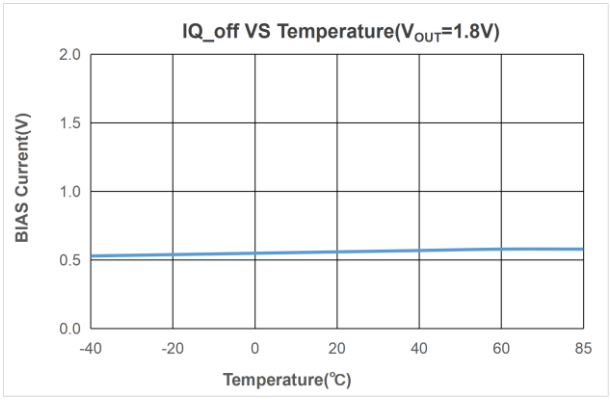
Typical Characteristics

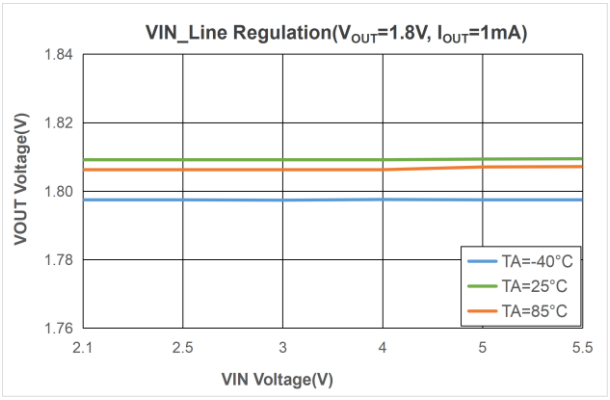
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

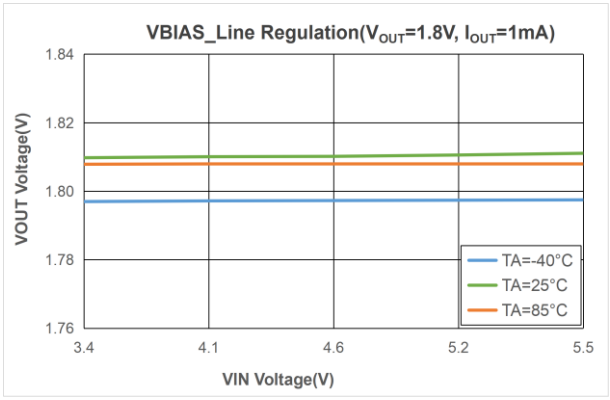
(V_{IN} = 2.1V, V_{BIAS} = 3.4V, I_{OUT} = 1mA, C_{IN} = 10μF, C_{OUT} = 22μF, C_{BIAS} = 1μF, V_{OUT} = 1.8V)

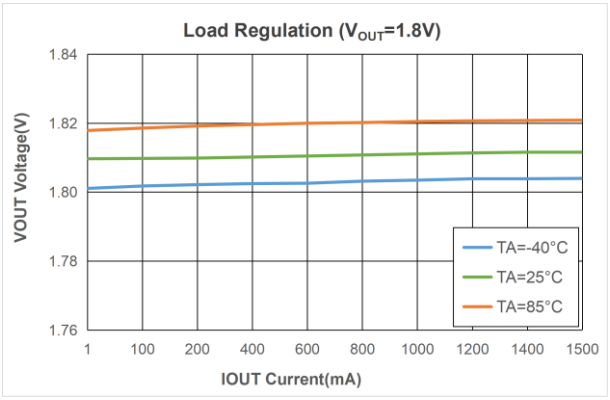












Typical Characteristics (Continued)

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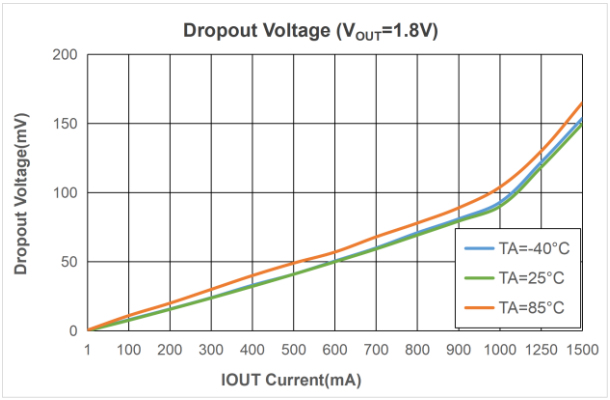
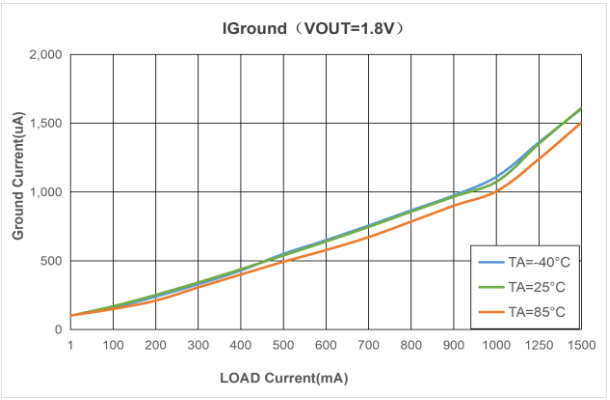
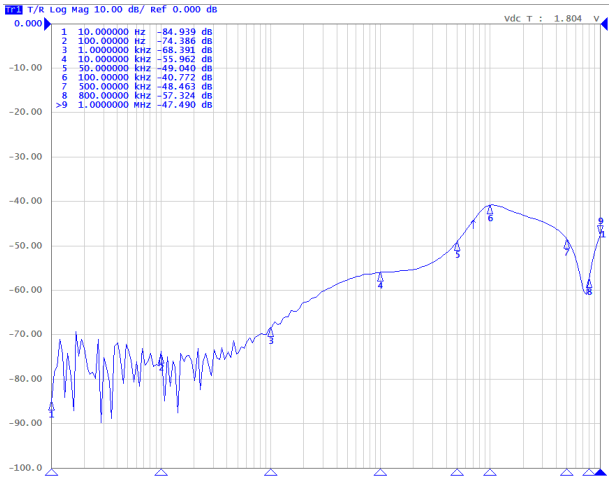
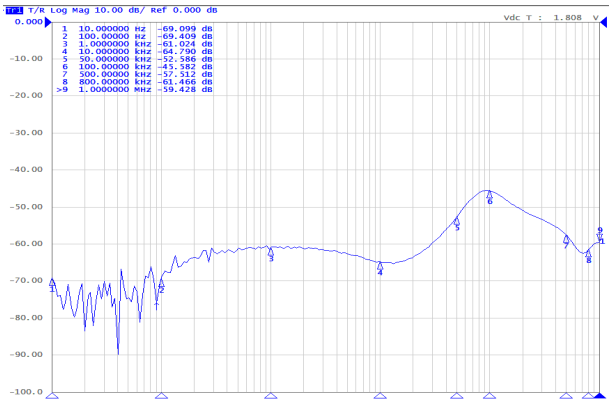
(V_{IN} = 2.1V, V_{BIAS} = 3.4V, I_{OUT} = 1mA, C_{IN} = 10μF, C_{OUT} = 22μF, C_{BIAS} = 1μF, V_{OUT} = 1.8V)



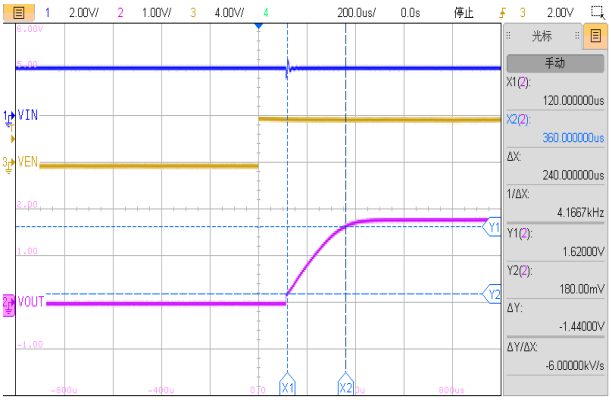




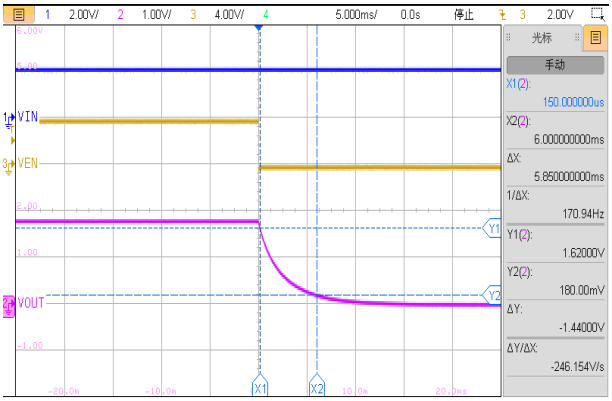
V_{IN} PSRR VS I_{OUT} (I_{OUT} = 30mA)



V_{BIAS} PSRR VS I_{OUT} (I_{OUT} = 30mA)



Turn On VS EN Voltage (I_{OUT} = 1mA)

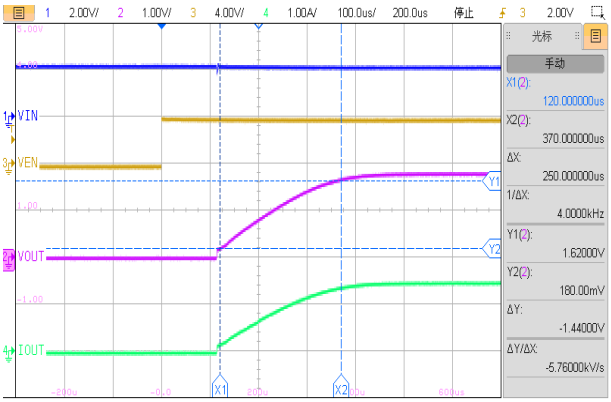


Turn Off VS EN Voltage (I_{OUT} = 1mA)

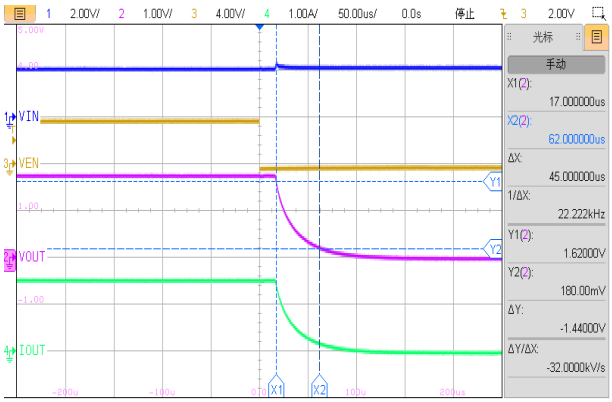
Typical Characteristics (Continued)

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

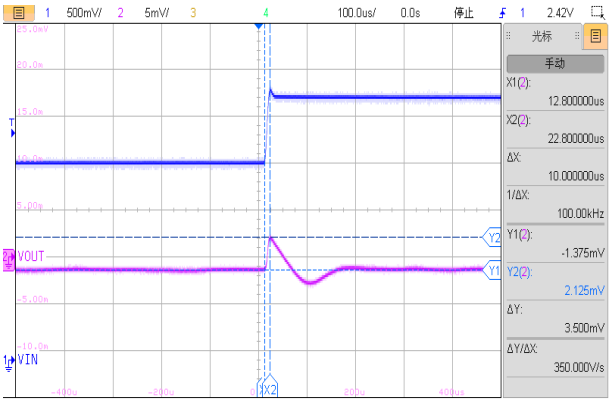
(V_{IN} = 2.1V, V_{BIAS} = 3.4V, I_{OUT} = 1mA, C_{IN} = 10μF, C_{OUT} = 22μF, C_{BIAS} = 1μF, V_{OUT} = 1.8V)



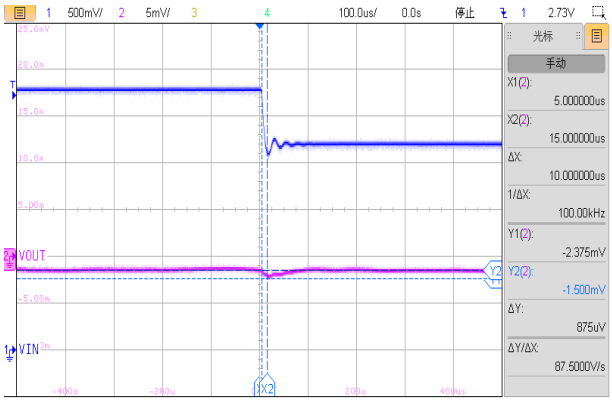
Turn On VS EN Voltage (I_{OUT} = 1500mA)



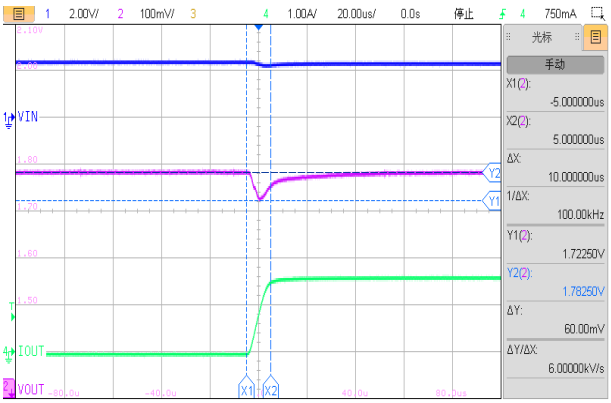
Turn Off VS EN Voltage (I_{OUT} = 1500mA)



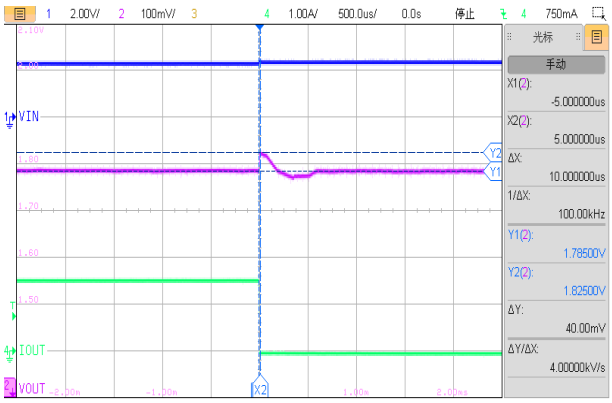
Line Transient Response(V_{IN} = 2.1~2.8V)



Line Transient Response(V_{IN} = 2.8~2.1V)



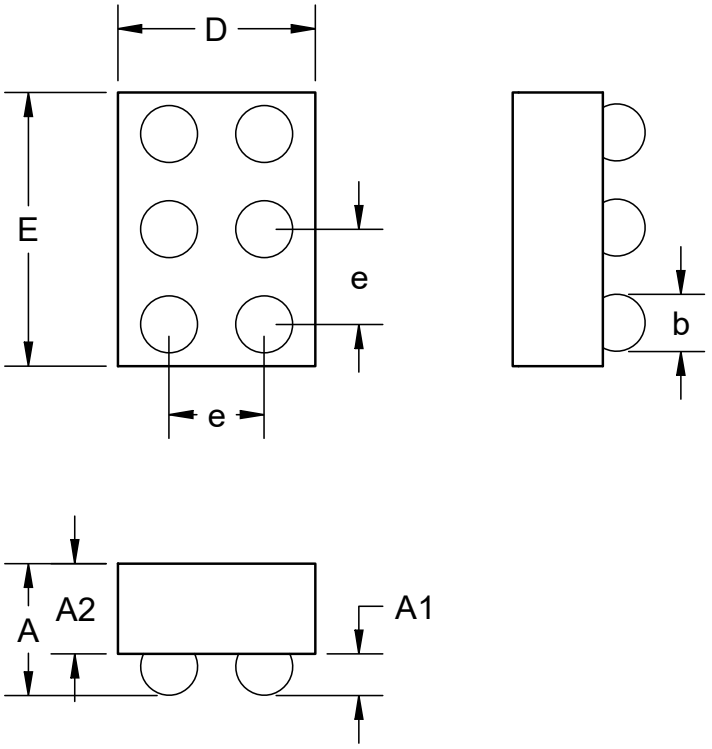
Load Transient Response (I_{OUT} = 1~1500mA)



Load Transient Response (I_{OUT} = 1500~1mA)

Package Dimension

WLCSP6

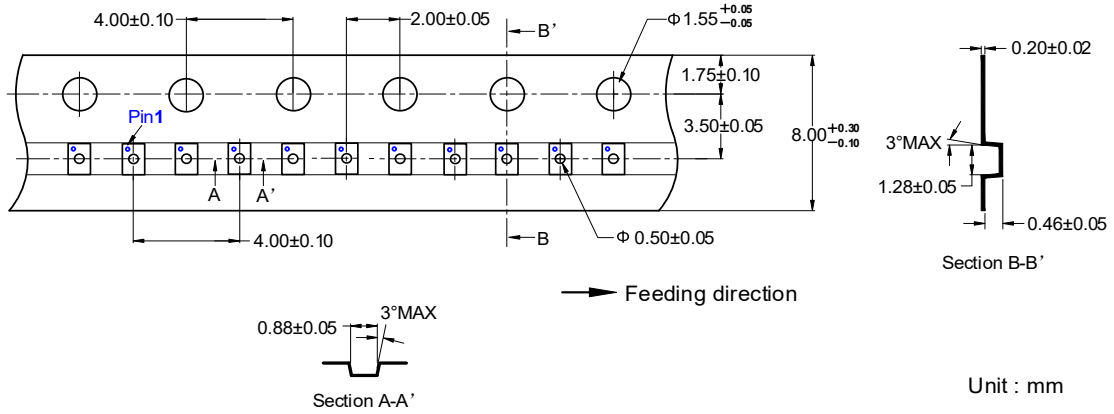


COMMON DIMENSIONS

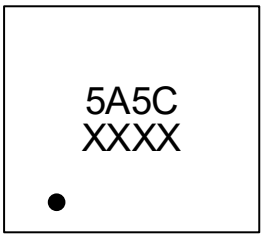
(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	0.32	0.36	0.40
A1	0.06	0.08	0.10
A2	0.26	0.28	0.30
b	0.22	0.24	0.26
D	0.754	0.774	0.804
E	1.156	1.176	1.206
e	0.400 BSC		

Tape Information



Marking Information



5A5C = Part Number
XXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2022-12-26	Preliminary Version	Tu guozhu	Liu xiaomin	Liu jiaying
1.0	2023-04-16	Official Version	Tu guozhu	Liu xiaomin	Liu jiaying
1.1	2026-04-23	Update Electrical Characteristics	Xu tao	Yang xiaoxu	Liu jiaying
1.1.a	2026-04-27	Update V_{BIAS_MIN} to 3.2V	Yang xiaoxu	Yang xiaoxu	Liu jiaying
1.2	2026-08-03	Update EC table and Tape	Xu tao	Yang xiaoxu	Liu jiaying