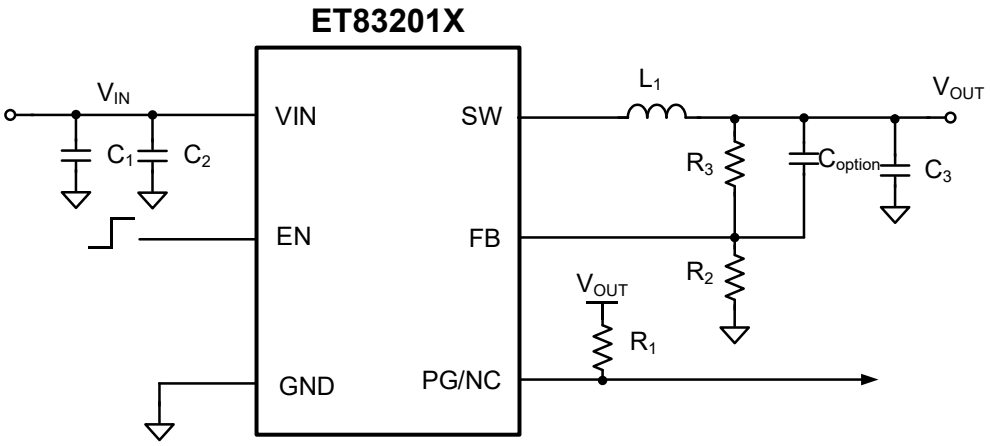
ET83201H – High Efficiency, 6V/2A Buck Converter

General Description

The ET83201H device family is a high-efficiency, synchronous step-down converter supports 2A output current and withstand 6V input voltage. The device operates with constant off time combined with a peak current control scheme. The control circuit calculates the off time for the low-side MOSFET, making the switching frequency relatively constant regardless of the variation of the input voltage, output voltage, and load current. The control scheme provides a fast transient response and eases loop stabilization. The 2.3MHz switching frequency allows the device to use small external components.

The ET83201H supports 100% duty mode when the required output voltage is higher than the input voltage and smooth switch to step-down operation when the input voltage is higher than the target output.

ET83201H is available in multiple package options, including: DFN-6 and SOT563.



Features

- Input voltage range: 2.4V – 6V, down to 1.9V after startup
- Reference voltage accuracy: 0.6V ± 1.0% at room temperature
- 40μA typical quiescent current
- High efficiency operation
  - -90% efficiency at 2A load from 5V to 3.3V conversion
  - -89% efficiency at 0.5A load from 3.6V to 1.2V conversion
- Automatic PFM mode to extend battery life or Forced PWM version to minimize output ripple
- Typical 2.3-MHz switching frequency
- Constant off time control scheme to achieve fast load transient response
- 100% duty mode
- PG output (with PG pin versions only)
- Integrated UVLO, OCP, SCP, and thermal protections
- 0.35ms typical soft-start time
- 1.2 V I/O compatible
- Active output discharge
- Package:

Part No.	Package	MSL
ET83201HY	DFN6 (1.6×1.6)	Level 1
ET83201H	SOT563	Level 1

Applications

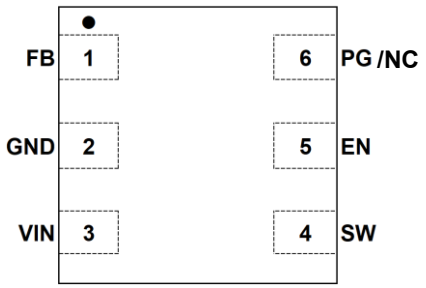
- Smartphone
- IPC
- TV/Box
- USB or single-cell Li-ion battery applications

Device Information

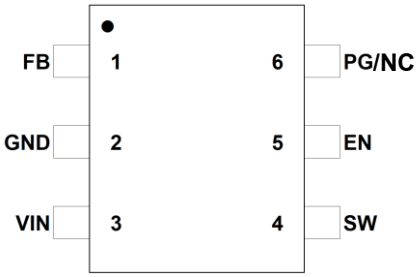
Orderable Part Number	Mode	Power Good
ET83201H	Auto PFM	NO
ET83201HY	Auto PFM	NO
ET83201HC[Note1]	FPWM	YES
ET83201HYC[Note1]	FPWM	YES

Note1: Not released. Please contact local ETEK sales for more information.

Pin Configuration



TOP VIEW (DFN1616)

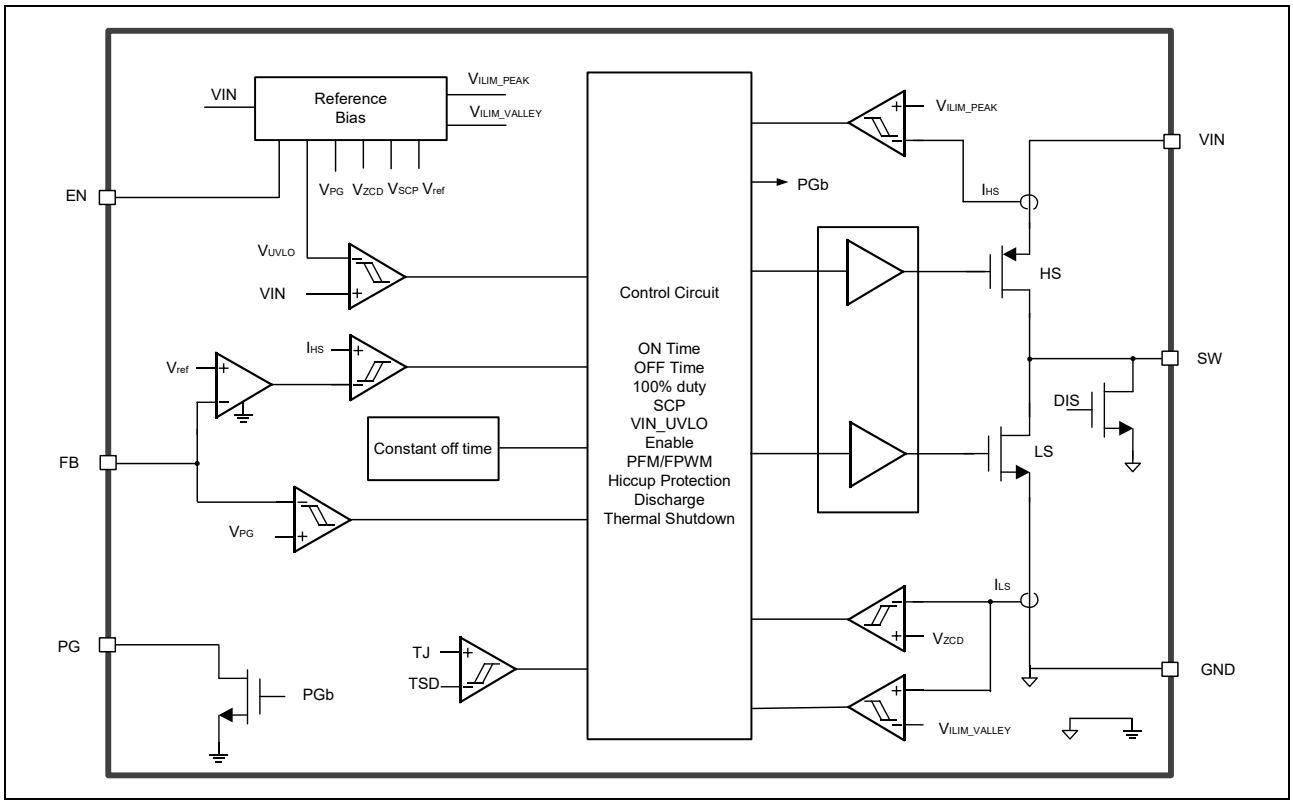


TOP VIEW (SOT563)

Pin Function

Pin No. Package DFN1616/SOT563	Pin Name	Pin Function
1	FB	Output voltage feedback. Connect resistor divider at this pin
2	GND	Ground
3	VIN	Power input. A 10μF bulk capacitor should be placed between this pin and GND pin.
4	SW	Switching Node
5	EN	Enable
6	PG/NC	For Power Good versions, this pin is the power good indication. This pin is open-drain output. For no Power Good versions in the device information list, this pin is no connection inside

Block Diagram



Functional Description

Overview

The ET83201H is a high-efficiency synchronous step-down converter supports up to 2A output current and withstand 6V input voltage. The ET83201H operates with constant off time combined with a peak current control scheme to achieve fast transient response. The control circuit calculates the off time for the low-side MOSFET, making the switching frequency relatively constant regardless of the variation of the input voltage, output voltage, and load current. The ET83201H seamless transfer between the buck mode and 100% duty mode by sensing the input voltage and output voltage.

Constant OFF-Time Control Scheme

The ET83201H is synchronous buck converter with the constant-off-time (COT) control mechanism to provides fast transient response and eases loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on. The on period is determined by both the error amplifier output voltage and the current through the HS-FET. When the current reaches the error amplifier output voltage, the on time is terminated and the LS-FET is turned ON, which is the start of the off-Time. The off-time is calculated by the control circuit which is proportional to the voltage difference between the input voltage and output voltage. The HS-FET turned on again when the off-time timer is over. By repeating operation this way, the converter regulates the output voltage.

Internal compensation is applied for constant off time control for stable operation even when ceramic capacitors are used as output capacitors.

The ET83201H operates at typical 2.3MHz switching frequency and please find the device information table for more information. Higer switching frequency operation enables better transient performance and reduced the output ripple at the cost of higher switching loss.

Auto-PFM

The ET83201H is designed to maintain high efficiency at light load by adopting automatic pulse-frequency modulation (Auto PFM). When the output current decrease, the current through the inductor decrease to zero during the off-time. When the inductor current reaches zero, detected by the zero-current detection (ZCD) comparator, the low-side MOSFET is turned off, together with the high-side MOSFET. Both MOSFETs remains off until the error amplifier output voltage rises above PFM threshold. As the load current decreases, the duration for both MOSFETs to remain off increases, leading to a lower switching frequency and higher power efficiency.

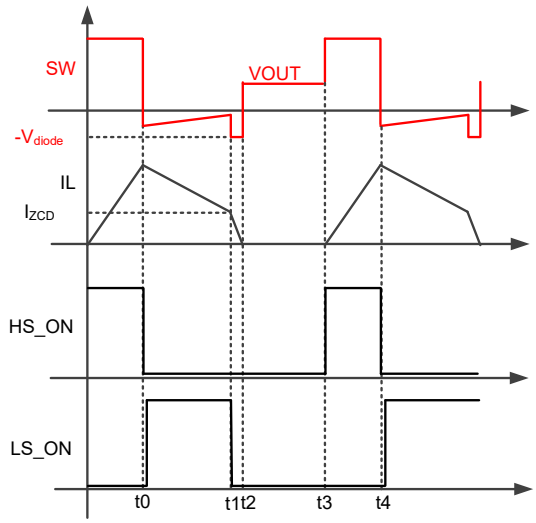


Figure 1. Auto-PFM at light load

ET83201H exits the PFM mode automatically and enter CCM when the load increases to the level when the minimum inductor current increases to higher than zero.

FPWM

In FPWM mode, the ET83201HXC keeps the switching frequency constant at light load condition. When the load current decreases, the high-side switch is not turned off even if the current of the high-side switch goes negative to keep the frequency constant. The output ripple is greatly reduced at light load compared with the PFM mode.

The ZCD threshold changes to positive with a typical -1.2A current limit which is named negative current limit (NOCL). When the inductor current hits the NOCL, the low side FET is turned off immediately and the high-side MOSFET is forced turning on after the dead time. In the next switching cycle, the inductor current ramps up again and then ramp down the same as the beginning.

For FPWM version, please choose the correct inductor to ensure the peak-to-peak current under no load condition is higher than 300mA.

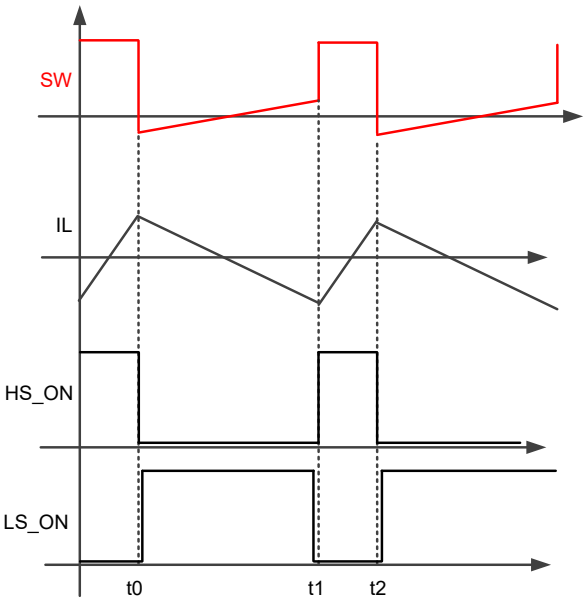


Figure 2. FPWM at no load

100% duty mode

ET83201H supports 100% duty mode when the input voltage is close or even lower than the target output voltage. This is achieved automatically inside ET83201H. The HS-FET is kept always ON and LS-FET is always OFF. The current limit function and short circuit protections are still active in 100% mode.

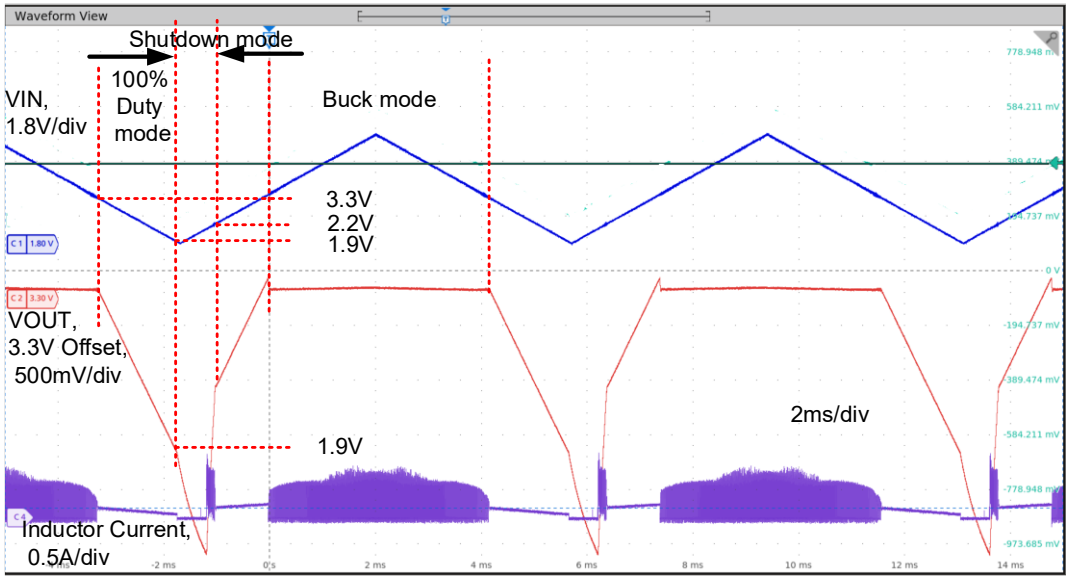


Figure 3. Entry and Exit 100% Duty Mode, 30Ω Load

Soft-start

When the VIN is above the UVLO threshold and EN voltage rises above the EN pin logic high threshold, after an EN blanking time t_b (1μs typically) and delay time T_d(see the value in EC table), then the ET83201H

enables all the internal circuits, delays for a certain delay time, and begins the soft-start. The internal reference voltage ramps up to V_{ref} in t_{ss} time.

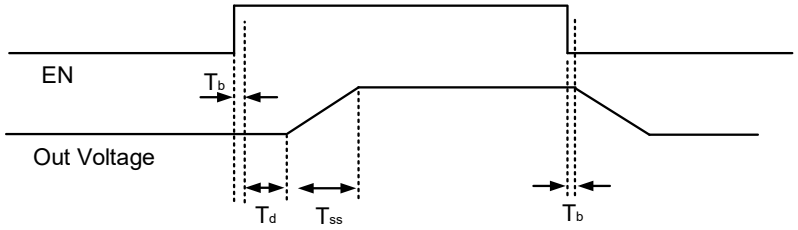


Figure 4. Soft-start and Shutdown

Over Current Protection and Short Circuit Protection (SCP)

The ET83201H protects an over current situation by limiting both the inductor both peak and valley current. The current of HS-FET and LS-FET are monitored all the time when the ET83201H is enabled. The HS-FET is turned off immediately when the peak current reaches the peak current limit and the HS-FET cannot be turned on if the LS-FET valley current is higher than the low-side valley current limit.

The SCP is realized by monitoring the inductor current whether is limited. Once the output load draws more current than the current limit, the output voltage drops. When the peak current limit is triggered for 32 switching cycles, the ET83201H shuts down, the LS-FET is kept on until the ZCD threshold is reached. A new soft-start begins after a typical 130μs wait time.

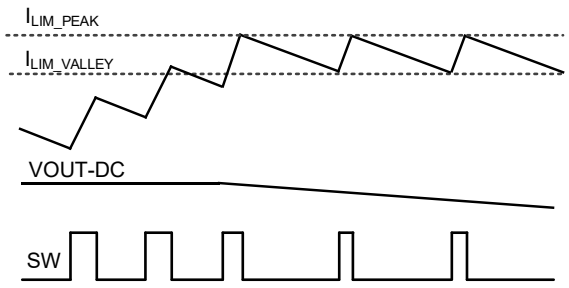


Figure 5. Current Limit

Output Active Discharge Function

The ET83201H sinks current from the SW pin when the device is shut down by EN. An internal discharge FET is turned on and the energy from the output capacitor is discharged to the ground. The typical resistance of the FET is 15Ω. The discharge function is disabled at below conditions:

1. During soft start
2. VIN UVLO threshold
3. Thermal shutdown

Power Good Indication (PG version only)

The Power Good (PG) pin is an open-drain output. Once the voltage of the FB pin rises above 93% of the

target output voltage, the PG detection is triggered and PG pin floats after a 20-μs deglitch time. A pullup resistor of 100 kΩ is recommended to pull the voltage up to VIN or VOUT. The PGD pin is pulled low when:

• FB pin voltage is lower than 90% of the target output voltage

• In a VIN UVLO, or thermal shutdown event

• During the soft-start period

• EN is pulled low

Thermal Protection

The ET83201H will shut down when the internal control circuit temperature is higher than 165°C and will restart after the temperature drops below 135°C as well.

Absolute Maximum Ratings

Symbol	Parameters (Items)	Value	Unit
V_{IN}	Supply voltage	-0.3 to 7	V
$V_{SW1(DC)}$	Switching node voltage (DC)	-0.3 to (V_{IN}+0.3V)	V
$V_{SW1(10ns)}$	Switching node voltage (10ns transient)	-3 to 10	V
	All other pins	-0.3 to 6	V
P_D	Continues power dissipation	0.6	W
T_J	Junction temperature	-40 to 150	°C
T_{Solder}	Maximum Soldering Temperature (at leads-10s)	260	°C
T_{STG}	Storage temperature	-55 to 150	°C

ESD Ratings

Symbol	Parameters (Items)	Value	Unit
HBM	Human body model, JS-001	±2000	V
CDM	Charged-device model, JESD22-C101	±1000	V

Thermal Characteristics

Symbol	Package	Parameters	Value	Unit
$R_{\theta JA}$	DFN1616	Junction-to-Ambient Thermal Resistance, JESD51-7	140	°C/W
	DFN1616	Measured on EVM, 2-layer, 2oz copper	80	°C/W
$R_{\theta JB}$	DFN1616	Junction-to-Bottom Thermal Resistance, JESD51-7	42	°C/W
$R_{\Theta jc(top)}$	DFN1616	Junction-to-Case Thermal Resistance, JESD51-7	53	°C/W

Recommended Operating Conditions

Symbol	Parameters	Min	Max	Unit
V_{IN}	Input voltage	2.4	6.0	V
V_{OUT}	Output voltage	0.6	VIN	V
T_A	Ambient temperature range	-40	85	°C
C_{IN}	Input decoupling capacitor, effective	4.7		μF
C_{OUT}	Output capacitor, effective	4.7	100	μF

Electrical Characteristics

The specifications are measured under conditions V_{IN} = 5V, T_J = 25°C, unless otherwise specified

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Input Section						
V_{ULVO}	Under voltage lockout threshold	Rising threshold	2.05	2.2	2.35	V
		Falling threshold	1.75	1.9	2.0	V
I_q	Input quiescent current	PFM, EN=VIN, FB=0.65V		40	55	μA
		Forced PWM, EN=VIN		0.5	2	mA
I_{IN_SD}	Input shutdown current	EN=0		0.1	2	μA
Power Stage						
I_{LIM_PEAK}	High-side peak current limit	T_J=25°C	2.5	3.5		A
I_{LIM_VAL}	Low-side valley current limit	T_J=25°C	2	2.7		A
R_{ON_HS-FET}	High-side FET on-resistance	V_{IN}=5V		110		mΩ
R_{ON_HS-FET}	Low-side FET on-resistance	V_{IN}=5V		83		mΩ
Control Circuits						
V_{ref}	Reference Voltage	25°C	0.594	0.6	0.606	V
		T_J=-40°C~-125°C	0.585	0.6	0.615	V
I_{leak_FB}	FB leakage current				0.1	μA
F_{sw}	Switching frequency			2.3		MHz
t_d[Note2]	EN delay time	From EN turn high to 1st switch		30		μs
t_{ss}[Note2]	Soft start time	5% to 90% of output voltage		0.35	0.6	ms
EN Logic						
V_H	Logic high	Rising threshold	0.9			V
V_L	Logic low	Falling threshold			0.3	V
R_{EN}	EN pull down resistor			1		MΩ
$R_{DIS-FET}$	Discharge FET resistance	EN=0, 10mA, From SW to GND		12	20	Ω
Power Good (PG version device only)						
V_{PG_rise}	PG UV threshold	FB Rising threshold	88	93	98	%
V_{PG_fall}		FB Falling threshold	86	91	96	%
R_{PGD}	PG pull down resistance	1mA, From SW to GND		8	15	Ω

Electrical Characteristics (Continued)

Symbol	**Parameters**	Conditions	Min	Typ	Max	Unit
Short Circuit Protection						
t_{SCP}[Note2]	SCP deglitch time			32		cycles
t_{HICCUP}[Note2]	Hiccup wait time			140		μs
Thermal Shutdown						
T_{jsd}	Thermal shutdown threshold	Rising threshold	155	165	175	°C
		Falling threshold		135		°C

Note2: Not production tested. Guaranteed by design.

Typical Characteristics

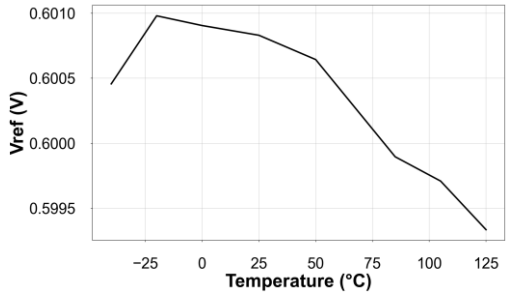


Figure 6. V_{ref} vs T_J

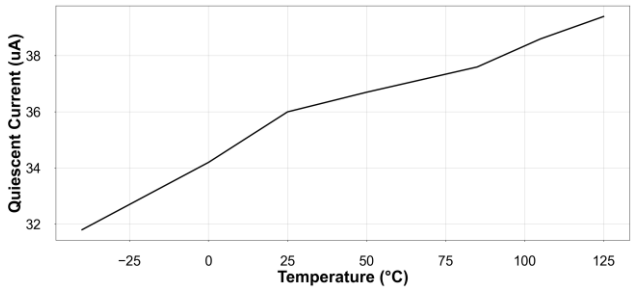


Figure 7. No Load Current vs T_J, EN=VIN

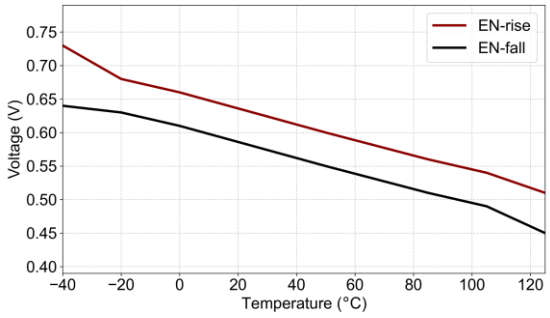


Figure 8. EN threshold vs T_J

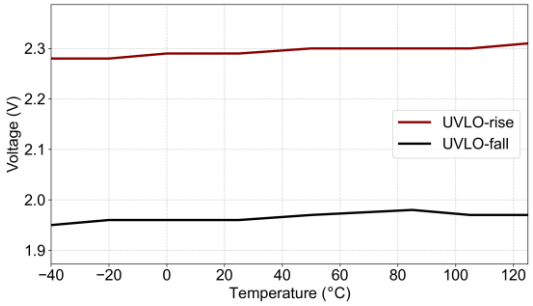


Figure 9. VIN UVLO threshold vs T_J

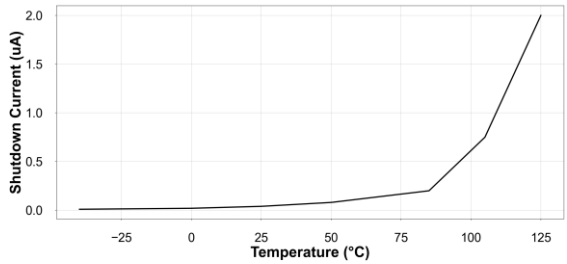


Figure 10. Shutdown Current vs T_J

Typical Characteristics

V_{IN} = 3.6V, 2.3MHz, HTTH25201T-1R0MTR-82 (1μH, DCR=21mΩ).

Cout=2*10μF, GRM155R60J106ME05D, (unless otherwise noted)

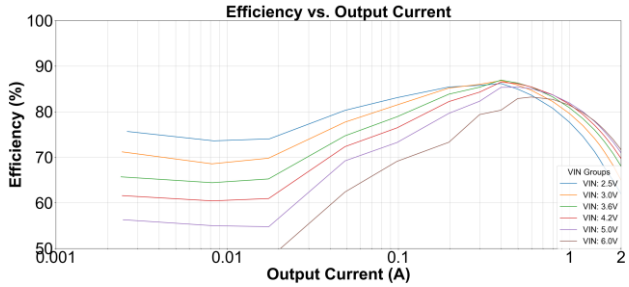


Figure 11. Efficiency vs Load Current, V_{OUT} = 0.9V

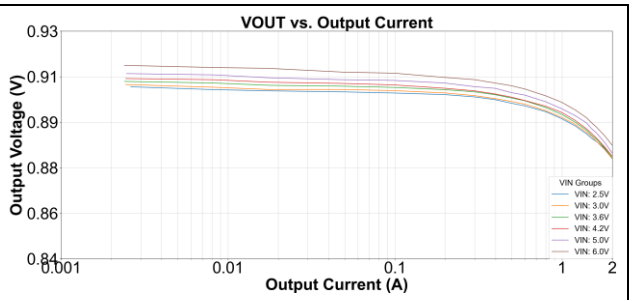


Figure 12. Load Regulation, V_{OUT} = 0.9V

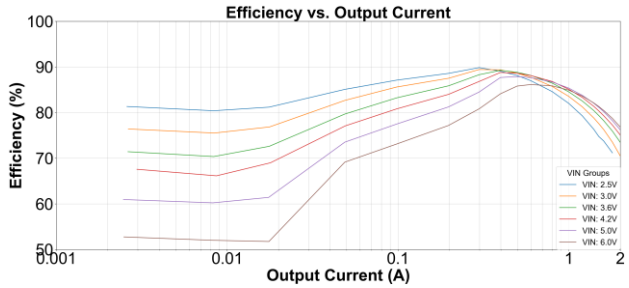


Figure 13. Efficiency vs Load Current, V_{OUT} = 1.2V

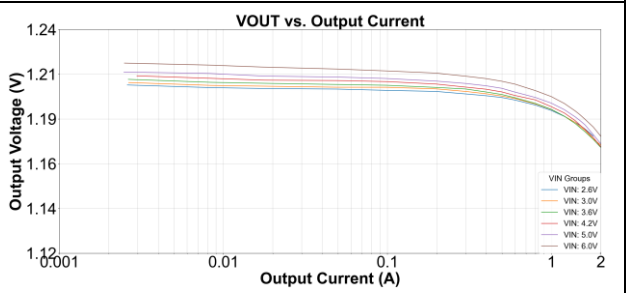


Figure 14. Load Regulation, V_{OUT} = 1.2V

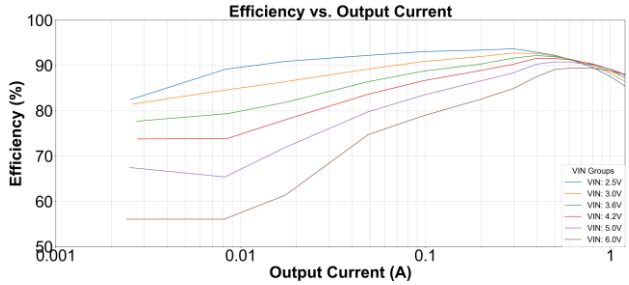


Figure 15. Efficiency vs Load Current, V_{OUT} = 1.8V

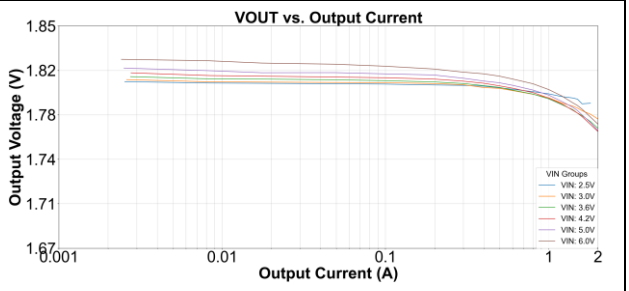


Figure 16. Load Regulation, V_{OUT} = 1.8V

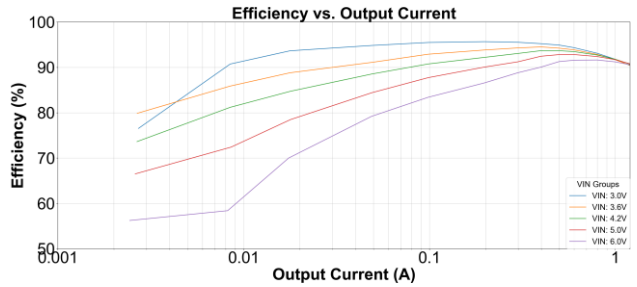


Figure 17. Efficiency vs Load Current, V_{OUT} = 2.5V

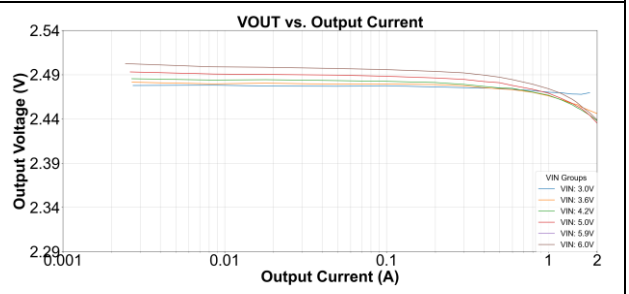


Figure 18. Load Regulation, V_{OUT} = 2.5V

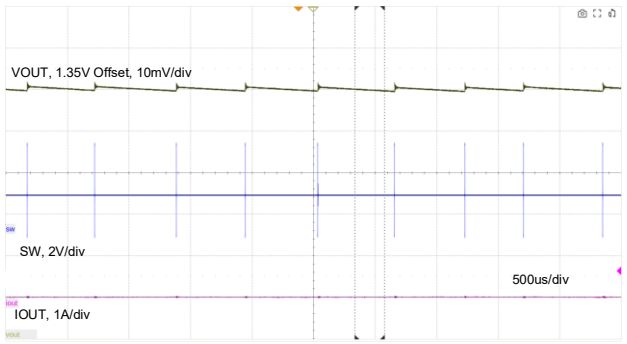


Figure 19. Output Ripple, No load

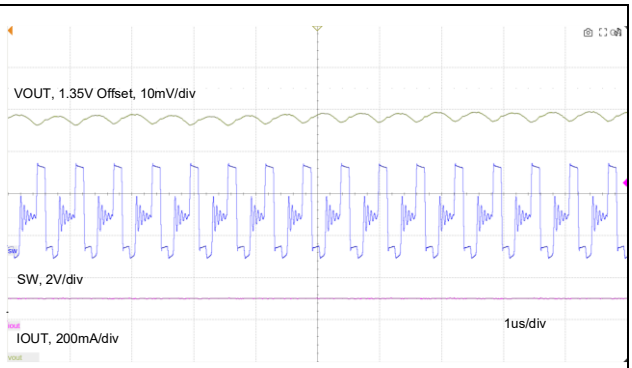


Figure 20. Output Ripple, 0.1A load

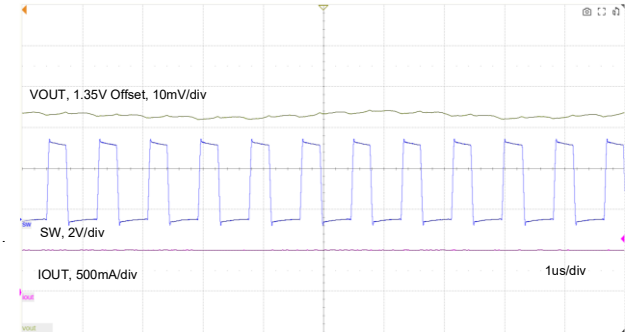


Figure 21. Output Ripple, 0.5A load

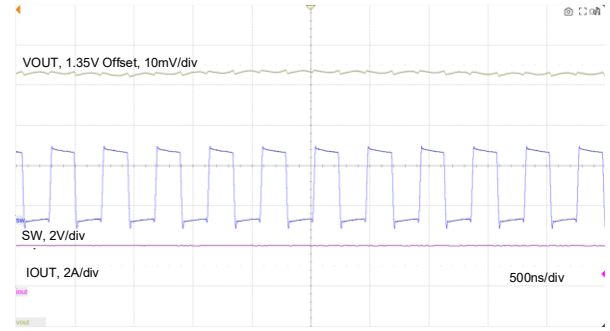


Figure 22. Output Ripple, 2A load

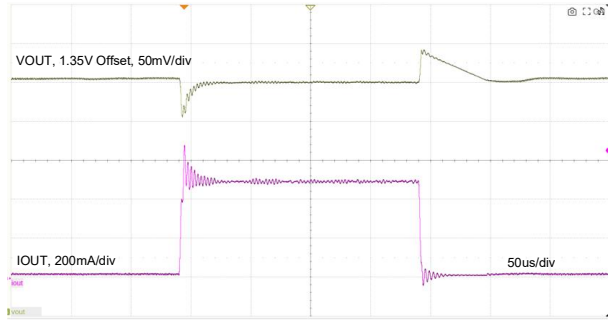


Figure 23. Load Transient,I_{OUT}=20mA to 0.5A,1A/μs

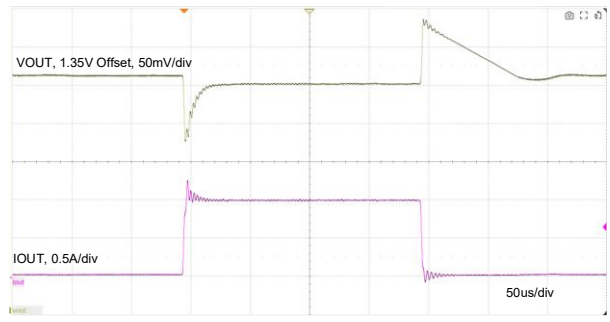


Figure 24. Load Transient, I_{OUT}=20mA to 1A, 1A/μs

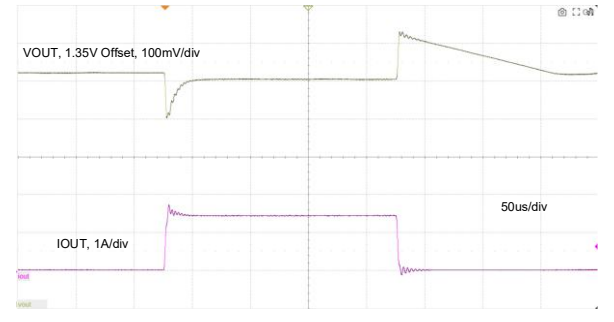


Figure 25. Load Transient,I_{OUT}=20mA to 1.5A,1A/μs

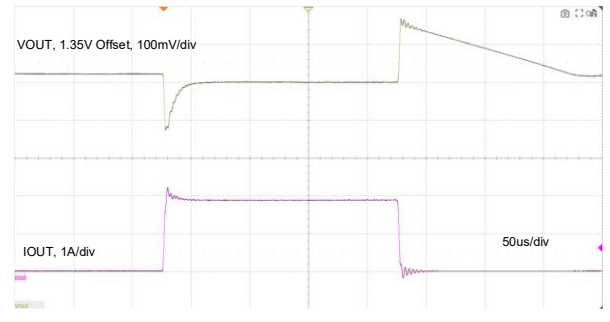


Figure 26. Load Transient, I_{OUT}=20mA to 2A, 1A/μs

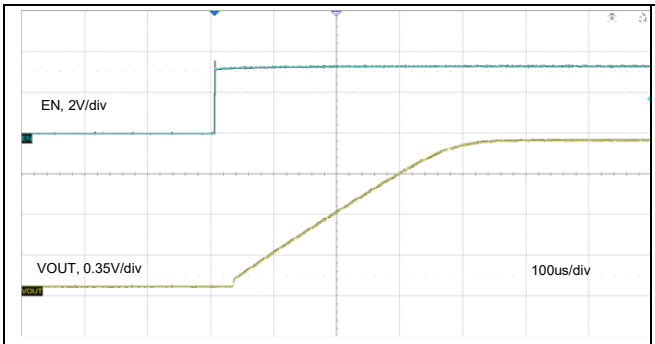


Figure 27. Startup by EN, No load

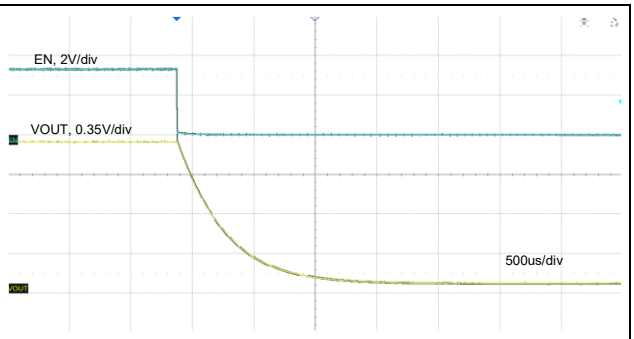


Figure 28. Shutdown by EN, No load

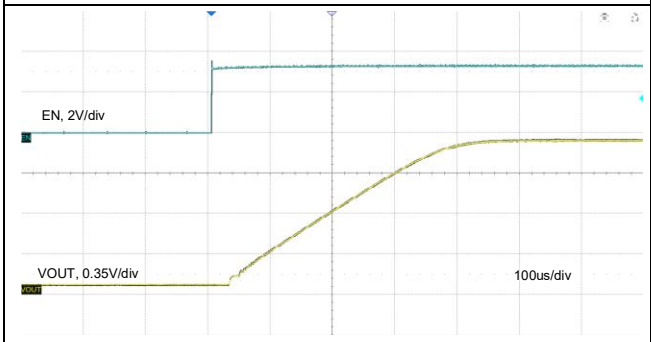


Figure 29. Startup by EN, 1Ω Load

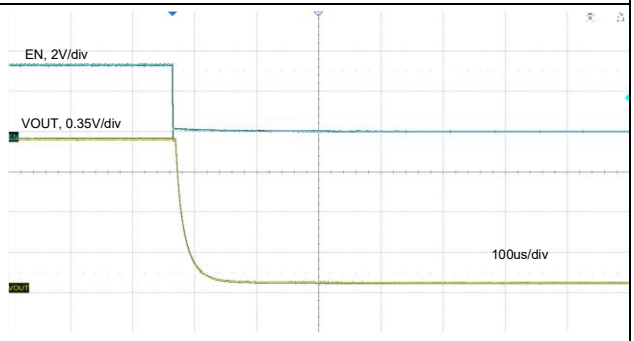


Figure 30. Shutdown by EN, 1Ω Load

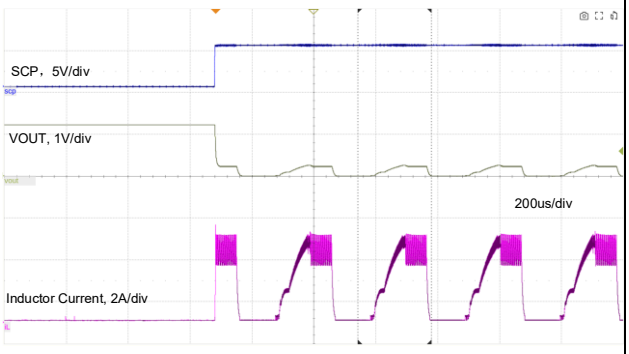


Figure 31. Short Circuit Protection

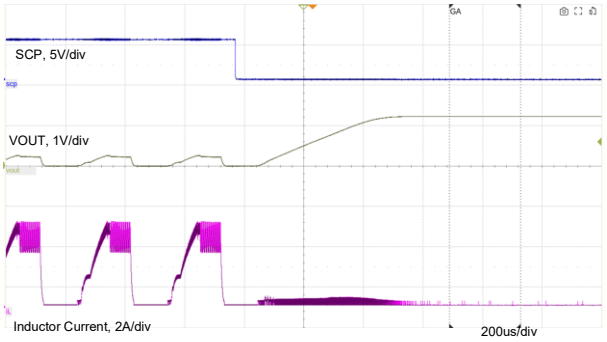
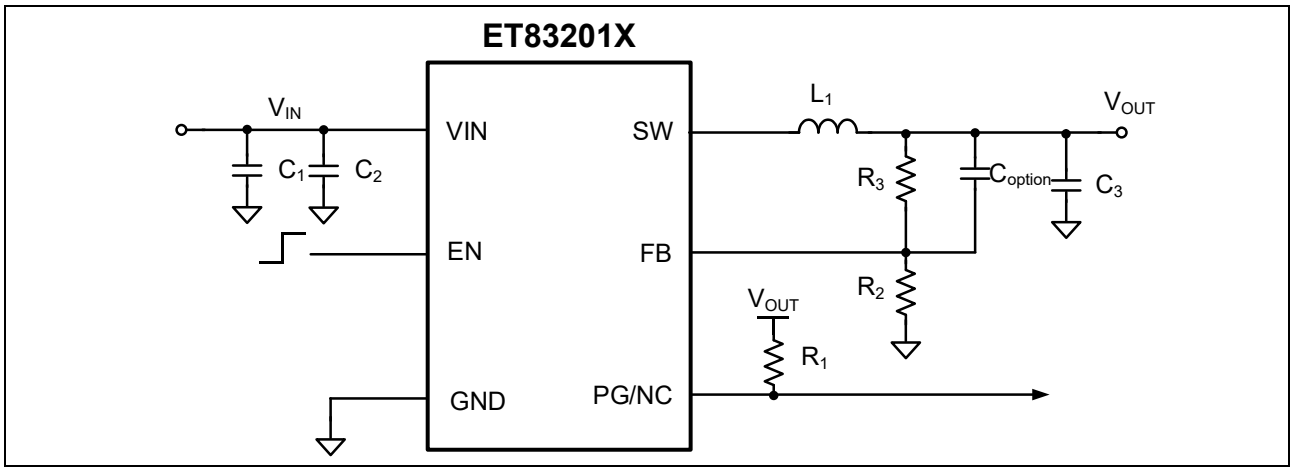


Figure 32. Short Circuit Protection, recovery

Application Circuit



Note*: This application circuit is for reference only.

The ET83201H is a highly-efficient, small, and highly-flexible synchronous step-down DC-DC converter that is easy to use. A typical system consists of a ET83201H IC, a power inductor L_1, and several resistors and capacitors as shown in the application circuit above.

Table II. Typical application of 1.8V output voltage

Symbol	Description	Recommended
L_1	1μH DCR=21mΩ, 2520	HTTH25201T-1R0MTR-82, Cyntec LTD. DFE252010P-1R0M, Murata (TOKO)
C_1, C_3	22μF, 6.3V, 0603	GRM188R61A226ME15, Murata
C_2	0.1μF, 10V, 0402	GRM022R61A104ME01, Murata
C_{option}	10~100pF, 0402	Reserved
R_1	100kΩ, ±5%, 0603	Std.
R_2	51kΩ, ±1%, 0603	Std.
R_3	100kΩ, ±1%, 0603	Std.

Output Voltage Setting

The output voltage of the ET83201H is adjustable. It can be programmed for output voltages from 0.6 V to 5.5 V, using a resistor divider from VOUT to GND. The voltage at the FB pin is regulated at 600 mV. The value of the output voltage is set by the selection of the resistor divider (R_2, R_3) from Table II. It is recommended to choose resistor values that allow a current higher than 50 times of FB pin leakage current, meaning the value of R2 should not exceed 100 kΩ. Lower resistor values are recommended for higher accuracy and lower noise at the cost of additional current consumption.

Inductor Selection

The inductor is a critical component, related to the efficiency, loop stability and transient response, etc. The ET83201H is designed for a nominal 1-μH inductor. Smaller values than nominal inductance cause larger inductor current ripple, which cause larger negative inductor currents in forced PWM mode and higher peak currents at full load.

$$I_{Lp2p} = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{V_{IN} * L * f_{SW}}$$

Please make sure the minimum peak current is higher than 150mA any time.

Capacitor Selection

The input capacitor not only serves as the power supply of the ET83201H, but also filters the high-frequency noise when switching. A 22μF input capacitor is recommended to serve as the bulk input, an additional 0.1~1μF 0201 small size capacitor is strongly recommended to be placed in parallel with the bulk capacitor to filter out the noise.

The output capacitor is another critical component, related to the loop stability and transient response as well. The table lists the typical capacitor and inductor selection and please consider the voltage derating effect when selecting Muti-layer ceramic capacitor (MLCC). At least one 22μF output capacitor should be soldered to guarantee stability. More output capacitors are good for better loop stability and transient performance.

The ET83201H supports 0.47μH and 2.2μH inductors as well, but the light load efficiency is impacted with 0.47μH and transient performance is impacted with 2.2μH inductor. Please verify the efficiency and transient behavior before selecting different inductance components.

Table III. Recommended Inductor and Output Capacitor

Output Voltage	FSW	L	COUT
0.6V	2.4MHz	0.47/1μH	⩾22μF*2
1.2V	2.4MHz	0.47/1μH	10μF*2
1.8V	2.4MHz	0.47/1μH	10μF*2
3.3V	2.4MHz	0.47/1μH	10μF*2

PCB Layout Guide

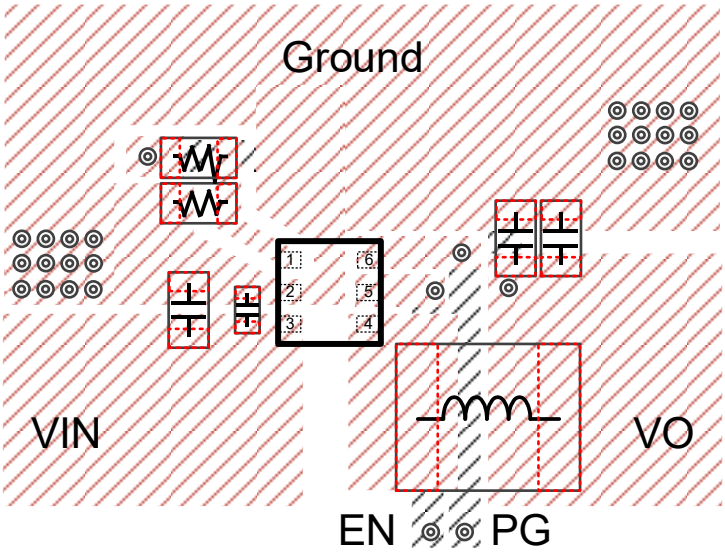


Figure 33 Layout example (Top Layer)

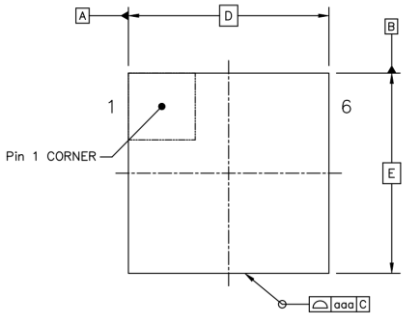
Please follow this specific order carefully to achieve the proper layout.

- Place input capacitor C_1 as close as possible to VIN pin and GND pin and use shortest copper trace connection or ground plane.
- Put output capacitor C_2 near to the inductor output terminal and the device. Ground connections need to

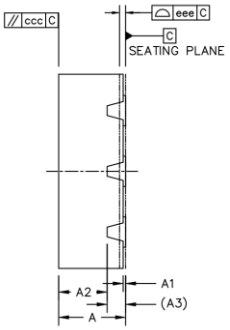
be tied to the IC ground with a short copper trace or ground plane.

- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
- At least 2-layer PCB is recommended and with 2-oz thickness copper to achieve good thermal performance.

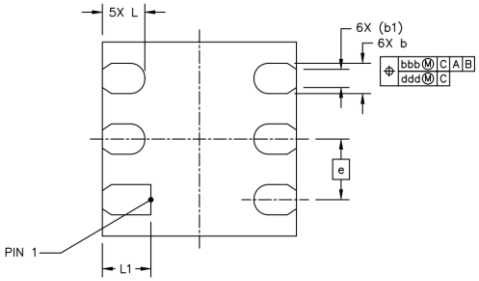
Package Dimension (DFN1616)



Top View



Side View

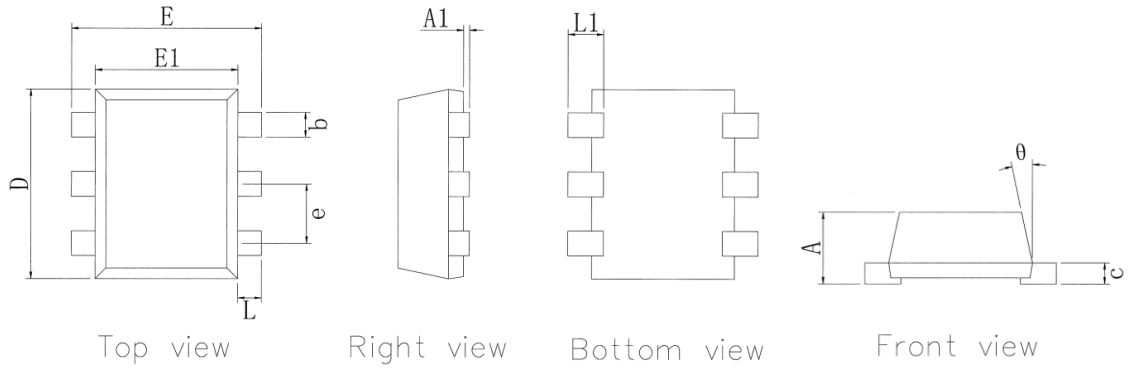


Bottom View

Dimensions Table (Units: mm)

Symbol	Min	Nom	Max
A	0.5	0.55	0.6
A1		0.02	
A2		0.4	
A3		0.152 REF	
b	0.20	0.25	0.30
b1		0.15 REF	
D		1.60 BSC	
E		1.60 BSC	
e		0.50 BSC	
L	0.30	0.35	0.40
L1	0.35	0.40	0.45
aaa		0.1	
bbb		0.1	
ccc		0.1	
ddd		0.05	
eee		0.05	

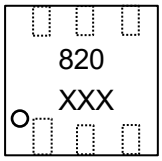
Package Dimension (SOT563)



Dimensions Table (Units: mm)

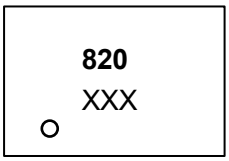
Symbol	Min	Nom	Max
A	0.530		0.600
A1	0.000		0.050
b	0.170		0.270
c	0.110		0.160
D	1.500	1.600	1.700
E	1.500	1.600	1.700
E1	1.100	1.200	1.300
e	0.500 BSC		
L	0.10	0.20	0.30
L1	0.200	0.300	0.400
θ	11°	12°	13°

Marking (DFN1616)



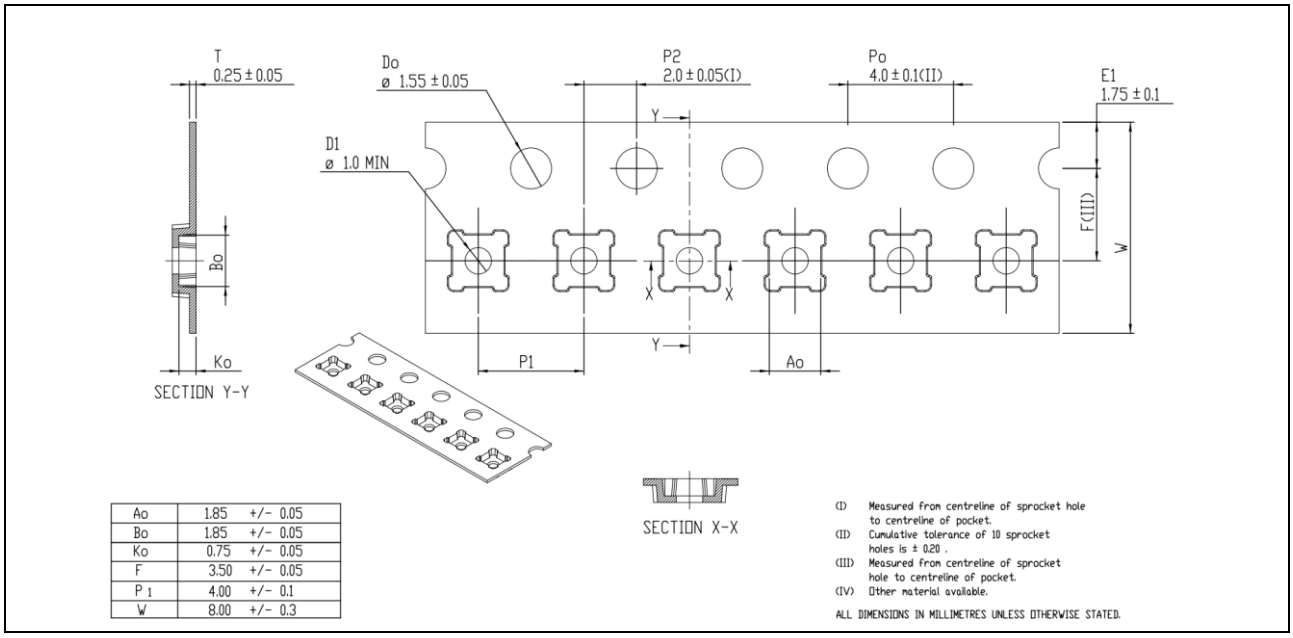
XXX = Tracking Number

Marking (SOT563)

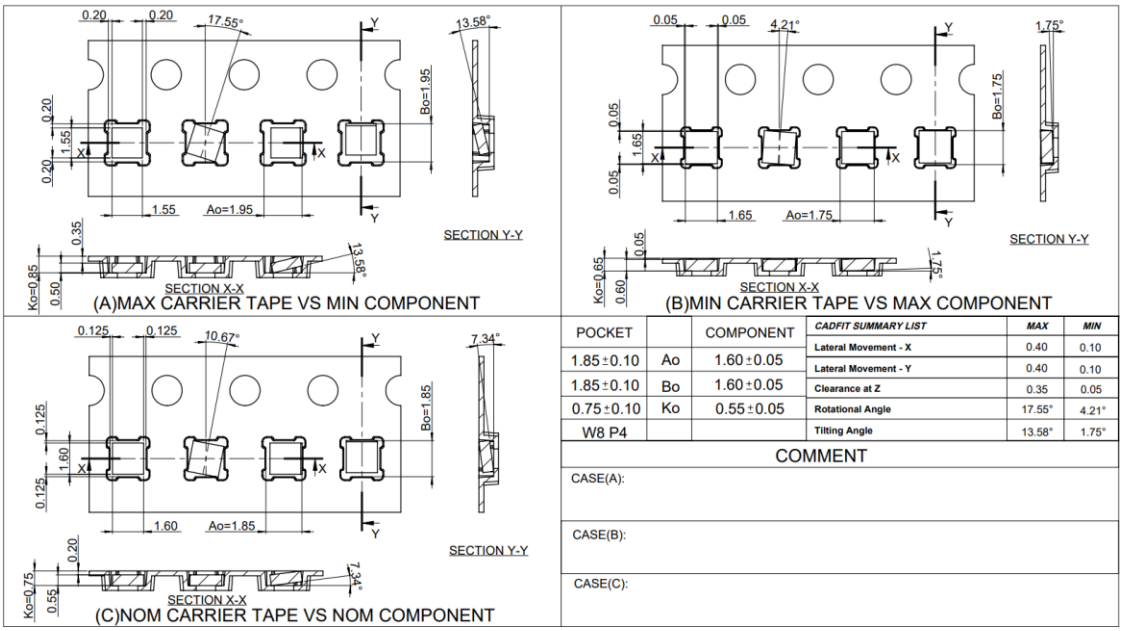


XXX = Tracking Number

Tape Information



Ao	1.85	+/- 0.05
Bo	1.85	+/- 0.05
Ko	0.75	+/- 0.05
F	3.50	+/- 0.05
P 1	4.00	+/- 0.1
W	8.00	+/- 0.3



POCKET		COMPONENT	CADFIT SUMMARY LIST	MAX	MIN
1.85±0.10	Ao	1.60±0.05	Lateral Movement - X	0.40	0.10
1.85±0.10	Bo	1.60±0.05	Lateral Movement - Y	0.40	0.10
0.75±0.10	Ko	0.55±0.05	Clearance at Z	0.35	0.05
W8 P4			Rotational Angle	17.55°	4.21°
			Tilting Angle	13.58°	1.75°

COMMENT

CASE(A):

CASE(B):

CASE(C):

Unit: mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025.6.20	First Release	Charles Wong		
1.1	2025.09.30	Update waveform	Charles Wong		
1.2	2026.6.30	UVLO falling change to 2V max	Charles Wong		