# High-Speed USB 2.0 480Mbps Switch

## General Description

The ET7227 is a double-pole/double-throw (DPDT) switches. Their wide bandwidth and low bit-to-bit skew allow them to pass high-speed differential signals with good signal integrity.

Each switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. Industry-leading advantages include a propagation delay of less than 250 ps, resulting from its low channel resistance and low I/O capacitance. Their high channel-to-channel crosstalk rejection results in minimal noise interference. Their bandwidth is wide enough to pass High-Speed USB 2.0 differential signals (480 Mb/s).

ET7227 is offered in a MSOP10 package.

## Features

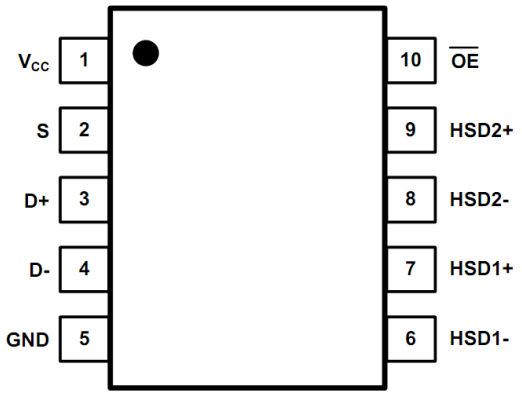
- $R_{ON}$ is typically 6.0 Ω @ $V_{CC}$ = 3.3 V
- Low Bit-to-Bit skew is typically 50 ps
- Low current consumption is 1.0 μA typical
- Near-zero propagation delay is typical 250 ps
- Channel on-capacitance is 8.0 pF typical
- $V_{CC}$ operating range from 1.65 V to 4.5 V
- Part No. and package

| Part No. | Package | Packing Option | MSL |
|---|---|---|---|
| ET7227U | MSOP10(4.9 mm×3.0 mm) | Tape and Reel ,4K | Level 3 |

## Applications

- Differential Signal Data Routing
- USB 2.0 Signal Routing

## Pin Configuration




Top View

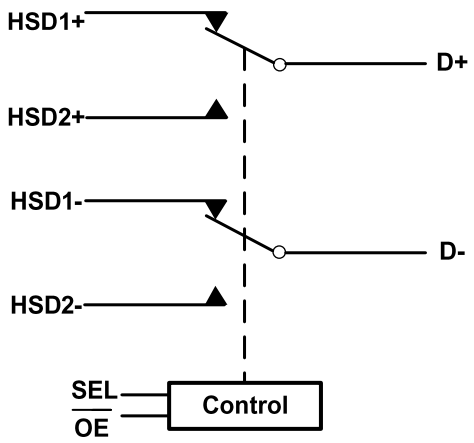
## Pin Function

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 3 | D+ | Data Ports |
| 4 | D- | Data Ports |
| 5 | GND | Ground |
| 6 | HSD1- | Data Ports |
| 7 | HSD1+ | Data Ports |
| 8 | HSD2- | Data Ports |
| 9 | HSD2+ | Data Ports |
| 10 | $\overline{OE}$ | Output Enable |
| 1 | VCC | Power supply |
| 2 | S | Select Input |

## Truth Table

| $\overline{OE}$ | S | HSD1+ to D+, HSD1- to D- | HSD2+ to D+, HSD2- to D- |
|---|---|---|---|
| 1 | X | OFF | OFF |
| 0 | 0 | ON | OFF |
| 0 | 1 | OFF | ON |

## Analog Symbol




Analog Symbol

## Absolute Maximum Ratings

| Symbol | Pins | Parameters | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | VCC | Positive DC Supply Voltage | -0.5 to +6.0 | V |
| $V_{IS}$ | HSD1+,HSD1-,HSD2+,HSD2- | Analog Signal Voltage | -0.5 to $V_{CC}$ | V |
| | D+,D- | | -0.5 to +5.5 | |
| $V_{IN}$ | $\overline{OE}$ | Control Input Voltage | -0.5 to +6.0 | V |
| $I_{CC}$ | VCC | Positive DC Supply Current | 50 | mA |
| $T_{STG}$ | | Storage Temperature | -65 to +150 | ˚C |
| $I_{IS_CON}$ | HSD1+,HSD1-,HSD2+,HSD2- D+,D- | Analog Signal Continuous Current | ±100 | mA |
| $I_{IS_PK}$ | HSD1+,HSD1-,HSD2+,HSD2- D+,D- | Analog Signal Continuous Current 10% Duty Cycle | ±150 | mA |
| $I_{IN}$ | $\overline{OE}$ | Control Input Current | ±20 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## Recommended Operating Conditions

| Symbol | Pins | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | VCC | Positive DC Supply Voltage | 1.65 | 4.5 | V |
| $V_{IS}$ | HSD1+,HSD1-,HSD2+,HSD2- | Analog Signal Voltage | GND | $V_{CC}$ | V |
| | D+,D- | | GND | 4.5 | |
| $V_{IN}$ | $\overline{OE}$ | Digital Select Input Voltage | GND | $V_{CC}$ | V |
| $T_A$ | | Operating Temperature Range | -40 | +85 | ˚C |

Minimum and maximum values are guaranteed through test or design across the Recommended Operating Conditions, where applicable. Typical values are listed for guidance only and are based on the particular conditions listed for section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

## DC Electrical Characteristics

**Control Input** (Typical: $T_A$ = 25 °C, $V_{CC}$ = 3.3 V)

| Symbol | Pins | Parameter | Test Conditions | $V_{CC}$ (V) | -40°C to +85°C | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{IH}$ | S<br>$\overline{OE}$ | Control Input High Voltage[(1)] | | 2.7<br>3.4<br>4.2 | 1.0<br>1.1<br>1.12 | - | - | V |
| $V_{IL}$ | S<br>$\overline{OE}$ | Control Input Low Voltage[(1)] | | 2.7<br>3.4<br>4.2 | - | | 0.4<br>0.4<br>0.5 | V |
| $I_{IN}$ | | Control Input Leakage Current | 0 ≤ $V_{IS}$ ≤$V_{CC}$ | 1.65 ~ 4.5 | - | - | ±1.0 | μA |

***Note1:*** $V_{IH}$ level is recommended to be consistent with $V_{CC}$ and $V_{IL}$ level is GND to reduce $I_{CC}$ current.

**Supply And Leakage Current** (Typical: $T_A$ = 25 °C, $V_{CC}$ = 3.3 V, $\overline{OE}$ = $V_{CC}$ or GND, S = $V_{CC}$ or GND)

| Symbol | Pins | Parameter | Test Conditions | $V_{CC}$ (V) | -40°C to +85°C | | unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| $I_{CC}$ | $V_{CC}$ | Quiescent Supply Current | $V_{IS}$ = $V_{CC}$ or GND; $I_{OUT}$ = 0A | 1.65 ~ 4.5 | - | 1.0 | μA |
| $I_{CCT}$ | $V_{CC}$ | Increase in $I_{CC}$ per Control Voltage | $V_{IN}$ = 2.6V | 3.6 | - | 10 | μA |
| $I_{OZ}$ | HSD1+<br>HSD1-<br>HSD2+<br>HSD2- | OFF Stage Leakage Current | 0 ≤ $V_{IS}$ ≤ $V_{CC}$ | 1.65 ~ 4.5 | - | ±1.0 | μA |
| $I_{OFF}$ | D+, D- | Power OFF Leakage Current | 0 ≤ $V_{IS}$ ≤ 4.5V | 0 | - | ±1.0 | μA |

**High Speed On Resistance** (Typical: $T_A$ = 25 °C, $V_{CC}$ = 3.3 V)

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | -40°C to +85°C | | | unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $R_{ON}$ | On-Resistance | $V_{IS}$ = 0.2V, 0.4V<br>$I_{ON}$ = 8mA | 2.7 | - | 6.5 | 12 | Ω |
| | | | 3.3 | | 6.0 | 10 | |
| | | | 4.2 | | 5.5 | 8 | |
| $R_{FLAT}$ | On-Resistance Flatness | | 2.7 | - | 0.3 | 1.5 | Ω |
| | | | 3.3 | | 0.2 | 1 | |
| | | | 4.2 | | 0.1 | 0.5 | |
| $\triangle R_{ON}$ | On-Resistance Matching | | 2.7 | - | 0.25 | 0.5 | Ω |
| | | | 3.3 | | 0.2 | 0.45 | |
| | | | 4.2 | | 0.15 | 0.4 | |

**Full Speed On Resistance** (Typical: $T_A$ = 25 °C, $V_{CC}$ = 3.3 V)

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | -40°C to +85°C | | | unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $R_{ON}$ | On-Resistance | $V_{IS}$ = 0.2$V_{CC}$,0.5$V_{CC}$,<br>0.8$V_{CC}$, $V_{CC}$<br>$I_{ON}$ = 8mA | 2.7 | - | 9.0 | 13 | Ω |
| | | | 3.3 | | 7.5 | 11 | |
| | | | 4.2 | | 6.0 | 9 | |
| $\triangle R_{ON}$ | On-Resistance Matching | | 2.7 | - | 0.5 | 0.8 | Ω |
| | | | 3.3 | | 0.4 | 0.7 | |
| | | | 4.2 | | 0.3 | 0.6 | |
| $R_{FLAT}$ | On-Resistance Flatness | $V_{IS}$ = 0.2V,0.4V,<br>0.7V,1.0V<br>$I_{ON}$ = 8mA | 2.7 | - | 1.0 | 3 | Ω |
| | | | 3.3 | | 0.5 | 1.5 | |
| | | | 4.2 | | 0.4 | 1.2 | |

## AC Electrical Characteristics(2)

**Timing / Frequency** (Typical: $T_A$ = 25 °C, $V_{CC}$ = 3.3 V, $R_L$ = 50 Ω, $C_L$ = 5 pF)

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | -40°C to +85°C | | | unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $t_{ON}$ | Turn-ON Time | | 2.7 ~ 4.5 | - | 14 | 20 | ns |
| $t_{OFF}$ | Turn-OFF Time | | 2.7 ~ 4.5 | - | 21 | 25 | ns |
| $t_{BBM}$ | Break-Before-Make Delay | $V_{IS}$ = 0V to $V_{CC}$ | 2.7 ~ 4.5 | 2 | 8 | - | ns |
| BW | -3 dB Bandwidth | $C_L$ = 5pF | 2.7 ~ 4.5 | - | 550 | - | MHz |
| | | $C_L$ = 0pF | | - | 900 | - | |

**Isolation** (Typical: $T_A$ = 25 °C, $V_{CC}$ = 3.3 V, $R_L$ = 50 Ω, $C_L$ = 5 pF)

| Symbol | Pins | Parameter | Conditions | $V_{CC}$ (V) | -40°C to +85°C | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $O_{IRR}$ | Open | OFF-Isolation | f = 250MHz | 1.65 ~ 4.5 | - | -30 | - | dB |
| $X_{TALK}$ | HSD1+ to HSD1- | Non-Adjacent Channel Crosstalk | f = 250MHz | 1.65 ~ 4.5 | - | -45 | - | dB |

**Capacitance** (Typical: $T_A$ = 25 °C, $V_{CC}$ = 3.3 V, f = 1 MHz)

| Symbol | Pins | Parameter | Conditions | $V_{CC}$ (V) | -40°C to +85°C | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $C_{IN}$ | $\overline{OE}$ | Control Pin Input Capacitance | | 0 | | 1.8 | | pF |
| $C_{ON}$ | D+ to HSD1/2+ | ON Capacitance | $V_{OE}$= 0V | 3.3 | | 8.0 | | pF |
| $C_{OFF}$ | HSD2+, HSD2- | OFF Capacitance | $V_{IS}$ = 3.3V<br>$V_{OE}$= 3.3V | 3.3 | | 3.5 | | pF |

***Note2:*** AC parameter is guaranteed by design.

## Typical Characteristics

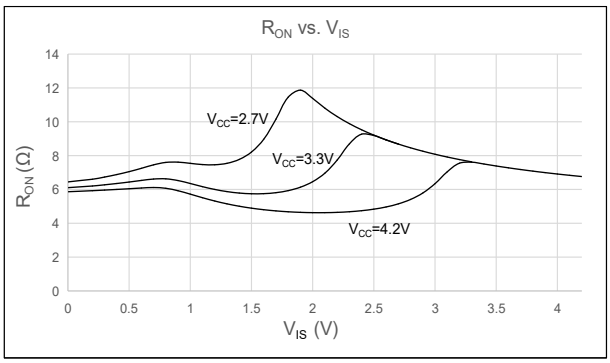



Figure 1. On-Resistance vs. $V_{IS}$

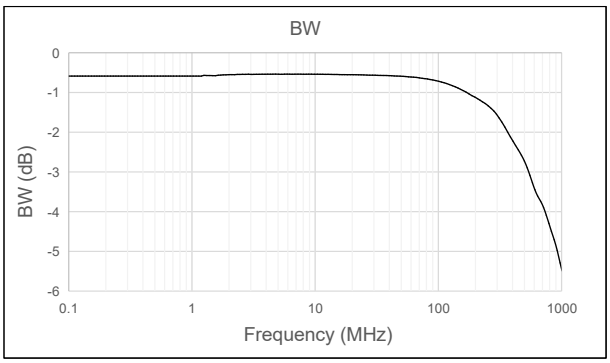



Figure 2. Bandwidth vs. Frequency @$V_{CC}$=3.3V

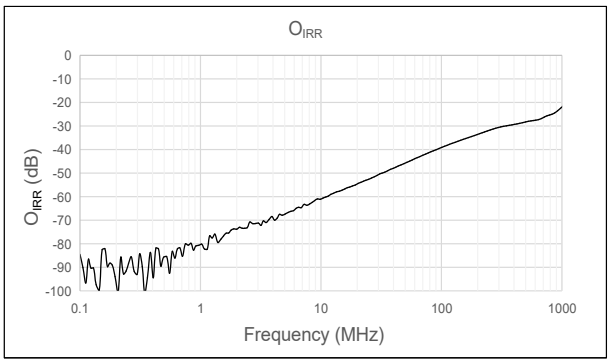



Figure 3. $O_{IRR}$ vs. Frequency @$V_{CC}$=3.3V

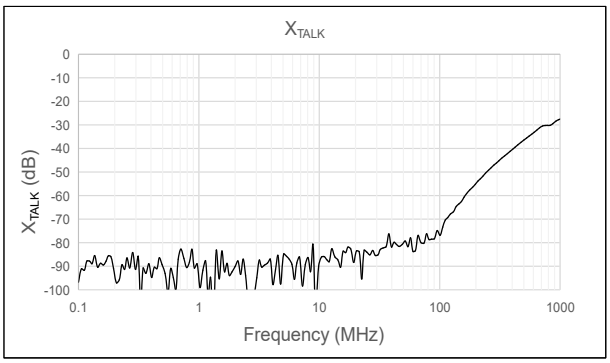



Figure 4. $X_{TALK}$ vs. Frequency @$V_{CC}$=3.3V

## Test Circuit and Waveform

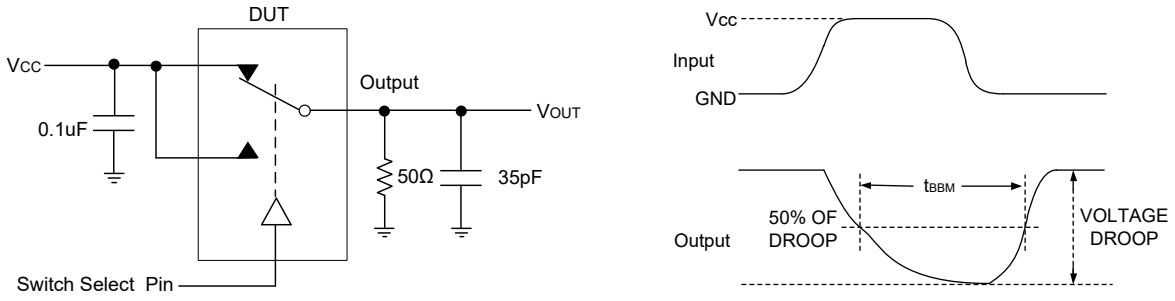



Figure 5. $t_{BBM}$ (Time Break-Before-Make)

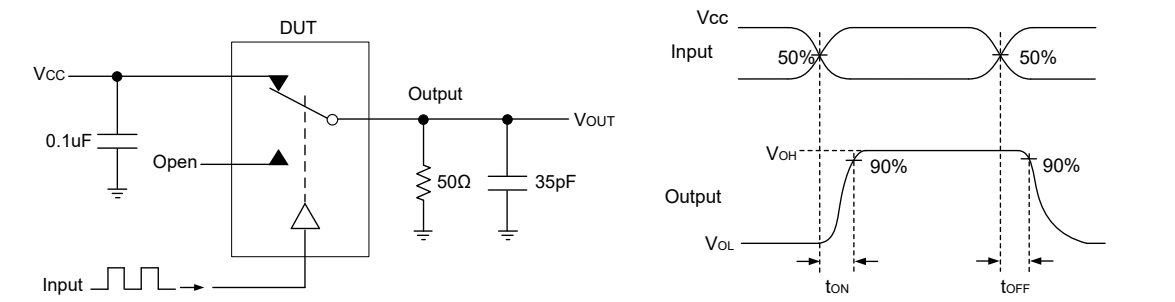



Figure 6. $t_{ON}$ / $t_{OFF}$

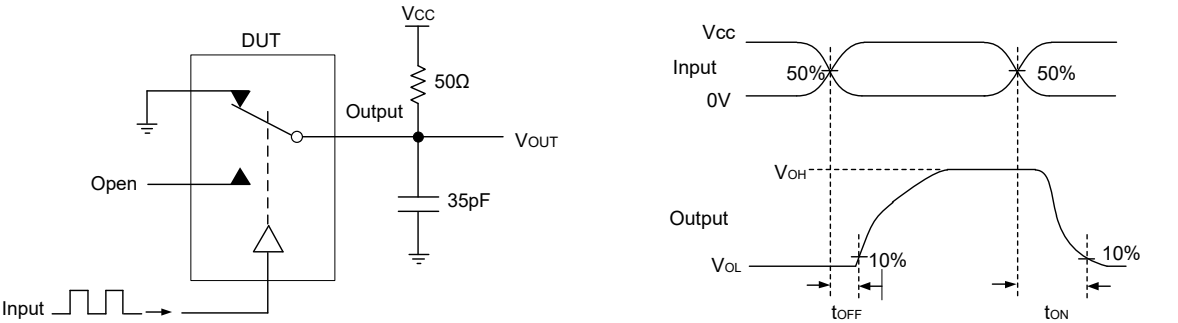



Figure 7. $t_{ON}$ / $t_{OFF}$

## Test Circuit and Waveform(Continued)

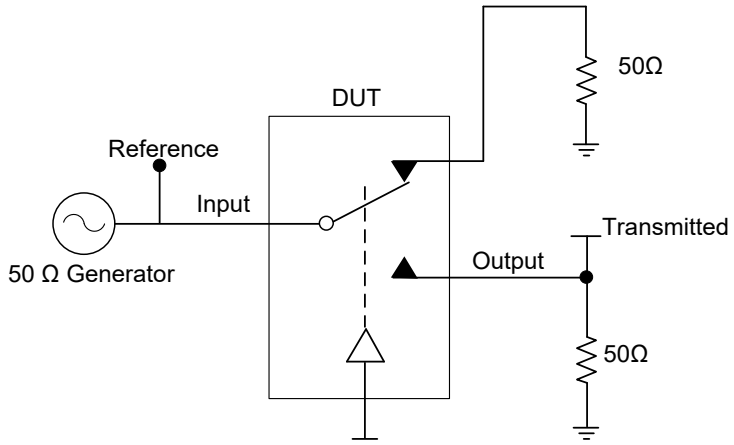



Figure 8. Off Channel Isolation/On Channel Loss(BW)/Crosstalk

(On Channel to Off Channel)/$V_{ONL}$

Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. $V_{ISO}$, Bandwidth and $V_{ONL}$ are independent of the input signal direction.

$V_{ISO}$ = Off Channel Isolation = $20 \text{ Log}\left(\frac{V_{OUT}}{V_{IN}}\right)$ for $V_{IN}$ at 100 kHz.

$V_{ONL}$ = On Channel Loss = $20 \text{ Log}\left(\frac{V_{OUT}}{V_{IN}}\right)$ for $V_{IN}$ at 100 kHz to 50 MHz.

Bandwidth (BW) = the frequency 3 dB below $V_{ONL}$.

$V_{CT}$ = Use $V_{ISO}$ setup and test to all other switch analog input/outputs terminated with 50 Ω.

## Typical Performance Curves

$T_A$ = +25 °C, Unless Otherwise Specified (Continued)

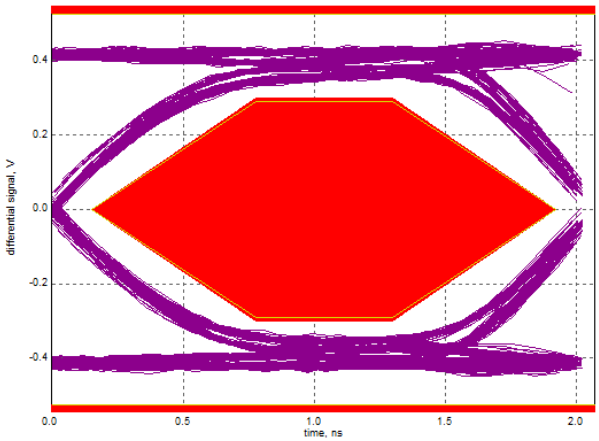
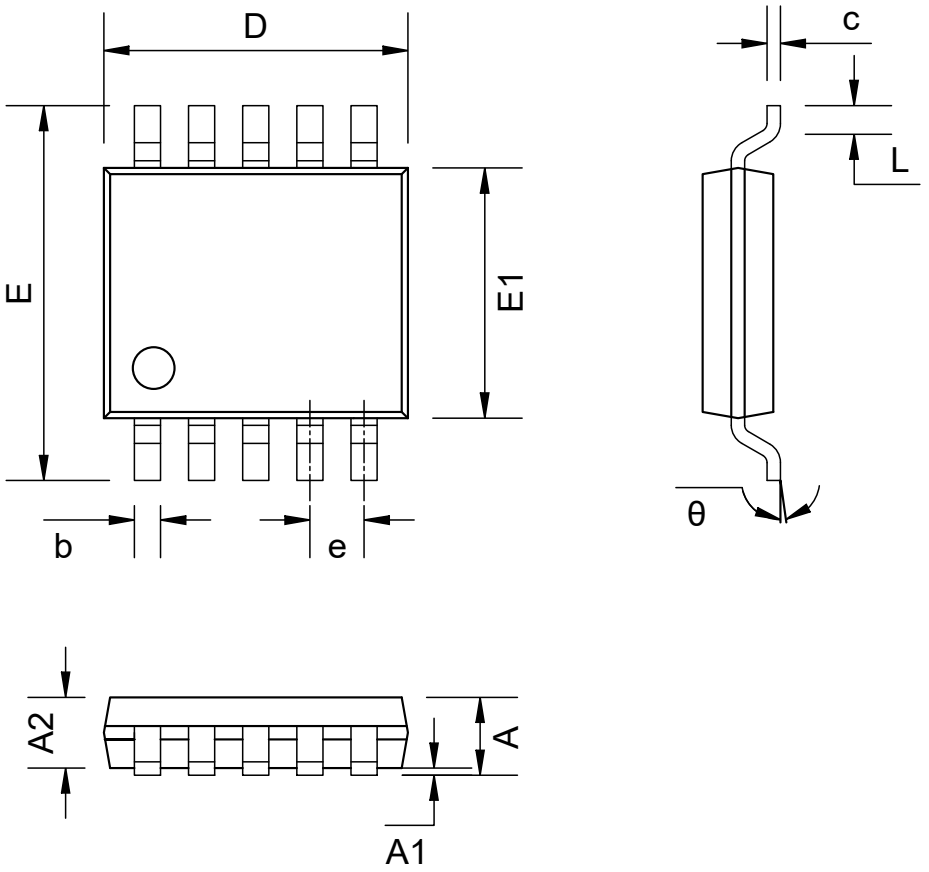



Figure 9. Eye Pattern : 480 Mbps with USB Switches the Signal Path (near end mask)

## Package Dimension

MSOP10




COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.82 | 0.95 | 1.10 |
| A1 | 0.02 | 0.07 | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| b | 0.18 | 0.23 | 0.28 |
| c | 0.09 | 0.16 | 0.23 |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.75 | 4.90 | 5.05 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | 0.50 TYP | | |
| L | 0.40 | | 0.80 |
| θ | 0° | | 6° |

## Revision History and Checking Table

| Version | Date | Revision Item | Modifier | Function & Spec Checking | Package & Tape Checking |
|---|---|---|---|---|---|
| 1.0 | 2015-09-20 | Original Version | Liu Xiao Min | Liu Xiao Min | Zhu Jun Li |
| 1.1 | 2022-11-15 | Update Typeset | Qinpl | Qinpl | Liujy |
| 1.2 | 2025-09-15 | 1、Update Typical Characteristics and Eye Pattern<br>2、Typo correction | Qinpl | Luh | Liujy |