7-Channel, 3.1~20V Input Voltage, High Integration power management IC

General Description

The ET598S6 is a highly integrated PMIC (Power Management IC) that integrates a 4-channel synchronous buck converter, 2-channel LDO, and 1-channel reset monitor. Its wide input voltage range, high efficiency, and high load driving capability provide a complete power supply solution for system design. In applications, it only requires a very small number of external components and has the characteristics of low power consumption and simple and convenient use. The integrated converter and built-in FET (Field Effect Transistor) have low impedance and are optimized for high-efficiency application scenarios (greater than 92%).

The ET598S6 has rich built-in protection functions, such as over-voltage protection, under-voltage protection, over-current protection, short circuit protection, over-temperature protection, etc. Which further improves its reliability in applications.

The ET598S6 is available in an QFN28L package.

Features

- 3.1V to 20V Input Voltage Range
- High Efficiency DC/DC Converter: Efficiency of 92% to 96%
- High Integration: 7-Channel Output Integrated on a Single Chip
- Buck DC/DC Converter (4-Channel)
  - -- HV BUCK1: Input 3.1V to 20V, Output 0.6V to V_{IN} Adjustable, Load Current up to 3A
  - -- HV BUCK2: Input 3.1V to 20V, Output 0.6V to V_{IN} Adjustable, Load Current up to 3A
  - -- LV BUCK1: Input 2.5V to 6V, Output 0.6V to V_{IN} Adjustable, Load Current up to 3A
  - -- LV BUCK2: Input 2.5V to 6V, Output 0.6V to V_{IN} Adjustable, Load Current up to 3A
- High PSRR LDO (2-Channel)
  - -- LDO1: Fixed 1.8V Output Voltage, Load Current up to 800mA
  - -- LDO2: Output Adjustable from 0.6V to 5.0V, Load Current up to 1000mA
- Reset monitor (1-Channel)
  - -- Provide POR Reset Signal to the Host Processor Through External Pull-up Voltage
- Multiple Protection Function
  - -- Over Current Protection Function
  - -- Short Circuit Protection Function
  - -- Over Voltage Protection Function

-- Under Voltage Protection Function

-- Over Temperature Protection Function

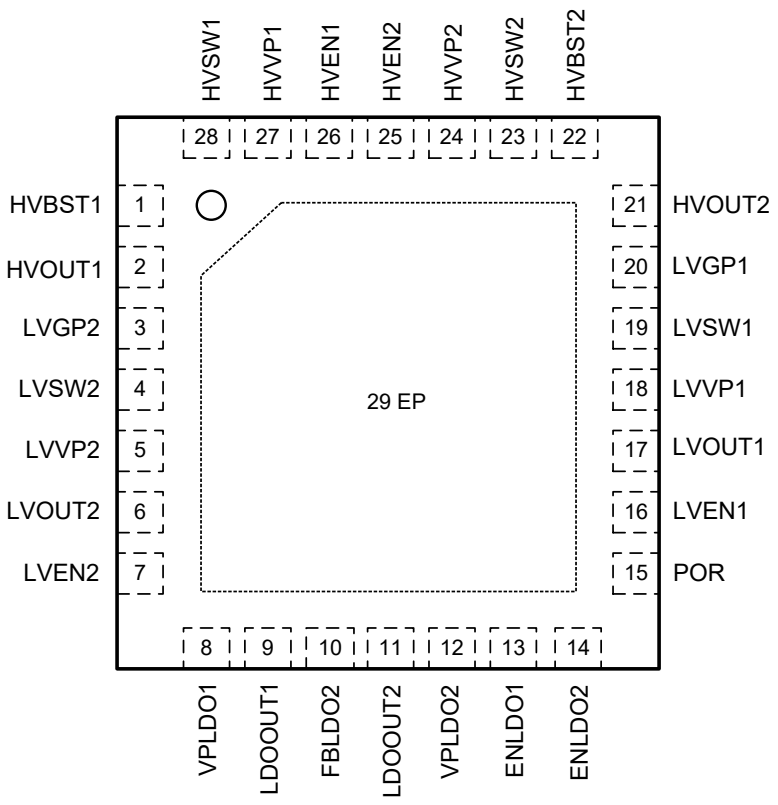
- Package:

Part No.	Package
ET598S6	QFN28L(4mm×4mm)

Applications

- Microprocessor
- Solid-State Drive
- PC, Server, Embedded System

Pin Configuration



Top View

Pin Function

Pin No.	Pin Name	Pin Function
HVBST1	1	Bootstrap Pin. The positive power supply pole of the MOSFET driver transistor with internal floating high side drive. Connect a 22nF bypass capacitor between this pin and HVSW1.
HVOUT1	2	HVBUCK1 Feedback Pin. Set the output voltage of the resistor divider from the output node to the feedback pin.
LVGP2	3	Ground.
LVSW2	4	LVBUCK2 Switch Pin. Connect this pin to an inductor to minimize the routing area and reduce EMI.
LVVP2	5	LVBUCK2 Power Pin. Connect a 10uF bypass capacitor to GND to reduce input noise.
LVOUT2	6	LVBUCK2 Feedback Pin. Set the output voltage of the resistor divider from the output node to the feedback pin.
LVEN2	7	Enabled (high level active) or Disabled (low level or suspended) of LVBUCK2.
VPLDO1	8	LDO1 Power Pin. Connect a 10uF bypass capacitor to GND to reduce input noise.
LDOOUT1	9	LDO1 Output Pin. Connect the 10uF bypass capacitor to GND.
FBLDO2	10	LDO2 Feedback Pin. Set the output voltage of the resistor divider from the output node to the feedback pin.
LDOOUT2	11	LDO2 Output Pin. Connect the 10uF bypass capacitor to GND.
VPLDO2	12	LDO2 Power Pin. Connect a 10uF bypass capacitor to GND to reduce input noise.
ENLDO1	13	Enable (high level active) or Disable (low level or floating) of LDO1.
ENLDO2	14	Enable (high level active) or Disable (low level or floating) of LDO2.
POR	15	Power On Reset.
LVEN1	16	Enable (high level active) or Disable (low level or floating) of LVBUCK1.
LVOUT1	17	LVBUCK1 Feedback Pin. Set the output voltage of the resistor divider from the output node to the feedback pin.
LVVP1	18	LVBUCK1 Power Pin. Connect a 10uF bypass capacitor to GND to reduce input noise.
LVSW1	19	LVBUCK1 Switch Pin. Connect this pin to an inductor to minimize the routing area and reduce EMI.
LVGP1	20	Ground.
HVOUT2	21	HVBUCK2 Feedback Pin. Set the output voltage of the resistor divider from the output node to the feedback pin.
HVBST2	22	Bootstrap pin. The positive power supply pole of the MOSFET driver transistor with internal floating high side drive. Connect a 22nF bypass capacitor between this pin and HVSW2.

Pin Function (Continue)

Pin No.	Pin Name	Pin Function
HVSW2	23	HVBUCK2 Switch Pin. Connect this pin to an inductor to minimize the routing area and reduce EMI.
HVVP2	24	HVBUCK2 Power Pin. Connect a 10uF bypass capacitor to GND to reduce input noise.
HVEN2	25	Enable (high level active) or Disable (low level or floating) of HVBUCK2.
HVEN1	26	Enable (high level active) or Disable (low level or floating) of HVBUCK1.
HVVP1	27	HVBUCK1 Power Pin. Connect a 10uF bypass capacitor to GND to reduce input noise.
HVSW1	28	HVBUCK1 Switch Pin. Connect this pin to an inductor to minimize the routing area and reduce EMI.
EP	29	Thermal Pad. Connected to GND。

Block Diagram

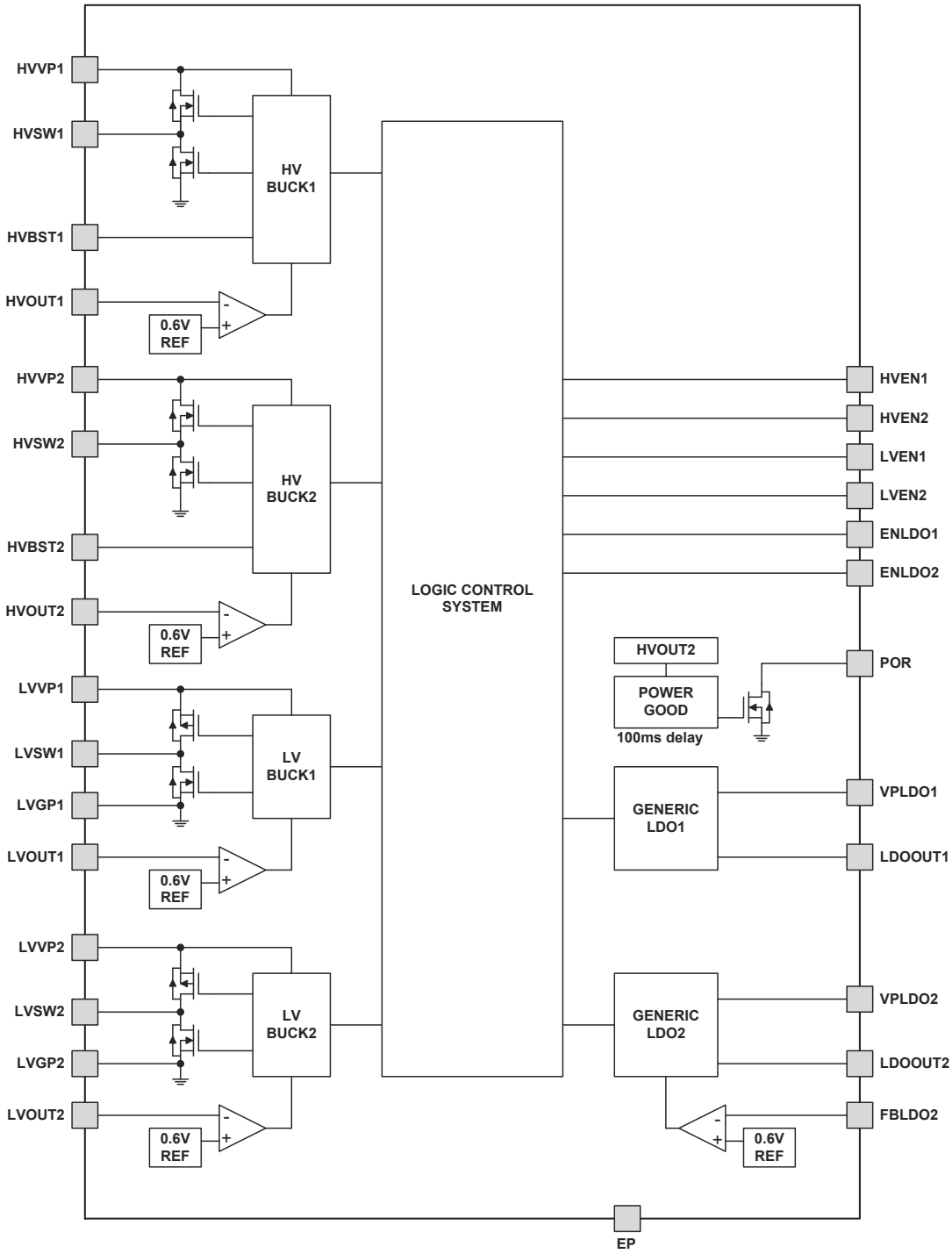


Figure 1. Internal functional block diagram

Functional Description

The ET598S6 is high efficient and highly integrated power management IC primarily designed for OTT and IPTV applications. It includes 4 high-efficiency synchronous buck regulators and 2 LDO, providing 6 output voltages. The device also includes a reset monitor that provides a reset output signal to the processor. Each voltage regulator is specifically designed for efficient operation across the entire load range. With a typical switching frequency of 1.2MHz, the external L-C filter can be very small and still provide very low output voltage ripple. Use recommended external inductors and capacitors for internal compensation to maintain stability. Synchronous rectification produces high-efficiency low voltage and high output current. Other functions include soft start, under-voltage protection, over-voltage protection, short current protection, over-current protection, and thermal overload protection. All Buck can operate in automatic mode (PWM/PFM). Under light load, Buck enters PFM mode and reduces the switching frequency and supply current to maintain high efficiency.

Soft Start

The ET598S6 has an internal soft start circuit that limits surge current during startup, allowing the converter to gradually reach a steady-state operating point when powered on, thereby reducing startup surge impact. During startup, the switch current limit gradually increases. The startup time depends on the capacitance value, load current, and output voltage.

Over Current Protection

The current limiting function can protect equipment and any external components under overload conditions. In PWM mode, current limiting is achieved by using an internal comparator, which trips at the current level based on its voltage reduction capability. If the output is short circuited to ground, the device enters a timed current limiting mode, in which the NFET conducts for a longer time until the inductor current drops below the low threshold, ensuring that the inductor current has more time to decay and prevent loss of control.

Start Timing

Once HVVP1/HVVP2/LVVP1/LVVP2/VPLD1/VPLDO2 reach the UVP threshold and the ENABLE pin is high, HVBUCKX/LVBUCKX/LDOX will start.

Reset Monitor

The POR pin of ET598S6 is an open drain output between the POR pin and the GND pin. Set the power on reset output to low level until the output voltage of HVOUT2 pin exceeds the set threshold (91%) and the descent timer (100ms) expires. In addition, as long as the HVEN2 pin is low or open, the POR will immediately set to low regardless of the output voltage. When POR is released (not set to low level), an external resistor connected to any external bias voltage will pull up the POR pin.

Under Voltage Protection

The voltage of HVVP1/HVVP2/LVVP1/LVVP2/VPLD1/VPLDO2 is monitored under power supply voltage conditions, and the operation of the device cannot be guaranteed. This component will be automatically disabled. To prevent unstable operation, UVP has a hysteresis window. Each under-voltage protection (UVP) will disable its output, and once the power supply voltage exceeds the UVP hysteresis, the device will initiate a power on sequence and then enter an active state.

Over Voltage Protection

The monitoring of HVVP1/HVVP2/LVVP1/LVVP2 voltage under over-voltage conditions of the power supply cannot guarantee the operation of the devices. The purpose of OVP is to protect the components connected to the PMIC output and all other components from any damage and malfunction. Once HVVP1/HVVP2 rises above 20V, HVBUCK1/HVBUCK2 will be automatically disabled. To prevent misoperation, OVP has a hysteresis window. Overvoltage protection (OVP) will force the device to enter a reset state. Once the power supply voltage falls below the OVP lower threshold, the device will initiate a power on sequence and then enter an active state.

HVBUCK1/HVBUCK2 operates at a maximum input voltage (with a guaranteed parameter of 20V). The absolute maximum value of the device is 30V.

Thermal Shutdown

The temperature of the chip is monitored under over temperature conditions, and if the temperature is too high, the component will be automatically disabled. Hot shutdown (OTP) will force the device to enter a reset state. When reset, all circuits are disabled. To prevent misoperation, the hysteresis window of OTP is approximately 20°C. Once the temperature drops below the OTP hysteresis, the device will initiate a power on sequence and then enter an active state. In the active state, the component will start as if it were the first time.

Absolute Maximum Ratings

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Symbol	Parameters	Min	Max	Unit
V_{IN}	HVVP1, HVSW1, HVEN1 Voltage Range	-0.3	30	V
	HVVP2, HVSW2, HVEN2 Voltage Range	-0.3	V_{IN}+0.3	V
	HVBST1, HVBST2 Voltage Range	-	HVSWX+6	V
	Other Pins Voltage Range	-0.3	10	V
V_{ESD}	Human Body Model (HBM)	-	2000	V
	Machine Model (MM)	-	200	V
T_J	Maximum Junction Temperature	-	+125	°C
T_A	Recommended Working Temperature Range	-40	+125	°C
T_{STG}	Storage Junction Temperature	-50	+150	°C
T_L	Reflow Soldering Temperature	-	300	°C
P_D	T_A=25°C,QFN28L 4X4	-	2.5	W

Electrical Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
HVBUCK1 & HVBUCK2 Characteristics (V_{IN} = 12V, T_A = 25°C, Unless Otherwise Noted)						
HVVP1/2	Operating Input Voltage Range		3.1		20	V
V_{UVLO}	Input UVLO Threshold	Input Voltage Falling			3	V
V_{OVP}	Input OVLO Threshold	Input Voltage Rising		20		V
I_Q	Quiescent Current	I_{OUT}=0, HVOUTX=103%		400	600	uA
I_{SHDN}	Shutdown Current	HVENX = 0V HVVPX = 12V		3		uA
V_{HVENX_R}	HVENX Rising Threshold	HVENX Rising		1.4		V
V_{HVENX_F}	HVENX Falling Threshold	HVENX Falling		0.6		V
V_{HVOUTX}	FB Reference Threshold		0.588	0.6	0.612	V
Line-Reg	Output Voltage Line Regulation			0.04	0.4	%/V
Load-Reg	Output Voltage Load Regulation			0.5		%
I_{LIM}	Current Limit	Duty = 30%		3.5		A
F_{SW}	Switching Frequency			1.2		MHz
R_{ON}	NMOS On-Resistance	I_{SW}=100mA		0.07		Ω
LVBUCK1 & LVBUCK2 Characteristics (V_{IN} = 3.6V, T_A = 25°C, Unless Otherwise Noted)						
LVVP1/2	Operating Input Voltage Range		2.5		6	V
V_{UVLO}	Input UVLO Threshold	Input Voltage Falling		2.2		V
V_{OVP}	Input OVLO Threshold	Input Voltage Rising		6.5		V
I_Q	Operating Current	I_{OUT}=0, LVOUTX=60%		150	200	uA
	Quiescent Current	I_{OUT}=0, LVOUTX=103%		40	80	uA
I_{SHDN}	Shutdown Current	LVENX = 0V LVVPX = 4.2V		0.1	1	uA
V_{LVENX_R}	LVENX Rising Threshold	LVENX Rising		1.4		V
V_{LVENX_F}	LVENX Falling Threshold	LVENX Falling		0.6		V
V_{OUT_ACC}	V_{OUT} Voltage Accuracy		-1.5	1	1.5	%

Electrical Characteristics (Continue)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
LVBUCK1 & LVBUCK2 Characteristics (V_{IN} = 3.6V, T_A = 25°C, Unless Otherwise Noted)						
V_{LVOUTX}	FB Reference Threshold		0.588	0.6	0.612	V
Line-Reg	Output Voltage Line Regulation			0.04	0.4	%/V
Load-Reg	Output Voltage Load Regulation			0.5		%
I_{LIM}	Current Limit	Duty = 30%		3.5		A
F_{SW}	Switching Frequency			1.2		MHz
R_{ON_P}	PMOS On-Resistance	I_{SW}=100mA		0.1		Ω
R_{ON_N}	NMOS On-Resistance	I_{SW}=100mA		0.07		Ω
LDO1 & LDO2 Characteristics (V_{IN} = 3.6V, T_A = 25°C, Unless Otherwise Noted)						
VPLDOX	Operating Input Voltage Range		2.5		6	V
V_{UVLO}	Input UVLO Threshold	Input Voltage Falling		2.2		V
V_{ENLDOX_R}	ENLDOX Rising Threshold	ENLDOX Rising		1.4		V
V_{ENLDOX_F}	ENLDOX Falling Threshold	ENLDOX Falling		0.6		V
V_{OUT_ACC}	V_{OUT} Voltage Accuracy		-3	1.5	3	%
V_{FBLDO2}	LDO2 FB Reference Threshold		0.588	0.6	0.612	V
Reset Monitor Characteristics (V_{PULLUP} = 3.3V, TA = 25°C, Unless Otherwise Noted)						
V_{HVOUT2}	POR Threshold	V_{HVOUT2} Rising	85	90	95	%
T_{delay}	Delay Time	POR Delay before release		100		ms

Application Circuits

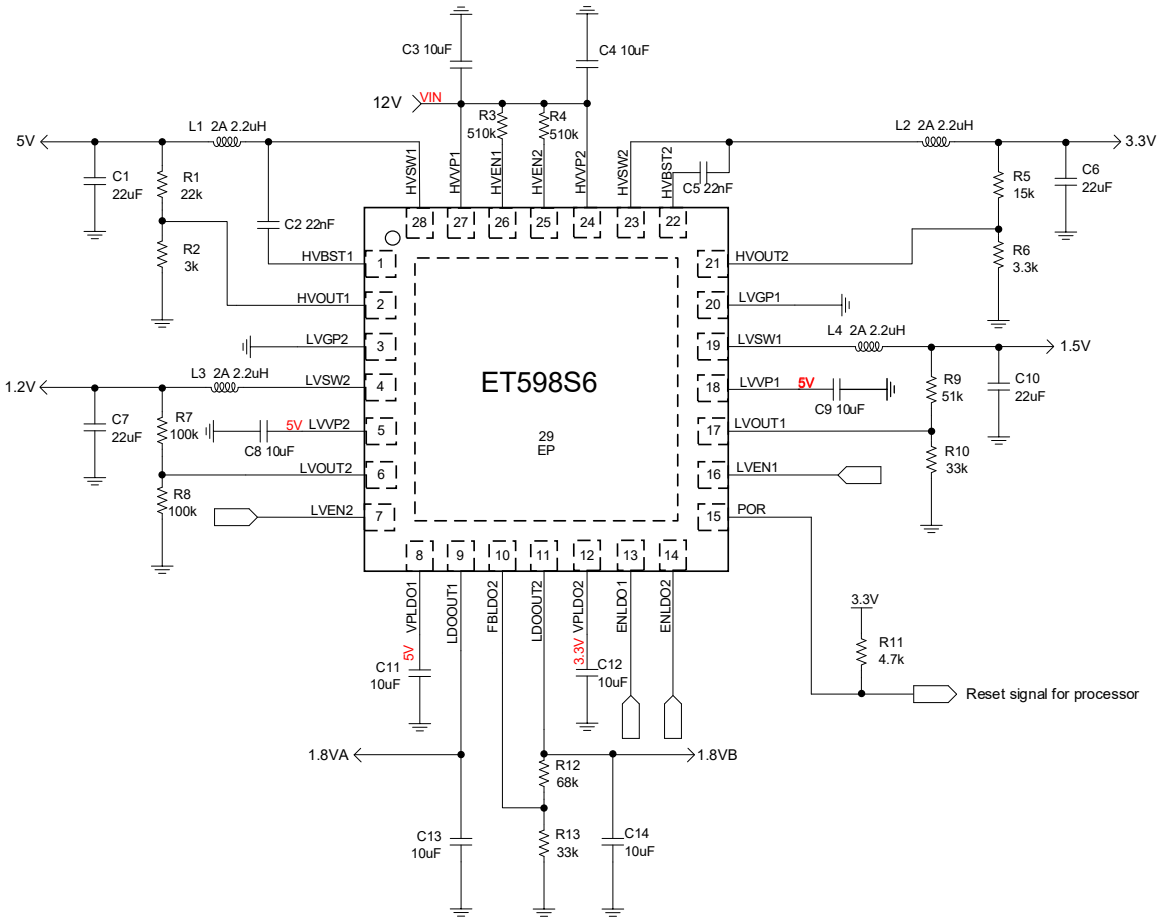


Figure 2. Typical application circuit diagram

*：The circuit is for reference only.

Applications Information

Output Voltage

ET598S6 uses a resistive voltage divider from the output node to the feedback pin to set the output voltage. It is recommended to use 1% or better accuracy for the voltage divider resistor. The calculation of the output voltage is shown in Equation 1:

$$V_{OUT} = \frac{V_{Feedback} \times (R1 + R2)}{R2} \quad (1)$$

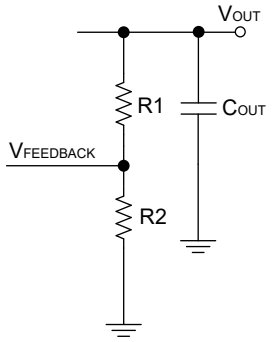


Figure 3. Application of output voltage regulation

To improve efficiency under light loads, high-value resistors can be considered, but excessively high values can increase system noise.

BUCK Power Supply Selection

The input voltage power supply range of HVBUCK1/HVBUCK2 is between 3.1V and 20V. The input voltage power supply range of LVBUCK1/LVBUCK2/LDO1/LDO2 is between 2.5V and 6V. The input power supply must be well regulated, and HVVP1/HVVP2/LVVP1/LVVP2 must be as close as possible to the input capacitor.

BUCK Inductors Selection

In applications, it is recommended to use inductors with a DC rated current at least 25% higher than the maximum load current. To achieve the highest efficiency, please choose inductors with a DC resistance less than 15mΩ. For most designs, derive the inductance value from the following Equation 2:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{(V_{IN} \times \Delta I_L \times F_S)} \quad (2)$$

In Equation 2, ΔI_L is the ripple current flowing through the inductor, and the selected inductor has a rated current close to 30% of the maximum load current. The calculation method for the peak current in the inductor is shown in Equation 3:

$$I_{L(MAX)} = I_{Load} + \frac{\Delta I_L}{2} \quad (3)$$

In light load mode (less than 100mA), using a larger inductance can improve device efficiency.

BUCK Input Capacitor Selection

The input current of a buck converter is discontinuous, therefore a capacitor is required to provide AC current to the buck converter and maintain DC input voltage. For optimal performance, please use low ESR capacitors, such as ceramic capacitors with X5R or X7R dielectric and low temperature coefficient. For most applications, a 10uF capacitor is sufficient. The input capacitor requires sufficient ripple current rating as it absorbs input switch noise. Equation 4 estimates the RMS current in the input capacitor:

$$I_{CIN} = I_{Load} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad (4)$$

The worst-case scenario occurs when $V_{IN}=2V_{OUT}$, at which point:

$$I_{CIN} = \frac{I_{Load}}{2} \quad (5)$$

For simplicity, please choose an input capacitor with a rated current greater than half of the maximum load current. The input capacitor can be an electrolytic capacitor, tantalum capacitor, or ceramic capacitor. When using electrolytic capacitors or tantalum capacitors, a small, high-quality ceramic capacitor (0.1uF) should be placed as close to the IC as possible. When using ceramic capacitors, please ensure that they have sufficient capacitance to provide sufficient charge to prevent excessive input voltage ripple. Estimate the input voltage ripple caused by capacitance using Equation 6:

$$\Delta V_{IN} = \frac{I_{Load}}{F_S \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

BUCK Output Capacitor Selection

The output capacitor stabilizes the DC output voltage and can use ceramic, tantalum, or low ESR electrolytic capacitors. If a low ESR electrolytic capacitor is used, Equation 7 estimates the output voltage ripple:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_S \times C_{OUT}}\right) \quad (7)$$

In Equation 7, L is the value of inductance, and RESR is the equivalent series resistance of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplicity, estimate the output voltage ripple using Equation 8:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F^2_S \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

For tantalum capacitors or electrolytic capacitors, ESR is dominant at the switching frequency, and the approximate estimation method for their output ripple is shown in Equation 9:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor will affect the stability of the regulator system. ET598S6 can be optimized for a wide range of capacitance and ESR values.

BUCK Bootstrap Capacitor Selection

A 0.1F ceramic capacitor must be connected between HVBST1 or HVBST2 pins and HVSW1 or HVSW2 pins for proper operation. Capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 6.3V or higher voltage rating.

LDO Output Capacitor Selection

To ensure the stability of the LDO design, there should be at least one 4.7uF output capacitor. When using low ESR capacitors, there is no need for series resistors. For most applications, it is recommended to use 10uF ceramic capacitors. The larger the value, the better the transient response and the higher the power supply rejection ratio (PSRR) of LDO. Please refer to typical performance characteristics for the allowable range of output capacitance to ensure the stability of the circuit.

PCB Layout

PCB layout is an important component of DC-DC converter design. Poor circuit board layout can damage the performance of DC-DC converters and surrounding circuits, leading to electromagnetic interference, ground bounce, and loss of voltage accuracy. These will provide feedback error signals to the DC-DC converter, leading to poor or unstable regulation. A good layout can be achieved by following some simple design rules.

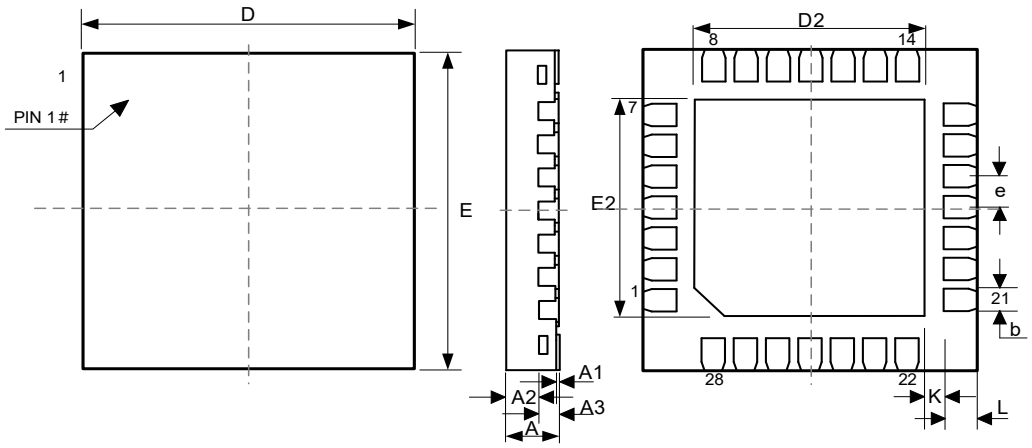
Minimize the area of the switch current circuit as much as possible. In a voltage regulator, there are two circuits for fast switching of current. The first circuit starts from the CIN input capacitor, to the VIN terminal of the regulator, to the SW terminal of the regulator, to the inductor, and then to the output capacitor COUP and load. The second circuit starts from the output capacitor ground, goes to the regulator GND terminal, goes to the inductor, and then goes to the COUP and load. In order to minimize the two circuit areas, the input capacitor should be placed as close as possible to the VIN terminal. The grounding of both input and output capacitors should be connected to GND through a small localized plane. Inductors should be placed as close as possible to the SW pin and output capacitor.

Line width principle:

1. The line width is determined by the magnitude of the current flowing through it. For high current wiring, sufficient line width should be provided to optimize efficiency and reduce heat generation; Especially for SW nodes, copper plating can be used if conditions permit. The line width of the control circuit should be at least 20mil, such as V_{CC}, GND (SGND);
2. Make the input and output bus connections as wide as possible. To reduce any voltage drop on the input or output of the converter and improve efficiency. If the voltage accuracy at the load is important, please ensure that the feedback point is as close to the load as possible, so as to avoid the impact of voltage drop on the feedback acquisition accuracy on the line.
3. Bypass/decoupling capacitor: The capacitor is arranged near the IC power pin. When there are multiple capacitors, the small capacitance value is close to the IC;
4. Minimize the trace length to the FB terminal. The feedback trace should be wired from the SW pin and inductor to avoid switch noise interference on the feedback signal.

Package Dimension

QFN28L



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
	--	0.55	--
A2		0.203 REF	
b	0.15	0.20	0.25
D		4.00 BSC	
D2	2.70	2.80	2.90
E		4.00 BSC	
E2	2.70	2.80	2.90
e		0.40 BSC	
L	0.30	0.40	0.50
K		0.25 REF	

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-01-29	Initial version	Caojc	Wuhs	Liujy