ET75116 - Laser Driver for ToF

General Description

ET75116 is a laser diode driver IC for ToF (Time of Flight), offered in small WLCSP25 package.

Features

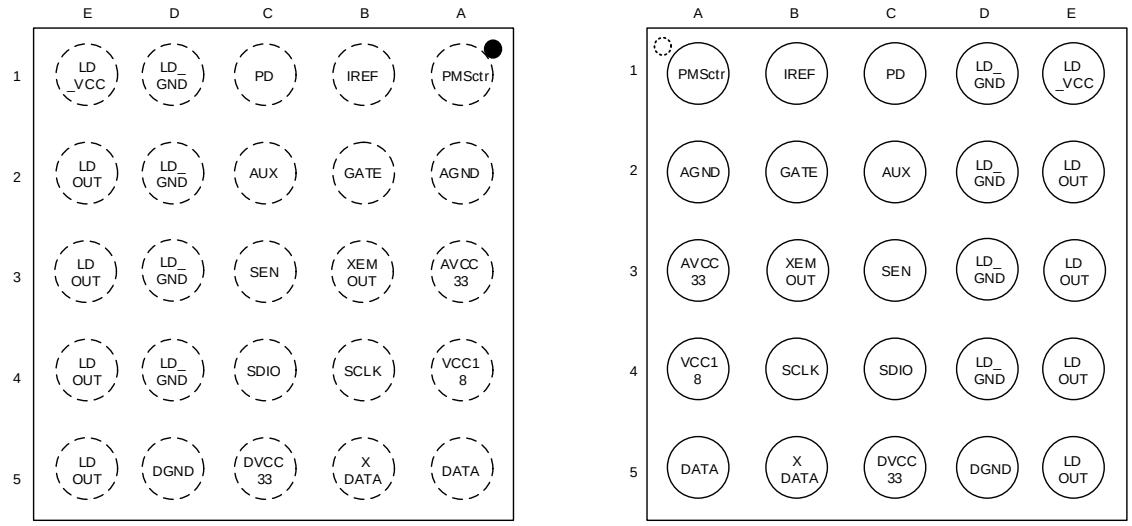
- Supply Voltage AV_{CC33} = DV_{CC33} = 3.0V~3.6V, LDV_{CC} = 3.0V~5.5V, V_{CC18} = 1.2V/1.8V
- Driver for Anode Common and Floating Laser
- Maximum Drive Current 3.0A
- Built-in Fail Safe Function of LVDS Input.
- APC (Auto Power Control), ACC (Auto Current Control) are Available
- Auto Bias APC, Fixed Bias APC are Available
- PMS Mode
- Over Current Detection, APC Error Detection
- Diffuser Removal Detection
- Temperature Monitor: 10bit ADC
- SPI Interface(1.2V/1.8V compatible)
- Package Information:

Part No.	Package	Packing	MSL
ET75116	WLCSP25 (2.30mm×2.13mm)	Tape and Reel,3.0K/Reel	1

Applications

- TOF Laser

Pin Configuration



Top View Bottom View

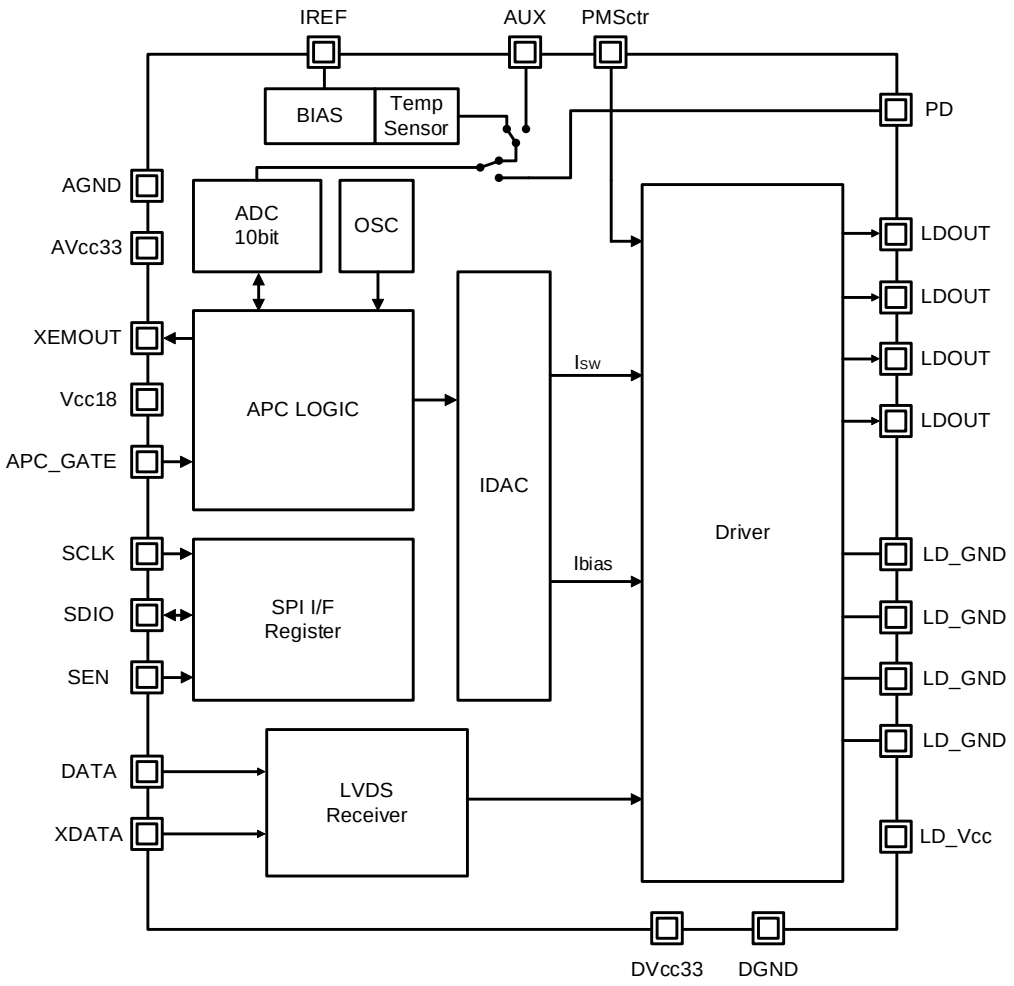
Pin Function

Pin No.	Symbol	I/O	Pin type	Description
A3	AV_{CC33}		Power	Analog power supply 3.3 V
C5	DV_{CC33}		Power	Digital power supply 3.3 V
E1	LDV_{CC}		Power	Power supply for Laser diode 3.3V
A4	V_{CC18}		Power	Logic power supply 1.2V/1.8V
A2	AGND		Ground	Analog power GND
D5	DGND		Ground	Digital power GND
D1～D4	LD_GND		Ground	Power GND for Laser diode
E2～E5	LDOUT	O	Analog Output	Current output for Laser diode
A5	DATA	I	Digital Input	Timing Pulse input for Laser diode drive
B5	XDATA			
B2	GATE (APC_GATE)	I	Digital Input	Laser emission area enable signal input L: Disable H: Enable
B4	SCLK			Serial clock line for SPI
C3	SEN			Serial Enable L: Serial Disable H: Serial Enable

Pin Function (Continued)

Pin No.	Symbol	I/O	Pin type	Description
C4	SDIO	I/O	Digital Input Output	Serial Data line for SPI
B3	XEMOUT	O	Digital Output	Emergency detection result L: Emergency error H: normal
C1	PD	I	Analog Input	Input of PD Connection of PD Anode
C2	AUX	I	Analog Input	External thermistor connection to internal ADC. ADC input Range 0V~2.5V
A1	PMSctr	I	Digital Input	PMS MODE control pin L: Disable H: Enable
B1	IREF	O	Analog Output	Pin for reference current setting. (connect to GND through 22KΩ)

Block Diagram



Functional Description

Serial I/F

Serial address bit definition

Bit	Bit definition
A7	Read/Write select bit 0: Serial interface write mode 1: Serial interface Read mode
A6～A0	Register address select bit

- Transmission and reception are performed in 16-bit units consisting of 8 address bits and 8 data bits.
- Both address and data are MSB first.
- The address switches to read or write mode by A [7].
- Read/Write supports continuous Read, continuous Write together.

Normal write

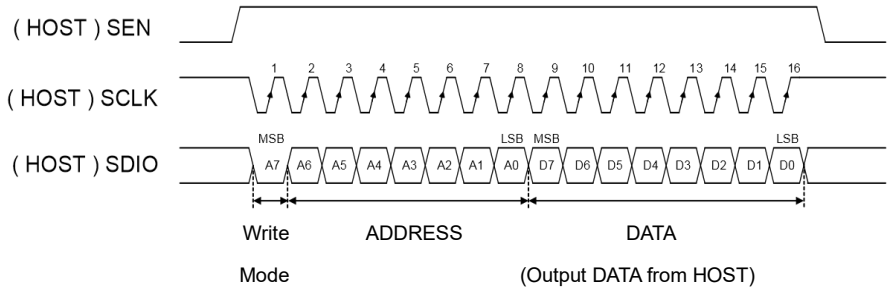


Figure 1

Continuous write

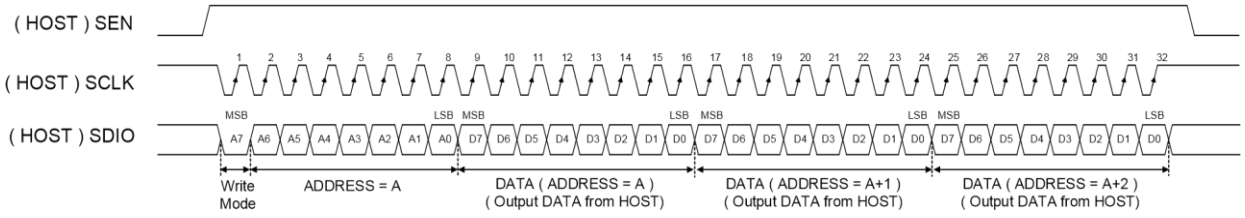


Figure 2

The data written in the register is effective at the rising edge of the 16th (last) SCLK signal.

Normal read

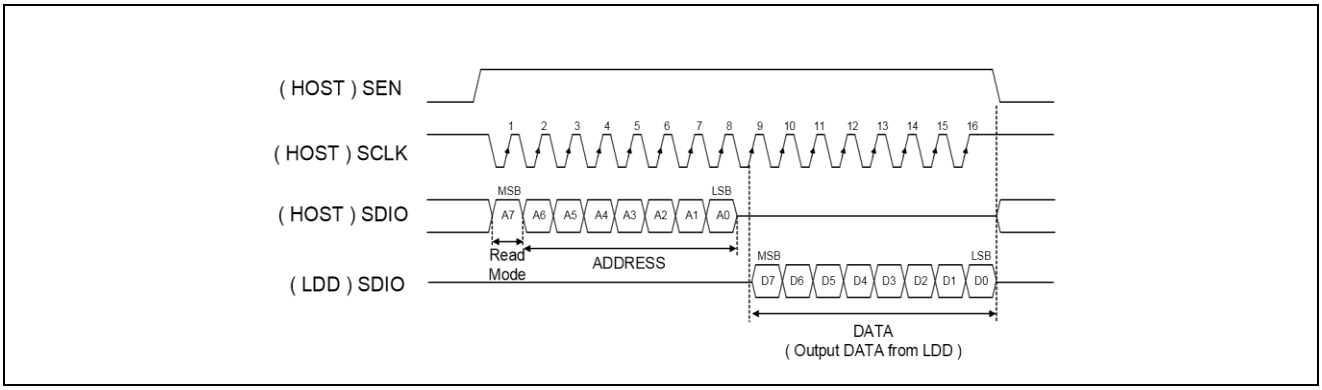


Figure 3

Continuous read

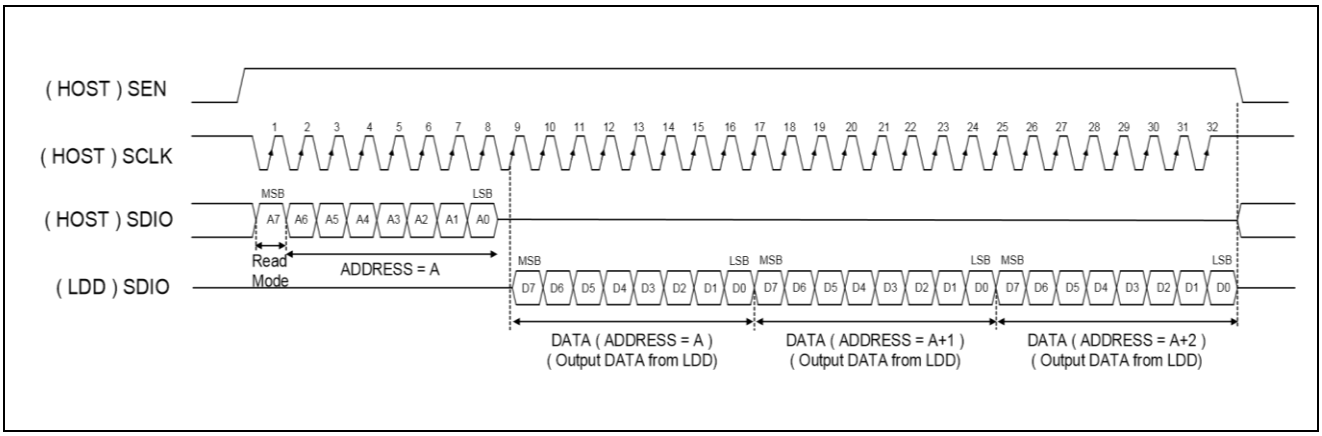


Figure 4

Address Map

In Address Map, even blank fields "-" have physical register. Please keep them as default value.

In undefined addresses, there are no physical registers.

In register continuous write, the reset of the abnormal detection error of Address 0x23h and the global reset of 0x25h are not performed.

Address	Data								Read/ Write
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
0x00	RST_DIS	VBGADJ [1:0]		ACC_MODE	APC_MODE [1:0]		PS_MODE	DEEP SLEEP	R/W
0x01	I_{BIAS}_APCL1 [7:0]								R/W
0x02	I_{BIAS}_APCH1 [7:0]								R/W
0x03	ISW_APCL1 [7:0]								R/W
0x04	ISW_APCH1 [7:0]								R/W
0x05	ISW_APCL2 [7:0]								R/W
0x06	ISW_APCH2 [7:0]								R/W
0x07	I_{BIAS}_FIX [7:0]								R/W

Address Map (Continued)

Address	Data								Read/ Write
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
0x08	ISW_FIX [7:0]								R/W
0x09	—	I_{BIAS}_BACK [6:0]							R/W
0x0A	—	—	—	—	TEMP INITAL_IN [9:8]		PD_TARGET_IN [9:8]		R/W
0x0B	PD_TARGET IN [7:0]								R/W
0x0C	TEMP_INITIAL_IN [7:0]								R/W
0x0D	DIF_ERR_SEL[1:0]		IAUX_OFFSET [2:0]			IPD_OFFSET [2:0]			R/W
0x0E	OC_CLAMP	APC2_ERR_SEL [1:0]		APC1_ERR_SEL	APC_ERR_MODE	OC_SEL [2:0]			R/W
0x0F	AS_I [3:0]				AS_W [3:0]				R/W
0x10	TEST_FSOFF	—	—	—	TrAS [3:0]				R/W
0x11	Reversed								R/W
0x12	Reversed						PMS_EM	PMS_EN	R/W
0x13	AD_GAIN [1:0]		ADC_START [1:0]		APC_CAL	ADSEL	ADEN [1:0]		R/W
0x14	AD_ALARM	APC_ALARM	—	—	—	—	TEMP_AD_DATA [9:8]		R
0x15	TEMP_AD_DATA [7:0]								R
0x16	AD_ALARM	—	—	—	—	—	PD_TARGET_DATA [9:8]		R
0x17	PD_TARGET_DATA [7:0]								R
0x18	I_{BIAS}_CALC [7:0]								R
0x19	ISW_CALC [7:0]								R
0x1A	PD_L2 [9:8]		PD_H1 [9:8]		PD_L1 [9:8] / CAL_Power [9:8]		PD_BG [9:8] /CAL_BG [7:0]		R
0x1B	—	—	APC2_CHECK_DATA [9:8]		APC1_CHECK_DATA [9:8]		PD_H2 [9:8]		R
0x1C	PD_BG [7:0] / CAL_BG [7:0]								R
0x1D	PD_L1 [7:0] / CAL_POWER [7:0]								R
0x1E	PD_H1 [7:0]								R
0x1F	PD_L2 [7:0]								R
0x20	PD_H2 [7:0]								R
0x21	APC1_CHECK_DATA [7:0]								R
0x22	APC2_CHECK_DATA [7:0]								R
0x23	APC2_EM	APC1_EM	VCC_EM	DIF_EM	OC_EM	VER_REG			R
0x24	Reversed								R/W
0x25	GL_RST								R/W

Description of Register

Address 0x00

Bit	Name	Bit definition	Initial
7	RST_DIS	Global reset (GL_RST) control selection by serial interface. 0: Enable 1: Disable	0
6-5	VBGADJ [1:0]	Temperature properties adjustment of the internal bandgap voltage 00: Standard condition 01: Temperature coefficient +0.5% 10: Temperature coefficient +1.0% 11: Temperature coefficient +1.5%	00
4	ACC_MODE	Selection of ACC (Auto Current Control) MODE 0: APC MODE 1: ACC MODE $I_{BIAS:}$ always on with current programmed by I_{BIAS_FIX} [7:0] $I_{SW:}$ controlled by DATA/XDATA with current programmed by $I_{SW\ FIX}$[7:0] No diffuser error detection and over current error detection at this mode.	0
3-2	APC_MODE[1:0]	Selection of APC (Auto Power Control) MODE Please set ACC_MODE =0 00: APC1(I_{BIAS} calculation) =ON. APC2(ISW calculation) =ON Both I_{BIAS} and I_{SW} drives laser by current operated in APC 01: APC1(I_{BIAS} calculation) =ON, APC2(ISW calculation) =OFF I_{SW} drives laser by fixed current programmed by $I_{SW\ FIX}$[7:0] 10: AAPC1(I_{BIAS} calculation) =OFF. APC2(ISW calculation) =ON I_{BIAS} drives laser by fixed current programmed by I_{BIAS_FIX} [7:0] 11: APC1(I_{BIAS} calculation) =OFF, APC2(ISW calculation) =OFF Both I_{BIAS} and I_{SW} drives laser by fixed current programmed by I_{BIAS_FIX} [7:0] and $I_{SW\ FIX}$[7:0 separately the diffuser error detecting, the Over Current error detecting are effective for all setting	00
1	PS_MODE	Interlocking control with APC_GATE of Power Save of the Driver. IDAC, LVDS circuit 0: Interlocking control with APC_GATE APC_GATE= Low: Driver. IDAC.LVDS Power Save APC_GATE= High: Active 1: No Interlocking control with APC_GATE Power Save controlled by DEEP_SLEEP only	0
0	DEEP SLEEP	Power Save control 0: Active 1: Deep Sleep Power Save	0

Address 0x01

Bit	Name	Bit definition	Initial
7-0	I_{BIAS}_APCL1[7:0]	Bias current setting of APCL1 00000000: 0 A ~ 11111111: 0.92A(3.59mA/step)	0000 0000

Address 0x02

Bit	Name	Bit definition	Initial
7-0	I_{BIAS}_APCH1 [7:0]	Bias current setting of APCH1 00000000: 0 A ~ 11111111: 0.92 A(3.59mA/step)	0000 0000

Address 0x03

Bit	Name	Bit definition	Initial
7-0	ISW_ APCL1 [7:0]	I_{SW} current setting of APCL1 00000000: 0 A ~ 11111111: 3.18 A(12.4mA/step)	0000 0000

Address 0x04

Bit	Name	Bit definition	Initial
7-0	ISW_ APCH1 [7:0]	I_{SW} current setting of APCH1 00000000:0 A ~ 11111111:3.18 A(12.4mA/step)	0000 0000

Address 0x05

Bit	Name	Bit definition	Initial
7-0	ISW_APCL2[7:0]	I_{SW} current setting of APCL2 00000000:0 A ~ 11111111:3.18 A(12.4mA/step)	0000 0000

Address 0x06

Bit	Name	Bit definition	Initial
7-0	ISW_APCH2 [7:0]	I_{SW} current setting of APCH2 00000000:0 A ~ 11111111:3.18 A(12.4mA/step)	0000 0000

Address 0x07

Bit	Name	Bit definition	Initial
7-0	I_{BIAS}_FIX [7:0]	Used as ①I_{BIAS} current setting in initial power adjustment ②I_{BIAS} current setting that is fixed with an APC mode selected in APC_MODE [1:0] ③In APC_ERR_MODE=0, set fixed I_{BIAS} current after APC error 0000 0000: 0 A ~ 1111 1111: 0.92 A (3.59mA/step)	0000 0000

Address 0x08

Bit	Name	Bit definition	Initial
7-0	ISW_FIX [7:0]	Used as ①I_{SW} current setting in initial power adjustment ②I_{SW} current setting that is fixed with an APC mode selected in APC_MODE [0:1] ③In APC_ERR_MODE=0, set fixed I_{SW} current after APC error 0000 0000: 0 A ~ 1111 1111: 3.18 A (12.4mA/step)	0000 0000

Address 0x09

Bit	Name	Bit definition	Initial
7	—	Not used. Please keep this bit "0".	0
6-0	I_{BIAS}_BACK [6:0]	Offset current setting from Bias calculation result 000 0000: 0 ~ 111 1111: 0.46A (3.59mA/step)	000 0000

Address 0x0A

Bit	Name	Bit definition	Initial
7-4	-	Not used. Please keep this bit "0".	0000
3-2	TEMP_INITIAL_IN [9:8]	AD level input of unrevised 25 °C temperature sensor. Higher 2Bit (input from external controller)	00
1-0	PD_TARGET_IN [9:8]	AD level input of the PD target. Higher 2Bit (input from external controller)	00

Address 0x0B

Bit	Name	Bit definition	Initial
7-0	PD_TARGET_IN [7:0]	AD level input of the PD target. Lower 8Bit (input from external controller)	0000 0000

Address 0x0C

Bit	Name	Bit definition	Initial
7-0	TEMP_INITIAL_IN [7:0]	AD level input of unrevised 25 °C temperature sensor. Lower 8Bit (input from external controller)	0000 0000

Address 0x0D

Bit	Name	Bit definition	Initial
7-6	DIF_ERR_SEL [1:0]	detect Diffuser issue compare PD_BG [9:0] with the PD ADC result that let you emit light in $I_{BIAS}+I_{SW}$ which you decided in APC1,2 00: Error in less than PB_BG [9:0] + 128dec 01: Error in less than PB_BG [9:0] + 64dec 10: Error in less than PB_BG [9:0] + 32dec 11: Error detection function OFF	00
5-3	IAUX_OFFSET [2:0]	Offset current setting to AUX_ADC terminal Enable when "APC_GATE = Low" only 000: OFF 001: 20uA 010: 40uA 011: 78uA 100: 152uA 101: 300uA 110: 592uA 111: 1172uA	000
2-0	IPD_OFFSET [2:0]	Offset current setting to PD terminal Enable when "APC_GATE = High" only 000: OFF 001: 20uA 010: 40uA 011: 78uA 100: 152uA 101: 300uA 110: 592uA 111: 1172uA	000

Address 0x0E

Bit	Name	Bit definition	Initial
7	OC_CLAMP	LDOUT, XEMOUT output control at the time of the Over Current detection. 0: Over Current detection, LDOFF and send error signal to XEMOUT and register OC_EM. 1: Over Current detection, send error signal to register OC_EM only. Clamp output current by Over Current threshold current.	0
6-5	APC2_ERR_SEL [1:0]	Selection of the APC2 error threshold compare PD_TARGET_IN [9:0] with the ADC result of the PD voltage that drive laser by I_{BAIS} + I_{SW} decided in APC1,2 and send error signal when error happened. 00: Error with errors more than ± 64dec（6.25% of PD AD full scales) 01: Error with errors more than ± 128dec (12.5% of PD AD full scales) 10: Error with errors more than ± 256dec (25% of PD AD full scales) 11: Error detection function OFF.	00
4	APC1_ERR_SEL	Judge error of I_{BIAS} calculated in APC1. 0: Calculated I_{TH} is smaller than 0; or When PD ADC results at the time of the laser drive are more than PD_B [9:0] + 64dec in I_{BIAS}, send error signal 1: Error detection function OFF (If Calculated I_{TH} is smaller than 0, I_{BIAS} will be zero).	0
3	APC_ERR_MODE	Processing method selection at the time of the APC1, APC2 error. 0: Make LDOFF and XEMOUT terminal will be low 1: Drive laser by fixed current programmed by I_{BIAS_FIX} [7:0], no error signal at XEMOUT The error flag of the register will be set for both case.	0
2-0	OC_SEL [1:0]	Selection of the Over Current threshold 000: 3.0A 001: 2.6A 010: 2.2A 011: 1.8A 100: 1.4A 101: 1.0A 110: 0.7A 111: Error detection function OFF	000

Address 0x0F

Bit	Name	Bit definition	Initial
7-4	AS_I	Division ratio setting of the wave assist current 0000: assist current weak ~ 1111: assist current strong	0100
3-0	AS_W	Revision width setting of the wave assist current 0000: 0.36 ns ~ 1111: 2.16 ns (0.12ns step)	0111

Address 0x10

Bit	Name	Bit definition	Initial
7	TEST_FSOFF	LVDS Fail Safe function control 0: Fail Safe function existence effect （LVDS input is forced LDOFF at the time of opening) 1: Fail Safe function is invalid	0
6-4	—	Not used. Please keep this bit "0".	000
3-0	TrAS [3:0]	Revised the quantity of Tr wave assist 0000: assist weak ~ 1111: assist strong	1100

Address 0x12

Bit	Name	Bit definition	Initial
7-2	—	Reversed	000000
1	PMS_EM	PMS error monitor 0:normal 1:PMS error detection (clean error flag by writing 0 to this address)	0
0	PMS_EN	PMS Enable，1.2V/1.8V compatible 1:enable 0:disable (when PMS_EN=1，APC starts，0x12 can be written in the last step)	0

Address 0x13

Bit	Name	Bit definition	Initial
7-6	AD_GAIN [1:0]	Gain setting of the ADC of the internal temperature sensor 00: 8 times 0.186 °C/dec 01: 4times 0.371 °C/dec 10: 2 times 0.742 °C/dec 11: 1 time 1.480 °C/dec	00

5-4	ADC_START [1:0]	Control of the ADC start signal 00: ADC start in High of the APC_GATE signal for APC 01: PD ADC start for initial Power adjustment (Condition of APC_CAL=1) *Automatically goes back up to 00 after ADC 10: ADC start for internal temperature sensor or AUX_ADC (invalid during movement of the PD ADC) *Automatically goes back up to 00 after ADC 11: ADC start in High of the APC_GATE signal for APC	00
3	APC_CAL	Initial power adjustment mode control 0: Normal operation mode 1: Initial power adjustment mode *After ADC completion by the initial power adjustment, automatically return to 0	0
2	ADSEL	Input selection to internal ADC 0: internal temperature sensor 1: AUX ADC terminal signal voltage (For external thermal resistor)	0
1-0	ADEN [1:0]	OSC circuit control for AD CLK (Internal OSC Control) 00: All time Disable (OSC OFF) 01: AOSC Enable only at the time of APC_GATE=H 10: Same as 01 11: All time Enable	01

Address 0x14

Bit	Name	Bit definition	Initial
7	TEMP_AD_ALARM	Alarm signal indicating the AD conversion average of TEMP 0: AD conversion completion 1: During AD conversion, and DATA is uncertain	0
6	APC_AD_ALARM	Alarm signal indicating the AD conversion average of APC 0: AD conversion completion 1: During AD conversion AD for temperature monitor and initial Power adjustment do not work at the time of 1	0
5-2	—	Not used. Please keep this bit "0".	0000
1-0	TEMP_AD_DATA [9:8]	AD DATA for temperature monitors Higher 2bit	00

Address 0x15

Bit	Name	Bit definition	Initial
7	TEMP_AD_DATA [7:0]	AD DATA for temperature monitors Lower 8bit	0000 0000

Address 0x16

Bit	Name	Bit definition	Initial
7	PD_AD_ALARM	Alarm signal indicating the AD conversion average of PD 0: AD conversion completion 1: During AD conversion, and DATA is uncertain	0
6-2	—	Not used. Please keep this bit "0".	00000
1-0	PD_TARGET_DATA [9:8]	PD AD DATA after the initial power adjustment Higher 2bit （stored to external memory）	00

Address 0x17

Bit	Name	Bit definition	Initial
7-0	PD_TARGET_DATA [7:0]	PD AD DATA after the initial power adjustment Lower 8bit （stored to external memory）	0000 0000

Address 0x18

Bit	Name	Bit definition	Initial
7-0	I_{BIAS}_CALC [7:0]	I_{BIAS}_DAC set point which was calculated in APC1	0000 0000

Address 0x19

Bit	Name	Bit definition	Initial
7-0	ISW_CALC [7:0]	I_{SW}_DAC set point which was calculated in APC2	0000 0000

Address 0x1A

Bit	Name	Bit definition	Initial
7-6	PD_L2 [9:8]	PD ADC result in APC_L2 Higher 2bit	00
5-4	PD_H1 [9:8]	PD ADC result in APC_H1 Higher 2bit	00
3-2	PD_L1[9:8] / CAL_POWER [9:8]	PD ADC result in APC_L1 Higher 2bit PD ADC result at the time of the initial Power adjustment Higher 2bit	00
1-0	PD_BG [9:8] / CAL_BG [9:8]	PD ADC result in the APC BG section (lights out section) Higher 2bit BG_ADC result at the time of the initial Power adjustment Higher 2bit	00

Address 0x1B

Bit	Name	Bit definition	Initial
7-6	—	Not used. Please keep this bit "0".	00
5-4	APC2_CHECK_DATA [9:8]	PD_ADC result at the time of the APC2 error check Higher 2bit	00

3-2	APC1_CHECK_DATA [9:8]	PD_ADC result at the time of the APC1 error check Higher 2bit	00
1-0	PD_H2 [9:8]	PD_ADC result in APC_H2 Higher 2bit	00

Address 0x1C

Bit	Name	Bit definition	Initial
7-0	PD_BG [7:0] / CAL_BG [7:0]	PD_ADC result in the APC BG section (lights out section) Lower 8bit BG_ADC result at the time of the initial Power adjustment Lower 8bit	0000 0000

Address 0x1D

Bit	Name	Bit definition	Initial
7-0	PD_L1[7:0]/ CAL_POWER [7:0]	PD_ADC result in APC_L1 Lower 8bit PD_ADC result at the time of the initial Power adjustment Lower 8bit	0000 0000

Address 0x1F

Bit	Name	Bit definition	Initial
7-0	PDL2 [7:0]	PD_ADC result in APCL2 Lower 8bit	0000 0000

Address 0x20

Bit	Name	Bit definition	Initial
7-0	PDH2 [7:0]	PD_ADC result in APCH2 Lower 8bit	0000 0000

Address 0x21

Bit	Name	Bit definition	Initial
7-0	APC1 CHECK DATA [7:0]	PD_ADC result at the time of the APC1 error check Lower 8bit	0000 0000

Address 0x22

Bit	Name	Bit definition	Initial
7-0	APC2 CHECK DATA [7:0]	PD_ADC result at the time of the APC1 error check Lower 8bit	0000 0000

Address 0x23

Bit	Name	Bit definition	Initial
7	APC2_EM	APC2 error monitor 0: Normal 1: APC2 error detection (cleared error result by Dummy Write to this Address)	0
6	APC1_EM	APC1 error monitor 0: Normal 1: APC1 error detection	0

		(cleared error result by Dummy Write to this Address)	
5	VCC_EM	Power supply monitoring error monitor 0: Normal 1: Power supply monitoring error detection (cleared error result by Dummy Write to this Address)	0
4	DIF_EM	Diffuser issue error monitor 0: Normal 1: Error detection (cleared error result by Dummy Write to this Address)	0
3	OC_EM	Over current error monitor 0: Normal 1: Over current error detection (cleared error result by Dummy Write to this Address)	0
2-0	VER_REG	IC version register (Read Only) 101: ET75116	101

Address 0x25

Bit	Name	Bit definition	Initial
7-0	GL_RST	At the time of RST_DIS = 0, reset the data of the register by writing in 00000001 in Register Write; At the time of RST_DIS = 1, no reset	0000 0000

Application Note

1. APC

Laser driver calibrates to optimized output power and tr/tf performance.

During about 100μs after APC_GATE=High, ET75116 makes laser emit 4 level of light, L1/H1/L2/H2. Based on the photo diode current (PD voltage), ADC inside ET75116 stores each level of light power and makes linear curve fitting to calculate I_{BIAS} and I_{SW}. Photo diode is required to make APC function. The calculated I_{BIAS} and I_{SW} values are applied to depth measurement period and I_{BIAS} and I_{SW} are updated when APC_GATE=High. This function contributes to improve laser temperature dependency performance, laser emitting timing and output power by time-related deterioration.

*For APC correctly worked, Set APC_GATE on the following condition.

- Please set it more than 130μs for the time to DATA luminescence start from APC_GATE=High. (Start of the depth measurement).
- Please make sure APC_GATE=Low section more than 5μs.
  I_{BIAS}, I_{SW} calculation method figure by APC function:

Initial Power Calibration APC

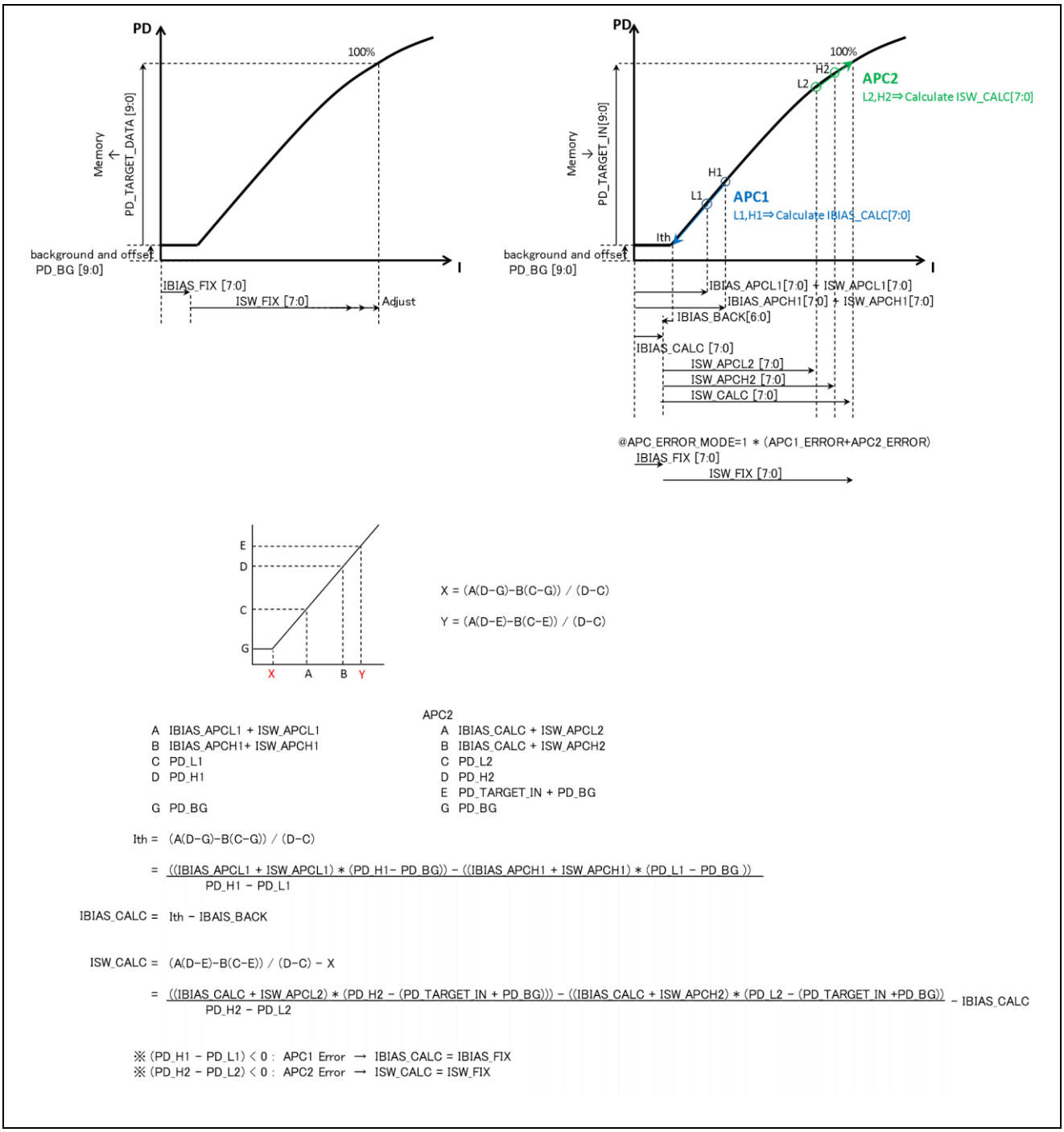


Figure 5

APC is required to take following steps

1) selection of resistor mounted on PD pad

Resistor value of PD is selected by the condition which is photo diode current multiplied by resistance is less than 2.3V at 100% output laser power. Adjustable resistor is not required.

2) Initial power adjustment

100% peak output power at depth measurement period is set by adjusting IBIAS DAC and ISW DAC, the read back AD value of photo diode current (PD voltage). At register APC_CAL = 1, ET75116 is in initial power calibration mode.

When register ADEN [1:0] = 0b11: initiate CLK inside

① When register APC_CAL = 1: output duty=50% signal to laser with 4μs (or 8μs) pulse high width

② Adjust IBIAS_FIX [7:0], ISW_FIX [7:0] to reach 100% peak output power at depth measurement period by monitoring output power. Output power at power meter is 50% duty power, so twice of the power is equivalent to 100% peak output power. I_{BIAS} current is referred to I_{TH} (threshold current) of laser specification.

③ When ADC_START [1:0] = 0b01,AD of photo diode current (PD voltage). AD value of difference between PD voltage (at 100% peak output power) and PD voltage (at no laser output, background) is stored into PD_TARGET_DATA [9:0].

④ Read back of PD_TARGET_DATA [9:0] and store value into external controller in order to send the value through SPI at power on sequence.

Initial Power Calibration

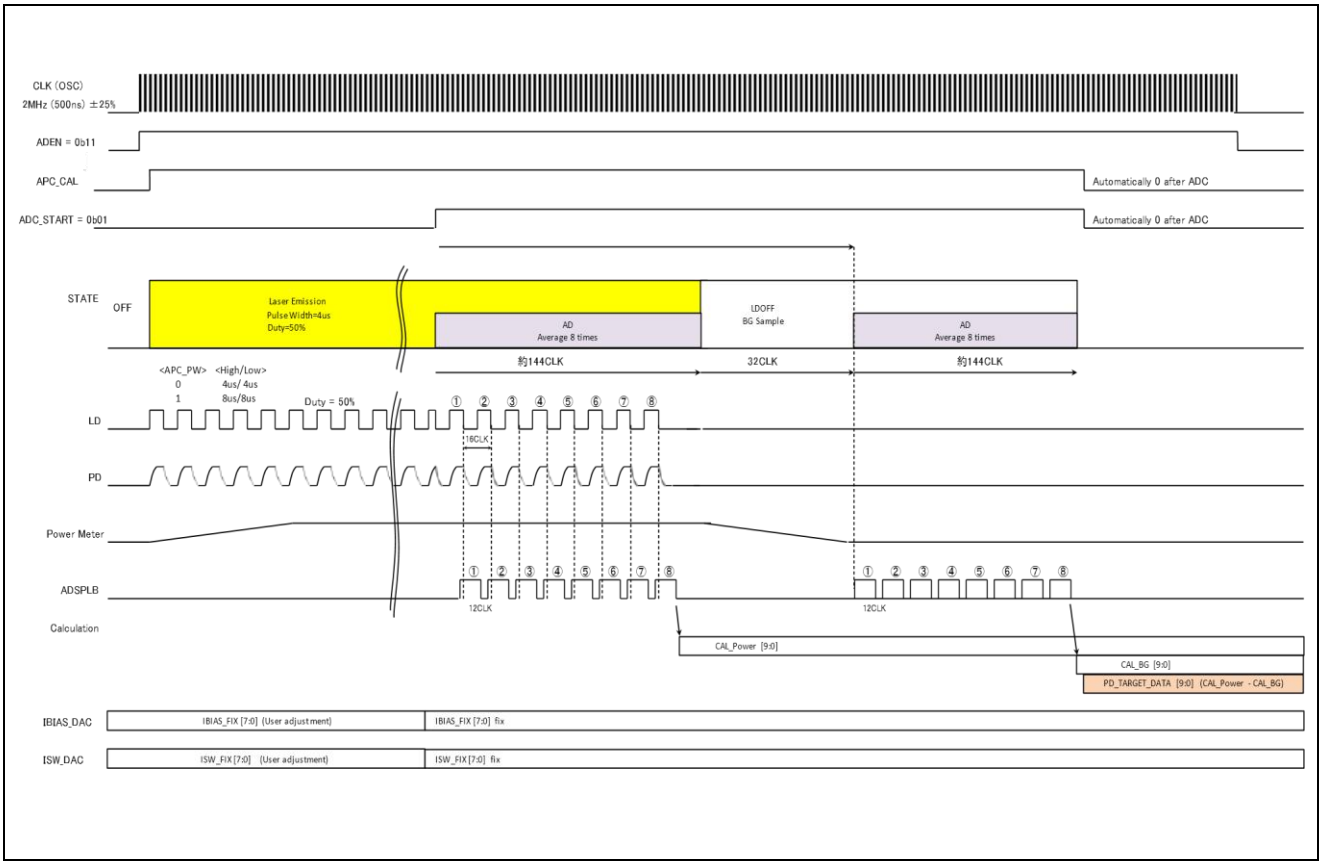


Figure 6. Initial power calibration Timing Chart

3) APC calibration and light emission for depth measurement

After APC_GATE receives high signal, ET75116 shifts to APC calibration period.

By measuring AD value of PD at laser output conditions, BIAS current and SW current are calculated. The value stored into PD_TARGET_DATA [9:0] through initial power adjustment flow is written into PD_TARGET_IN [9:0] during initial sequence. SW current is determined by adjusting photo diode voltage to PD_TARGET_IN [9:0] during APC2 period. The following steps shows work flow from APC to light emission for depth measurement. By measuring AD value at no emission (background), ambient and offset of circuit are canceled.

① Measure AD value of PD at LDOFF (no emission)

② measure AD value of PD at L1 level (I_{BIAS}_APCL1 [7:0] + ISW_APCL1 [7:0])

③ measure AD value of PD at H1 level (I_{BIAS}_APCH1 [7:0] + ISW_APCH1 [7:0])
*L1 < H1 is required

④ from ①②③ results, take linear curve fitting and calculate I_{TH} and subtract I_{BIAS}_BACK [6:0].
Finally, I_{BIAS} current is determined.

⑤ measure AD value of PD at L2 level (I_{BIAS}_APCL2 [7:0] + ISW_APCL2 [7:0])

⑥ measure AD value of PD at H2 level (I_{BIAS}_APCH2 [7:0] + ISW_APCH2 [7:0])
*L2 < H2 is required.

⑦ from ⑤⑥ results, I_{SW} current is determined by adjusting PD voltage at I_{BIAS} + I_{SW} to PD_TARGET_IN [9:0] + PD_BG [9:0].

⑧ with calculated I_{BIAS} current condition, check AD value of PD if it's correctly set.

⑨ with calculated I_{BIAS} current + I_{SW} current condition, check AD value of PD if it's correctly set.

If there is not any issue on results of ⑧ and ⑨, ET75116 shifts from APC calibration period to normal depth measurement state. If it detects error, register APC_ERR_MODE set off of LDOUT or activate LDOUT with certain level of current which is set by IBAIS_FIX [7:0] and ISW_FIX [7:0].

If PD_H1 [9:0] – PD_L1 [9:0] is 0 or negative value at APC1 calibration period or PD_H2 [9:0] – PD_L2 [9:0] is 0 or negative value at APC2 calibration period, it's possible to set LDOFF, send error signal to XEMOUT, and store error flag into specific register address.

During ①~⑨, ET75116 cannot receive signal input through SPI. APC calibration period is about 100μs.

pulse width of emission at APC can be set to 4μs or 8μs is select-able by APC_PW register.

APC_MODE [1:0] register can set on or off of APC1(I_{BIAS} calculation) and APC2(I_{SW} calculation).

If APC calibration is set to off, IBIAS_FIX [7:0] and ISW_FIX [7:0] register values are applied to drive current to laser.

APC & DATA Emission

- Luminous amplitude 4μs (APC_PW = 0)

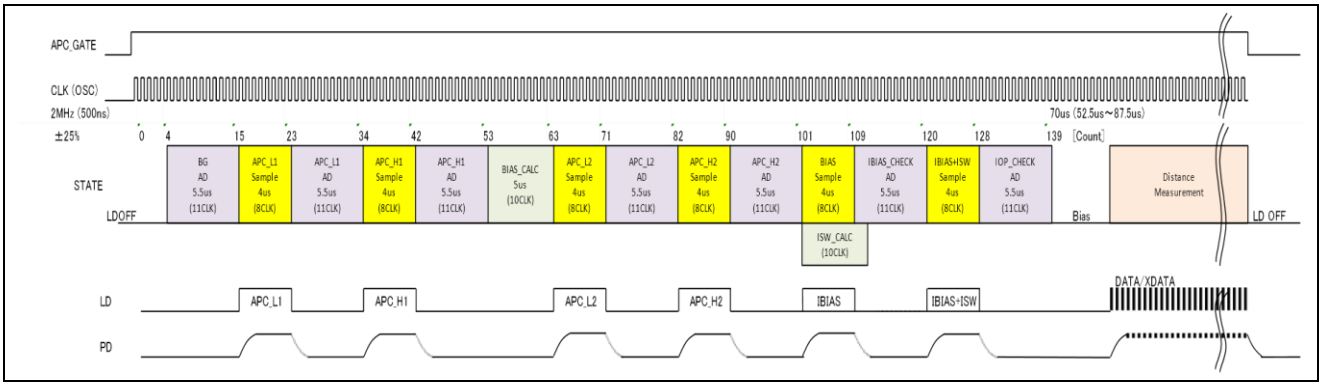


Figure 7

- Luminous amplitude 8μs (APC_PW = 1)

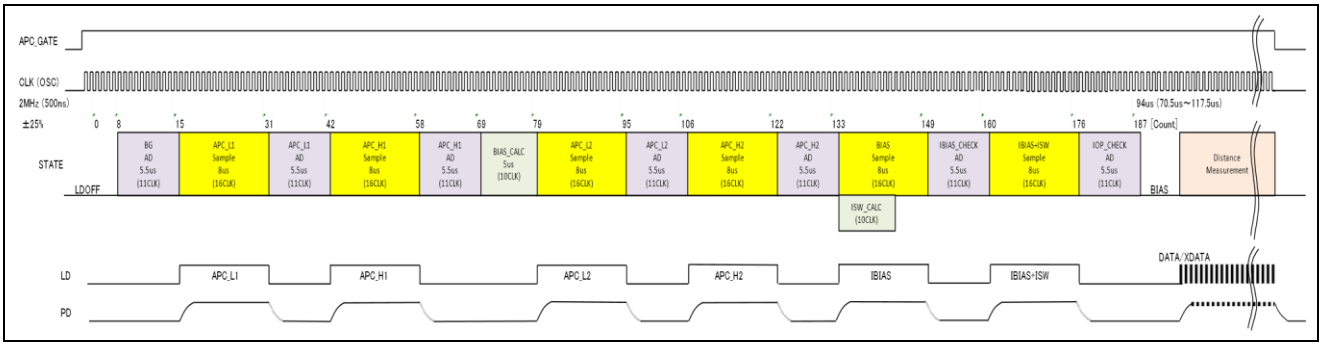


Figure 8

APC calibration and light emission for depth measurement Timing Chart

2. Temperature sensor ADC

ADC for temperature is used for either temperature sensor inside ET75116 or input of thermal resistor voltage through AUX_ADC pad. ADSEL register can be set either case. It's required to take initial calibration to cancel offset.

1) Initial calibration

To cancel circuit or thermal resistor offset, under 25°C condition it's requited to measure AD value of temperature sensor and store the value into peripheral memory which is used at initial setting.

① Set 296dec (AD expectation value at 25°C) to TEMP_CAL_IN [9:0] register.
(if condition is different from 25°C, this calculation is applied and set to register. 296 dec ± (5.4 [dec/°C] × difference temperature from 25°C)

② At ADEN = 0b11：internal CLK activated

③ At ADC_START = 0b10：internal AD activated, AD result is stored into TEMP_AD_DATA [9:0] register. after completing AD, automatically ADC_START is set to 0b00.

④ read back TEMP_AD_DATA [9:0] register and store into peripheral memory.

2) Temperature sensor function work flow

① At initial setting, stored value into peripheral memory is set into TEMP_CAL_IN [9:0] through SPI

② At ADEN = 0b11：internal CLK activated

③ At ADC_START = 0b10：internal AD activated, AD result is stored into TEMP_AD_DATA [9:0] register. after completing AD, automatically ADC_START is set to 0b00.

④ Read back TEMP_AD_DATA [9:0] register and store into peripheral memory.

At ①, ET75116 takes offset cancel and adjust 25°C=296 dec.

Temp Sensor ADC

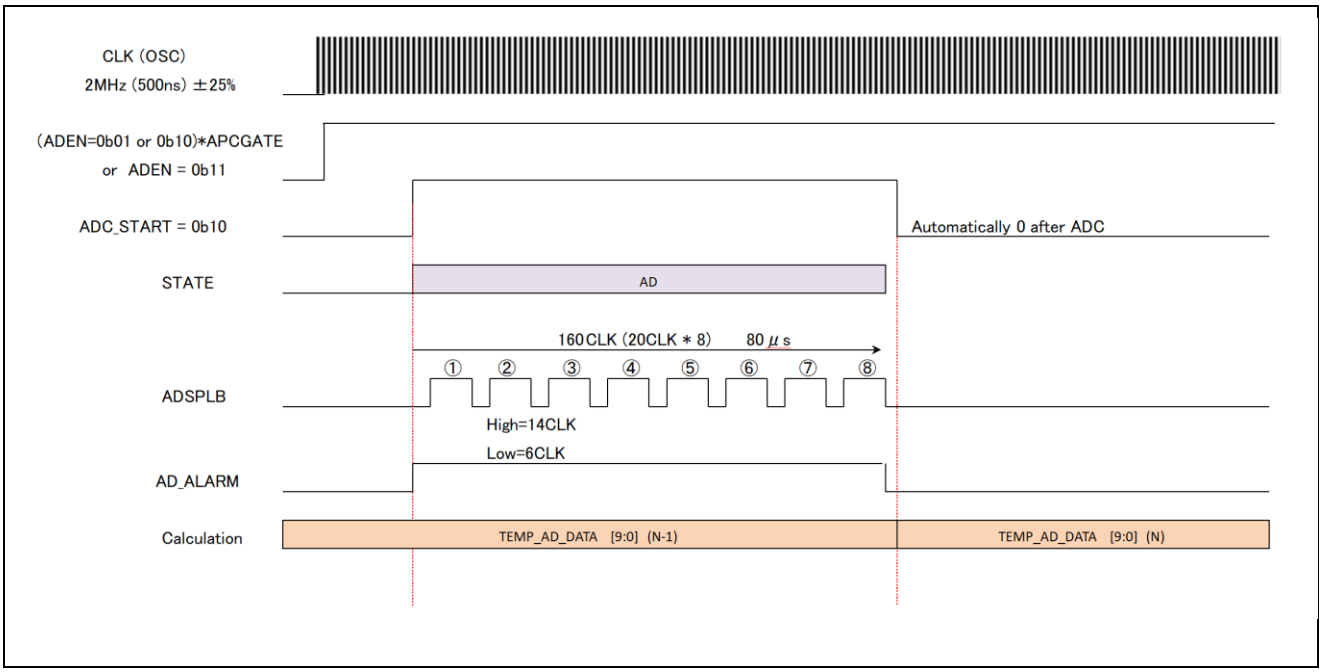


Figure 9

3. Emergency Detection Function

Emergency detection function is for power supply monitor, over current, diffuser removal detection, APC1 error, and APC2 error. When ET75116 detects abnormal phenomena by taking OR or all of functions, then ET75116 takes followings,

- force control of LDOFF (no signal output to laser)
- send signal to XEMOUT pad (Low effective at error detected case)
- error flag is stored into register (1 is for error case, possible to reset by dummy write to the register)

each detection function can be set on or off by register setting except power supply monitor function. Error flag stored into register is kept after error is even canceled. To reset error flag, dummy write of register or global reset are required.

Emergency Detection Function

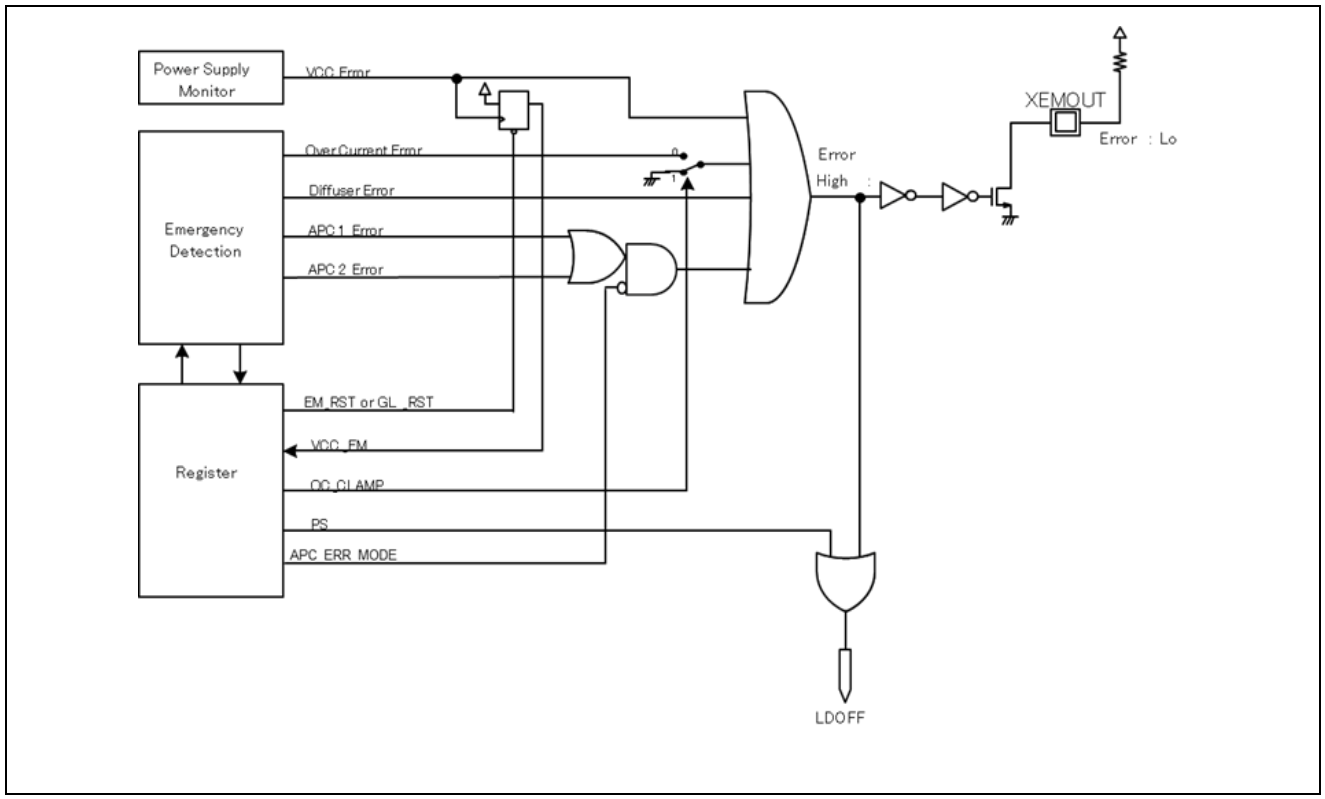


Figure 10.

Stored register of Emergency Error flag

(Error flag is reset by dummy write to each address)

Bit	7	6	5	4	3
Name	APC2_EM	APC1_EM	VCC_EM	DIF_EM	OC_EM
0:	Normal				
1:	Error				

1) Power Supply Monitor

Power Supply Monitor function monitors AV_{CC33} voltage in operating. When the voltage is under 2.5V, it becomes error.

Once it recovers to over 2.65V, error signals of LDOFF and XEMOUT are reset. However, error flag stored into register is kept.

2) Over Current

Over current function monitors I_{BIAS_CALC} [7:2] and I_{SW_CALC} [7:0] APC which are calculated by APC. OC_SEL [1:0] set over current threshold level and when I_{BIAS_CALC} [7:2] + I_{SW_CALC} [7:0] is larger than equivalent of threshold level of OC_SEL[1:0], it becomes error.

OC_SEL [2:0]	Over Current threshold level
000	3.0 A (I_{BIAS_CALC} [7:2] + I_{SW_CALC} [7:0] = 233dec)
001	2.6 A (I_{BIAS_CALC} [7:2] + I_{SW_CALC} [7:0] = 200dec)
010	2.2 A (I_{BIAS_CALC} [7:2] + I_{SW_CALC} [7:0] = 167dec)
011	1.8 A (I_{BIAS_CALC} [7:2] + I_{SW_CALC} [7:0] = 133dec)
100	1.4A (I_{BIAS_CALC} [7:2] + I_{SW_CALC} [7:0] = 107dec)
101	1.0A (I_{BIAS_CALC} [7:2] + I_{SW_CALC} [7:0] = 80dec)
110	0.7A (I_{BIAS_CALC} [7:2] + I_{SW_CALC} [7:0] = 53dec)
111	Function OFF

Register OC_CLAMP controls LDOUT and XEMOUT output in error case. When OC_CLAMP = 1 and Over Current is occurred, the current to laser is clamped to over current threshold level instead of LDOFF and error flag is sent to XEMOUT pad. However, error flag is stored into register, OC_EM.

OC_CLAMP	LDOFF, XEMOUT control at Over Current detection
0	LDOFF, send error signal to XEMOUT, error flag stored into OC_EM register
1	Clamp to threshold level current (no LDOFF), no output error signal at XEMOUT, error flag stored into OC_EM register

3) Diffuser Removal Detection

Diffuser Removal Detection function monitors AD value of PD voltage which is calculated by APC calibration (I_{BIAS} + I_{SW}). When the AD value is less than PB_B[9:0] (Background) + 128dec, ET75116 detects error. This detection is activated during APC calibration period.

DIF_ERR_SEL[1:0]	Diffuser Removal Detection
00	error at less than PB_B[9:0] (Background) + 128dec
01	error at less than PB_B[9:0] (Background) + 64dec
10	error at less than PB_B[9:0] (Background) + 32dec
11	Function OFF

4) APC1 error

APC1 error function monitors AD value of PD with I_{BIAS} calculated at APC1 period. This detection is activated during APC calibration period.

APC1_ERR_SEL	Detect I_{BIAS} error at APC1
0	Error at I_{BIAS} < 0 at APC1 or PD ADC is larger than PD_B [9:0] + 64dec
1	Function OFF

5) APC2 error

APC2 error function monitors AD value of photo diode with I_{BIAS}+I_{SW} calculated at APC1 and APC2 period. AD value is compared to PD_TARGET_IN [9:0]. This detection is activated during APC calibration period.

APC2_ERR_SEL	APC2 error threshold level
00	Error: Larger than PD_TARGET_IN [9:0] + PD_BG[9:0] ±64dec (6.25% of PD AD full scale)
01	Error: Larger than PD_TARGET_IN [9:0] + PD_BG[9:0] ±128dec (12.5% of PD AD full scale)
10	Error: Larger than PD_TARGET_IN [9:0] + PD_BG[9:0] ±256dec (25% of PD AD full scale)
11	Function OFF

6) APC_ERR_MODE

APC_ERR_MODE controls output of LDOUT pad and output to XEMOUT when APC1 error or APC2 error. Register APC_ERR_MODE controls LDOUT and XEMOUT.

APC_ERR_MODE	Output control at APC1 or APC2 error
0	Off at LDOUT and Low at XEMOUT
1	LDOUT with BIAS_FIX [7:0] and ISW_FIX [7:0] current condition, no error signal at XEMOUT, error flag stored into register

7) Output processing at the time of the abnormal detection function and error outbreak

				Output processing at the time of the error outbreak					
				APC_ERR_MODE = 0			APC_ERR_MODE = 1		
Item	**Sub item**	**Contents**	**Effective / invalidity selection of the detection function**	**LDOUT output**	**XEMOUT output**	**Register error flag**	**LDOUT output**	**XEMOUT output**	**Register error flag**
APC1_ ERROR	APC1 operation error	PD_H1[9:0] - PD_L1[9:0] ≤0 : ERROR APC1 operation result overflows : ERROR	always effective	LDOFF	Error output Low	Error output 1	LDON The current which was set in IBIAS_FIX [7:0] ,ISW_FIX[7:0]	Error output High	Error output 1
	APC1_CHECK	Operated Ith is smaller than 0; or When PD ADC results in APC1 check (IBIAS) ≥ PD_B[9:0] + 64dec	APC1_ERR_SEL = 0 Detection function existence effect	LDOFF	Error output Low	Error output 1	LDON The current which was set in IBIAS_FIX[7:0], ISW_FIX[7:0]	Error output High	Error output 1
			APC1_ERR_SEL = 1detection function is invalid	error does not occur When I_{th} is smaller than 0, I output 0					

				Output processing at the time of the error outbreak					
				APC_ERR_MODE = 0			APC_ERR_MODE = 1		
Item	**Sub item**	**Contents**	**Effective / invalidity selection of the detection function**	**LDOUT output**	**XEMOUT output**	**Register error flag**	**LDOUT output**	**XEMOUT output**	**Register error flag**
APC2_ ERROR	APC2 operation error	PD_H2[9:0] - PD_L2[9:0] ≤0 : ERROR APC2 operation result overflows : ERROR	always effective	LDOFF	Error Output Low	Error output 1	LDON The current which was set in IBIAS_FIX[7:0], ISW_FIX[7:0]	Error output High	Error output 1
	APC2_CHECK	Operated ISW_CALC is smaller than 0; or When judge an error of PD_ADC and (PD_TARGET_IN + PD_BG) in APC2 check (IBIAS+ISW)	APC2_ERR_SEL[1:0] ≠ 2'b11 Detection function existence effect	LDOFF	Error Output Low	Error output 1	LDON The current which was set in IBIAS_FIX[7:0], ISW_FIX[7:0]	Error output High	Error output 1
			APC2_ERR_SEL[1:0] = 2'b11 detection function is invalid	error does not occur					

			Output processing at the time of the error outbreak					
			OC_CLAMP = 0			OC_CLAMP = 1		
Item	**Contents**	**Effective / invalidity selection of the detection function**	**LDOUT output**	**XEMOUT output**	**Register error flag**	**LDOUT output**	**XEMOUT output**	**Register error flag**
OC ERROR	monitor quantity of output current by IBIAS_FIX + ISW_FIX setting 3.0A / 2.6A / 2.2A / 1.8A /1.4A /1.0A / 0.7A	OC_SEL [2:0] ≠3'b111 Detection function existence effect	LDOFF	Error output Low	Error output 1	CLAMP at the output current upper limit with the threshold of OC_SEL[1:0]	Error output High	Error output 1
		OC_SEL [2:0] = 3'b111 detection function is invalid	error does not occur					

			Processing at the time of the error		
Item Diffuser ERROR	Contents PD AD result in APC2 check (IBIAS+ISW) ≦ PD_BG[9:0] + 128dec / 64dec / 32dec	Effective / invalidity selection existence effect	LDOUT	XEMOUT Low	Register Error 1
		DIF_ERR_SEL[1:0] = 2'b11 detection function is invalid	error does not occur		

			Processing at the time of the error		
Item	**Contents**	**Effective / invalidity selection of the detection function**	**LDOUT output**	**XEMOUT output**	**Register error flag**
VCC ERROR	monitor the VCC voltage	always effective	LDOFF	Error Output Low	Error output 1

4. laser output assist function

Due to PCB board design and LD load, LD emission waveform has sag and distortion. AS_I function is capable to compensate sag and AS_W and Tr_AS functions compensate distortion.

(Adjustment flow)

① evaluate LD emission waveform with AS_I, AS_W, Tr_AS default values .

② flattening of sag with AS_I compensation function .

③ adjust AS_W,Tr_AS for distortion.

LDD current waveform / LD emission waveform

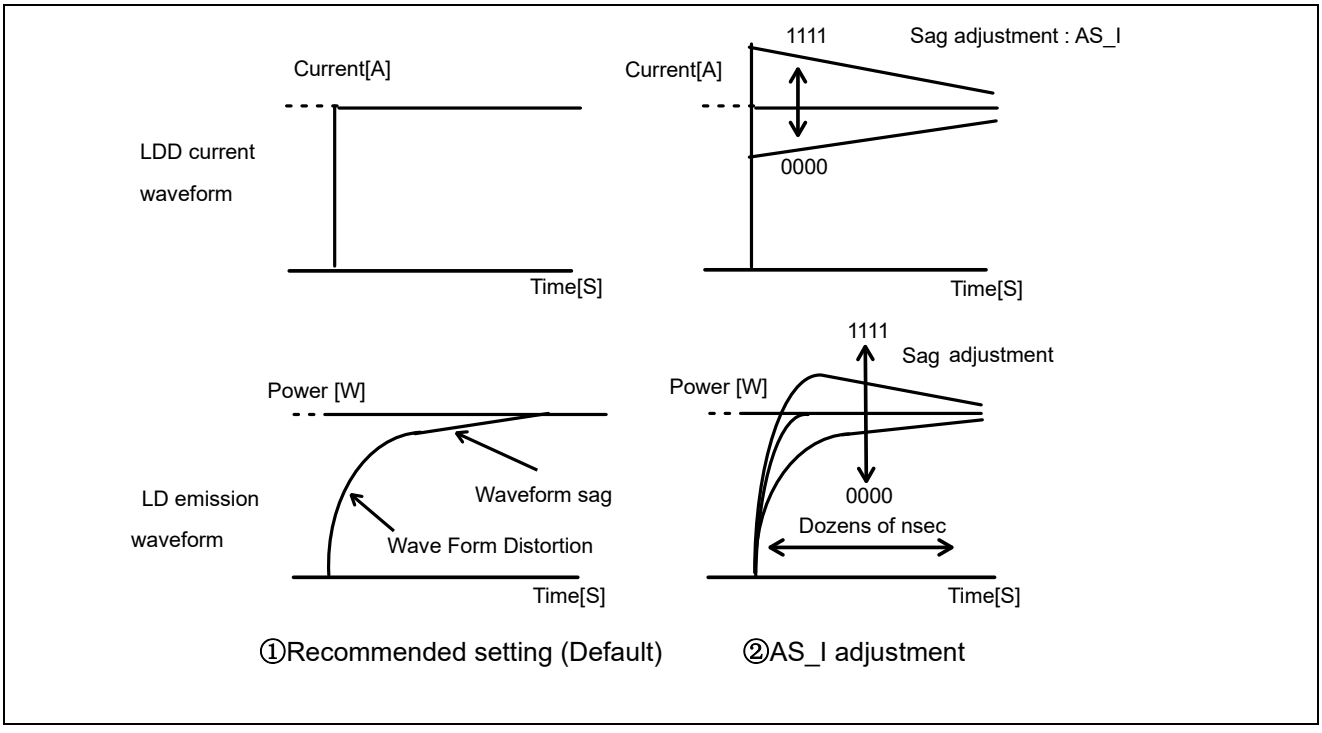


Figure 11

LDD current waveform / LD emission waveform

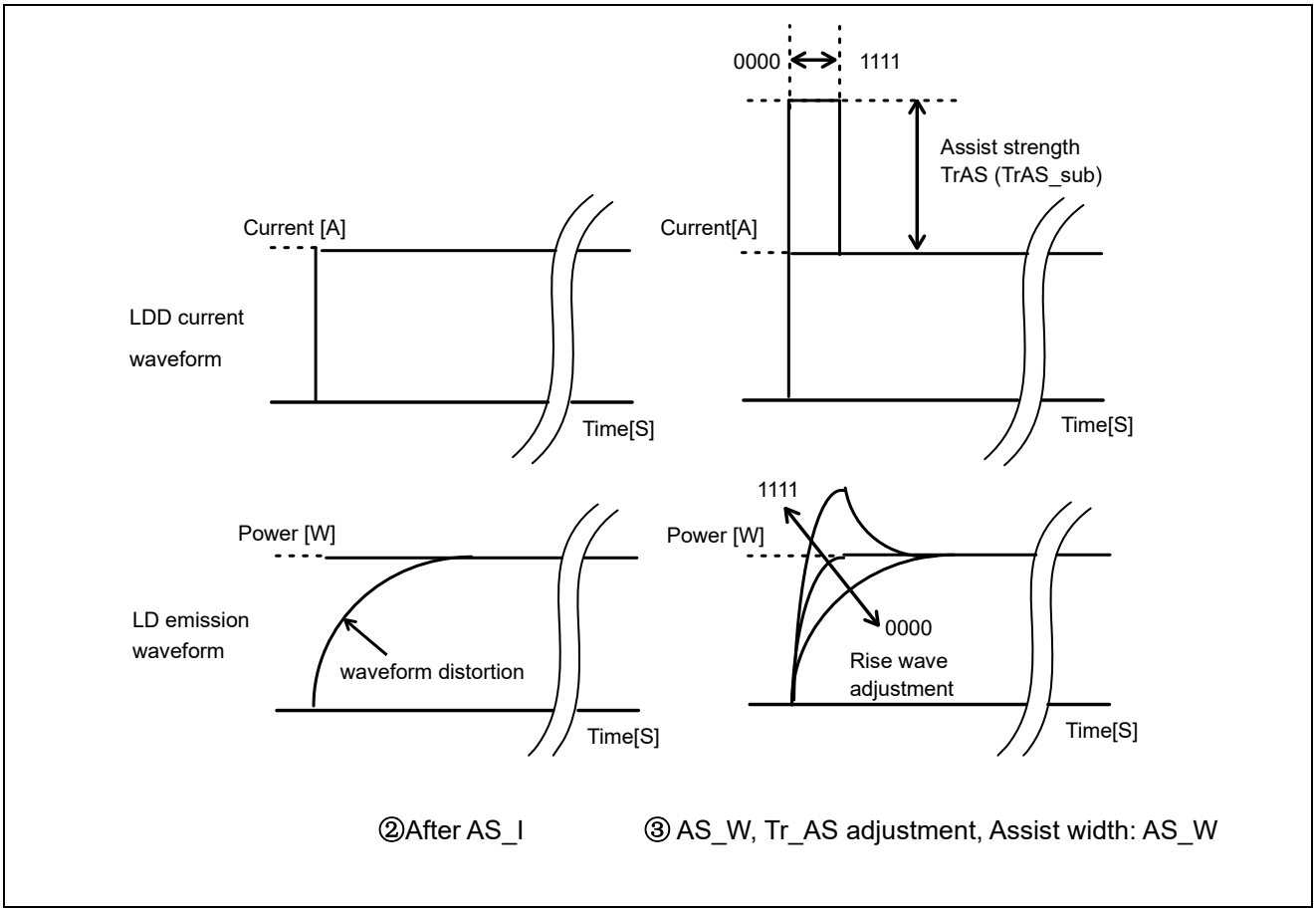


Figure 12

PMS MODE

PMS stands for Proximity Sensor. It reuses TOF VCSEL and receives control signals from pin A1, named PMSctr. The TOF mode or PMS mode can be selected through register programming,bit0 of register 0x12 is the PMS enable bit.

PMSctr is a rectangular wave, compatible with high level of 1.2V (when VCC18 = 1.2V or 1.8V), operating at frequencies between 20KHz and 60KHz, with duty cycle of 30% to 50%， high effective. If the high-level time exceeds 70us, the VCSEL will shut down until power is restarted or error flag bit1 of register 0x12 is cleared. The propagation delay from PMSctr to LDOUT is less than 10ns. A1 pin is a high-impedance input over 1Mohm.

Absolute Maximum Ratings

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. (T_A=25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage 1	V_{CC}	AV_{CC33}, DV_{CC33},			4.5	V
	V_{CC18}	V_{CC18}			2.7	V
Supply Voltage 2	LDV_{CC}	LDV_{CC}			6	V
Input Pin Voltage	V_{IN1}	DATA, XDATA PD, AUX	-0.5		4.5	V
	V_{IN2}	APC_GATE	-0.5		2.7	V
		SCLK	-0.5		2.7	V
		SDIO	-0.5		2.7	V
		SEN	-0.5		2.7	V
		PMSctr	-0.5		2.7	V
Output Pin Voltage	V_O	XEMOUT	-0.5		4.5	V
		SDIO	-0.5		2.7	V
	V_{OLD}	LDOUT	-0.5		6	V
Allowable Power Dissipation	P_D				1	W
Storage Temperature	T_{STG}		-65		+150	°C
Junction Temperature	T_J		-40		+150	°C
Electrostatic Discharge Capability	V_{ESD}	Human Body Model	±2			kV
		Charged Device Model	±0.5			kV

Recommended Operating Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage V_{CC33}	V_{CC33}	AV_{CC33}, DV_{CC33}	3.0	3.3	3.6	V
Supply Voltage V_{CC18}	V_{CC18}	Vcc18=1.8V	1.65	1.8	1.95	V
		Vcc18=1.2V	1.08	1.2	1.32	
Supply Voltage LDV_{CC}	LDV_{CC}	LDV_{CC}	3.0	3.3	5.5	V
Operating Frequency	F_{OP}				200	MHz
Operating Temperature	T_A		-40		+85	°C

Electrical Characteristics

(T_A=-40°C~85°C, AV_{CC33} = DVcc3 = LDV_{CC} = 3.3V, V_{CC18} = 1.2V/1.8V)

Current consumption

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
1	V_{CC33} supply current 1 (Power Save)	I_{CC33_1}	DEEP_SLEEP = 1	2	4	10	μA
2	V_{CC33} supply current 2 (Standby)	I_{CC33_2}	PS_MODE = 0, APCGATE = L	1.9	2.4	2.9	mA
3	V_{CC33} supply current 3 (Laser emission)	I_{CC33_3}	ADEN = 1, APCGATE = H LDOUT Current 3A Not including LDOUT Current	18	23.5	29	mA
4	LDV_{CC} supply current (Laser emission)	I_{CCLDV}				1	μA
5	V_{CC18} supply current	I_{CC18}				1	μA

CMOS Logic

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
6	Input Voltage High Level	V_{SH}	V_{CC18}=1.2V,SCLK,SEN, SDIO, APCGATE	0.9		V_{CC18}	V
			V_{CC18}=1.2V/1.8V, PMSctr				
			V_{CC18}=1.8V;SCLK,SEN, SDIO, APCGATE	1.2		V_{CC18}	
7	Input Voltage Low Level	V_{SL}	V_{CC18}=1.2V;SCLK,SEN, SDIO, APCGATE	0		0.4	V
			V_{CC18} = 1.2V/1.8V, PMSctr				
			V_{CC18}=1.8V,SCLK,SEN,SDIO, APCGATE	0		0.5	
8	Input Current High Level 2	I_{SH1}	SCLK, SEN, APCGATE (VSH = 1.2V/1.8V)	6	9	12	μA

CMOS Logic(Continue)

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
9	Input Current Low Level 1	I_{SL1}	SCLK, SEN, APCGATE (VSL = 0V)	-1	0	1	μA
10	Input Current2	I_{SL2}	SDIO	-1	0	1	μA
11	Output Voltage High Level	V_{OSH}	SDIO IOH = -2mA	V_{CC18}-0.4	-	V_{CC18}	V
12	Output Voltage Low Level	V_{OSL}	SDIO, XEMOUT I_{OL} = 2mA	0	-	0.4	V

LVDS Input

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
13	Maximum Operating Frequency	F_{MAX}		200	-	-	MHz
14	Input Voltage Range	V_{DR_L}		0.5	0.8	1.9	V
15	LVDS Differential Input Amplitude	V_{DTH_L}		0.1	0.15	1	V

LVDS

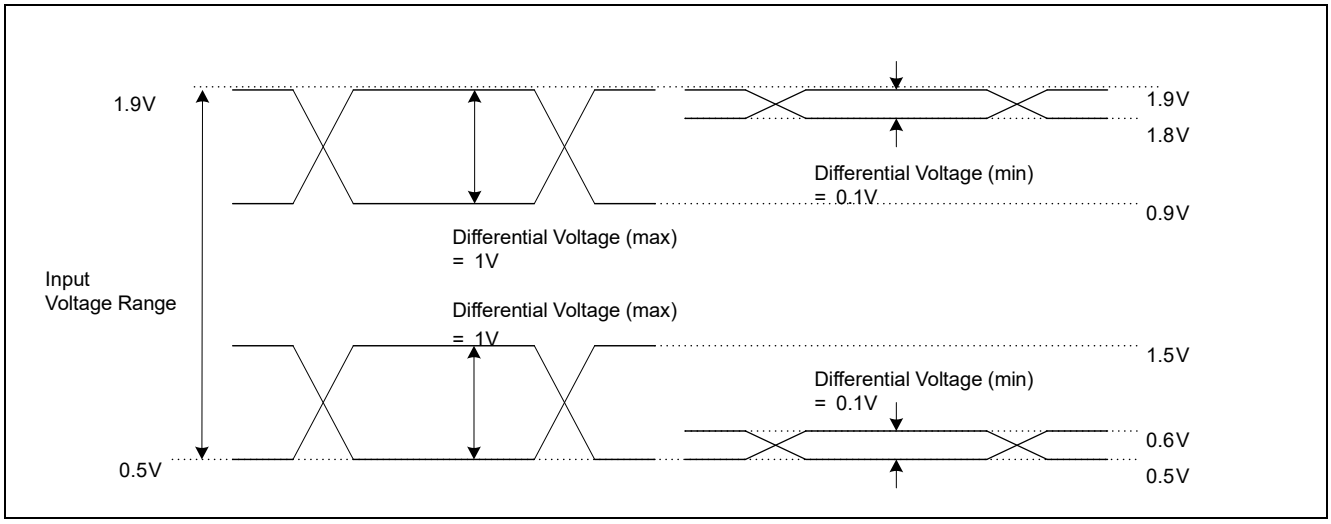


Figure 13

Serial Interface

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
16	SCLK Operating Frequency	F_{SCLK}				10	MHz
17	SCLK “H” Pulse Width	T_{WHSC}		26			ns
18	SCLK “L” Pulse Width	T_{WLSC}		26			ns
19	SEN Setup Time	T_{SSE}		30			ns
20	SEN Hold Time	T_{HSE}		100			ns
21	SEN “L” Time	T_{WLSE}		52			ns
22	SDI Setup Time	T_{SSDI}		30			ns
23	SDI Hold Time	T_{HSDI}		30			ns
24	SDO Output Delay Time	T_{DSDO}				30	ns

Serial Interface Timing

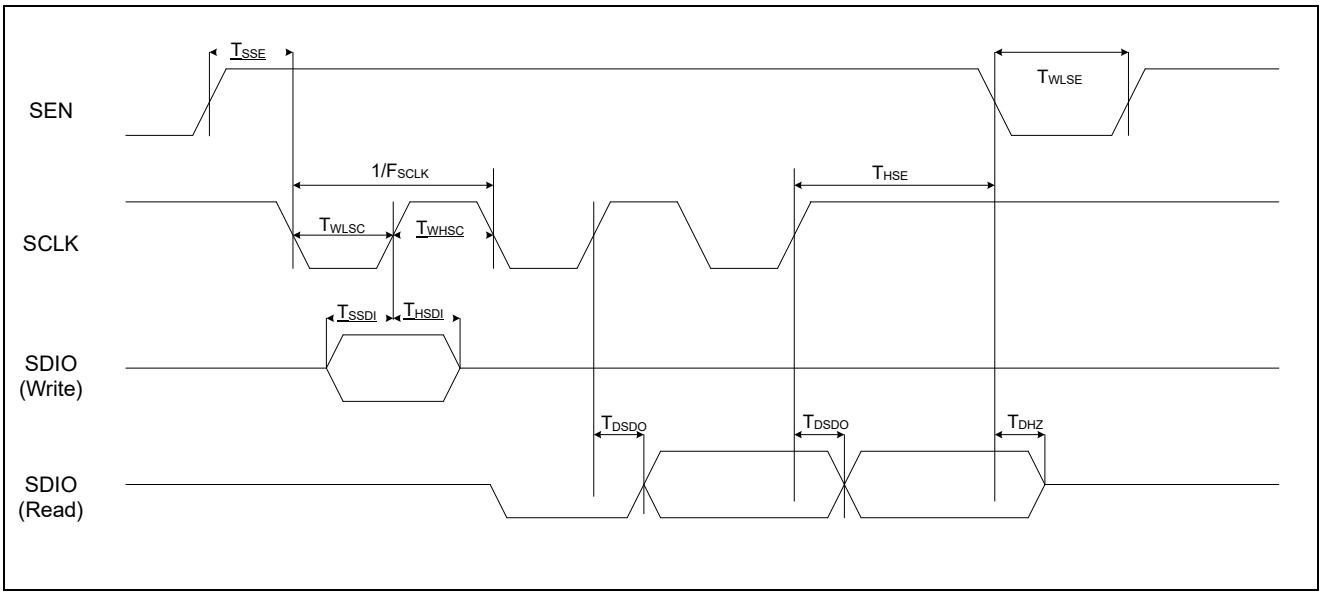


Figure 14

LD Driver Characteristics

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
25	I_{SW} current full scale	I_{SWF}	V_{CC33} = 3.3V, LDOUT = 1V ISW_DAC = 1111 1111		3.18		A
26	Bias current full scale	I_{BF}	V_{CC33} = 3.3V, LDOUT = 1V I_{BIAS}_DAC = 1111 1111	0.8	0.92	1.1	A
27	Rise time	T_R	Bottom = 0.3A, Top=2A 10 % - 90 % LDOUT pin load condition 1.5V + (0.2Ω//1000pF)		1.0		ns
28	Fall time	T_F			1.0		ns
29	Propagation Delay	D_{IDD}	LVDS ~ LDOUT 50% Pulse width addition = 0ns		3		ns
30	Propagation Delay Temperature coefficient	D_{IDDT}	LVDS ~ LDOUT 50% Pulse width addition = 0ns		2		ps/°C

APC

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
31	PDIN Input Voltage range	V_{PDR}	As ADC input D-range	0.2	-	2.3	V
32	APC_L emission time	T_{WAPCL}		2.8	3.5	4.5	μs
33	APC_H emission time	T_{WAPCH}		2.8	3.5	4.5	μs
34	APC operation result		I_{TH} precision that was calculated by APC_L, APC_H (at Δ30dec. Over)		±1		LSB

Emergency detection

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
35	Over Current threshold	I_{THOC}	LDOUT current at which Over Current is detected, OC_SEL = 000	2.7	3.0	3.3	A
36	Power supply LDOFF (3.3V)	$V_{CCTHOFF}$	V_{CC33}: 3.3V → 0 V V_{CC33} voltage at which LDOFF results	2.2	2.45	2.7	V
37	Power supply LDON (3.3V)	V_{CCTHON}	V_{CC33}: 0V → 3.3 V V_{CC33} voltage at which LDOFF is canceled	2.35	2.6	2.85	V
38	Register reset voltage	V_{POR}	The voltage of V_{CC33} by which registers are reset		1.3	1.75	V

Temperature Sensor ADC

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
39	Temperature Error	T_{ERROR}	0°C ~ 105°C After offset adjustment	-3		3	°C
40	Resolution	T_{ADCRES}			10		Bits
41	Conversion Time	T_{CONV}	8 times Average		80		μs

Application Circuits

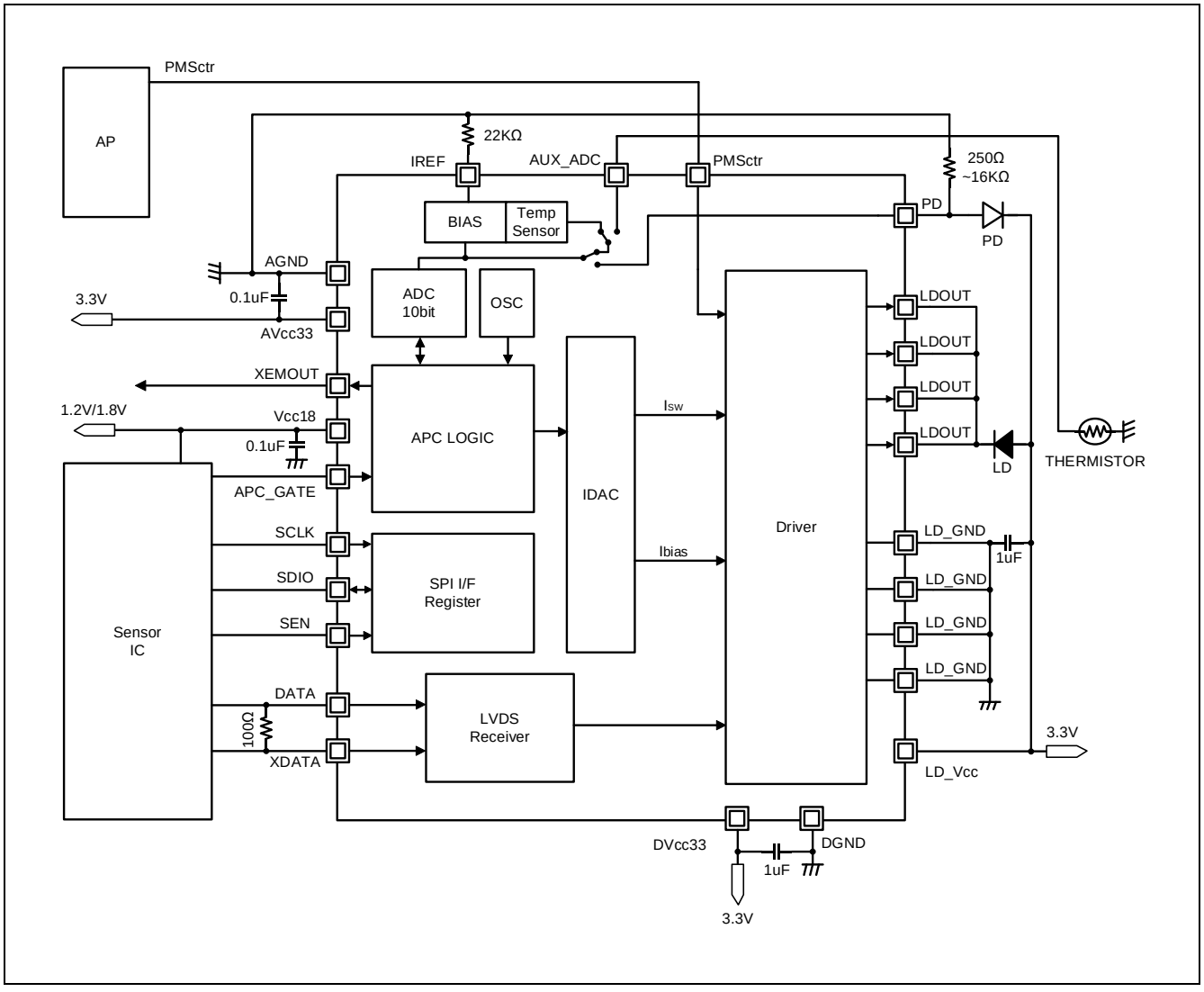


Figure 15

Reference Circuit Diagram & Board Pattern

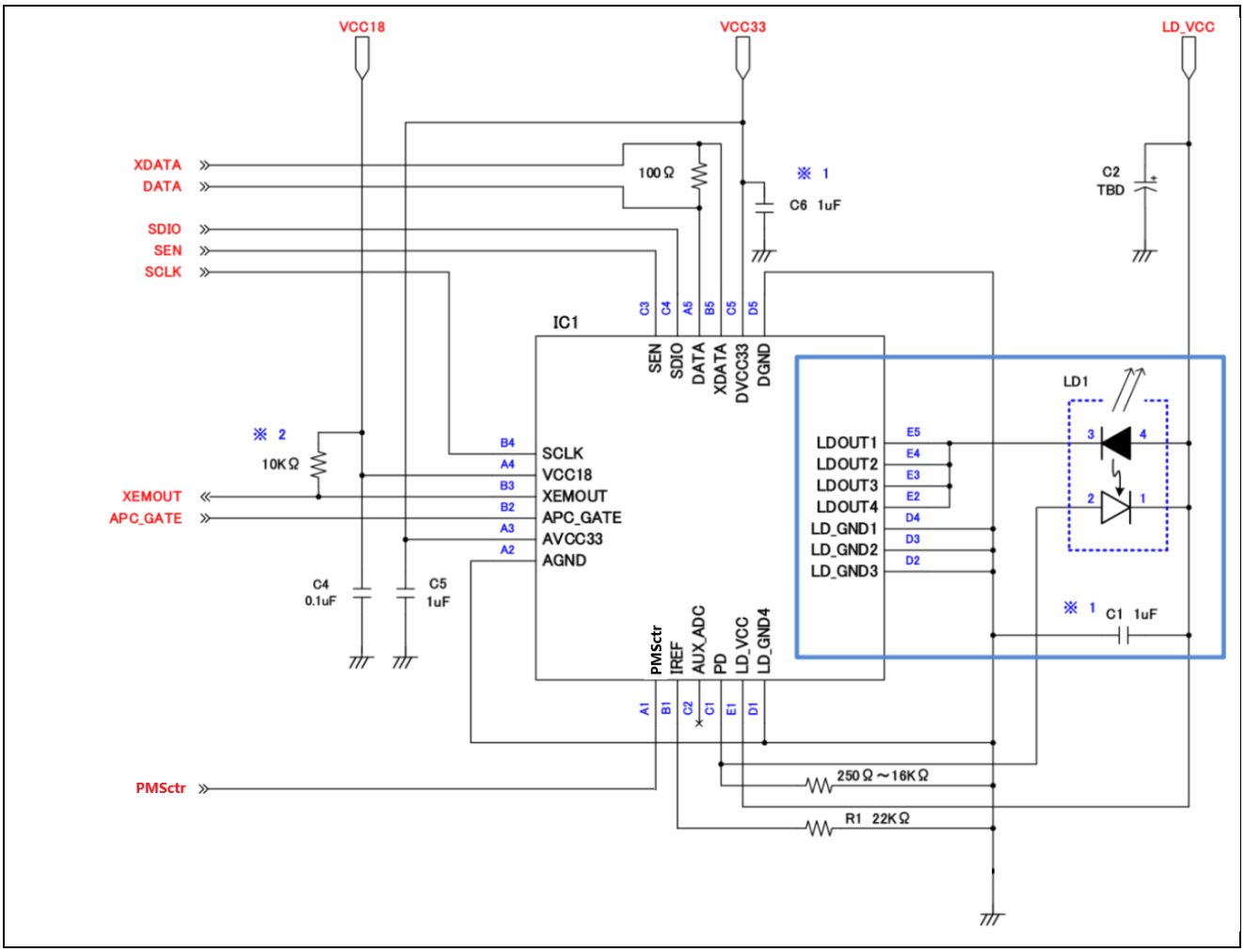


Figure 16. Circuit diagram

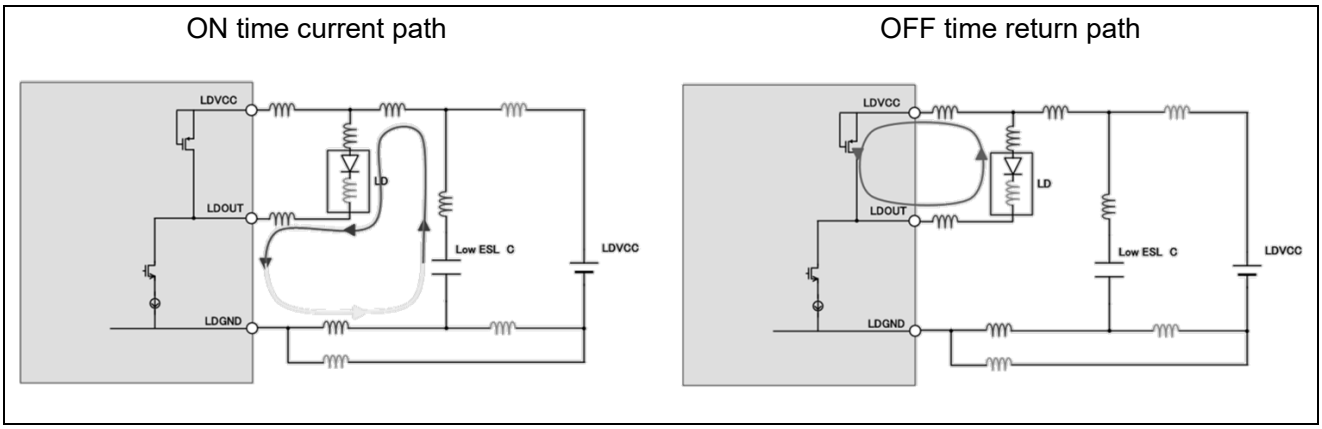


Figure 17. Return path

Using capacitor with low ESL, please place it in the shortest way between LD_VCC, LD_GND.

LDOUT and cathode of LD are the shortest and connected as wide as possible.

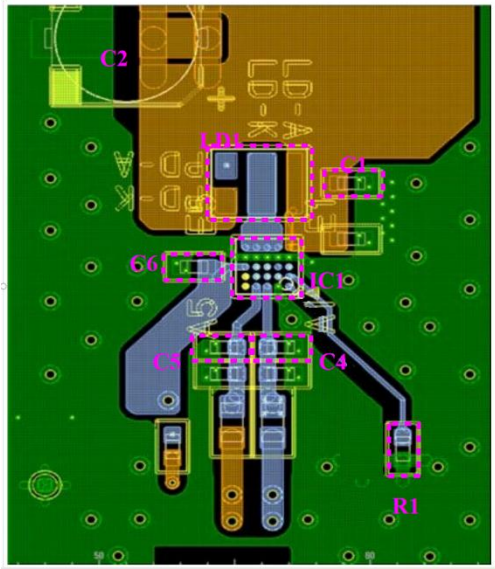
Design board parasitic inductance between LDOUT and LDVCC as small as possible.

Notes: C1 becomes the important capacitance to constitute output return path.

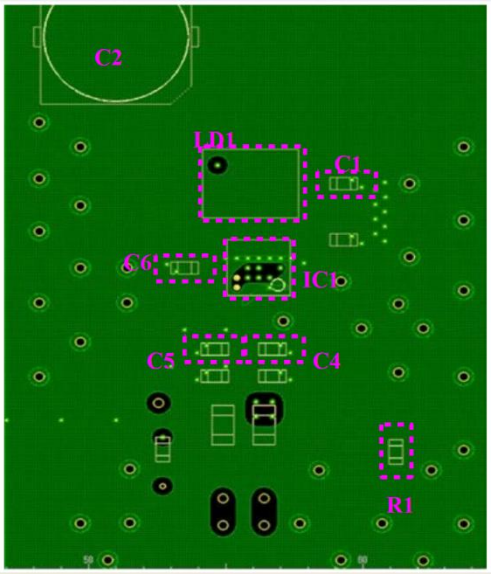
*1 recommend low ESL capacitance.

Board Pattern

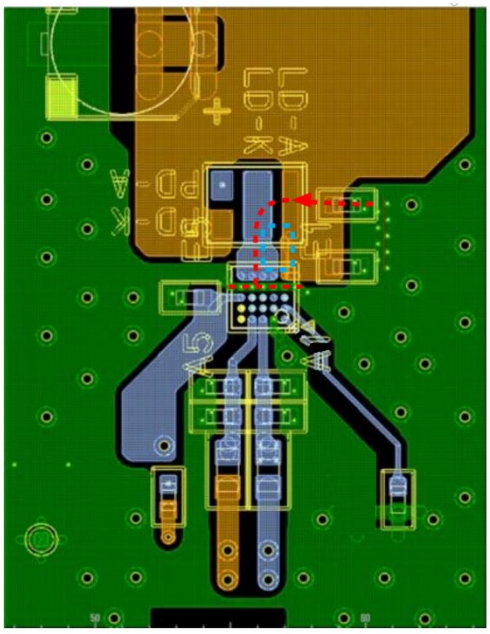
Layer 1 (Reference parts placement)



Layer 2 (Reference parts placement)



Layer 1 (Reference return path)



Layer 2 (Reference return path)

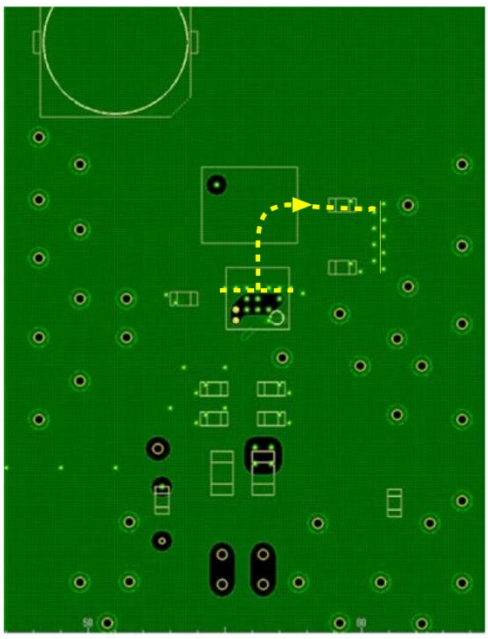


Image of return path and the mutual

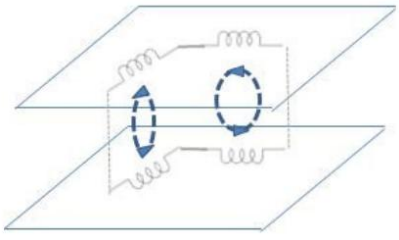


Figure 18.

Point of the board layout

Output light emission characteristic is almost decided in layer 1 and layer 2.

Return path is constructed at the time of the high current for an electromagnetic field and constitutes return path right under a driving current node like the red line and yellow line mentioned above to deny a self-inductance in a mutual inductance. Therefore, please layer 2 on GND without interruption.

The parasitic inductance becomes small by denying a self-inductance in a mutual inductance.

In addition, put connection Via on the edge of both nodes as much as possible, and please lower the impedance. Because a mutual inductance does not commit the return path constructed only in layer1, there are few effects to lower parasitic inductance.

As the mutual inductance depends on the inter-lamellar thickness of layer 1 and layer 2, layer interval recommends a thin board as much as possible.

DATA, XDATA input (LVDS input) assumes it isometric wiring, and ET75116 is latest, and please place the terminal resistance.

Please place VREF terminal connection capacitor, the IREF terminal connection resistor to the ET75116 neighborhood.

A reference pattern of mention is one case in view of the point mentioned above, and the characteristic may change by the kind of the application board and characteristics are not guaranteed.

In case of use, board inspection by the electromagnetic field simulation.

* Recommendation: Parasitic inductance is less than 1nH.

(Board parasitic inductance +LD parasitic inductance).

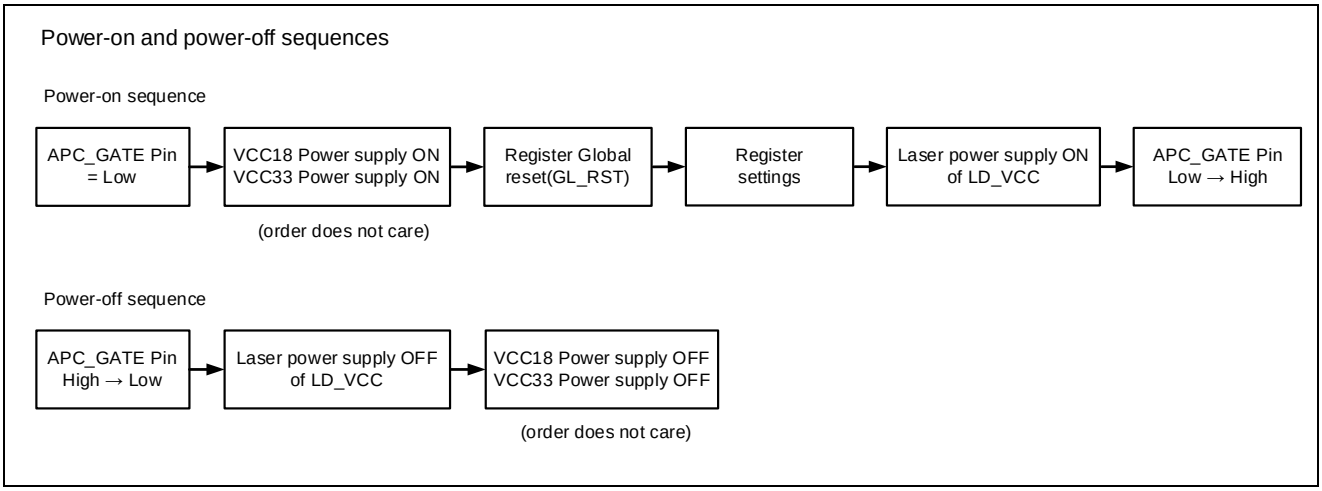
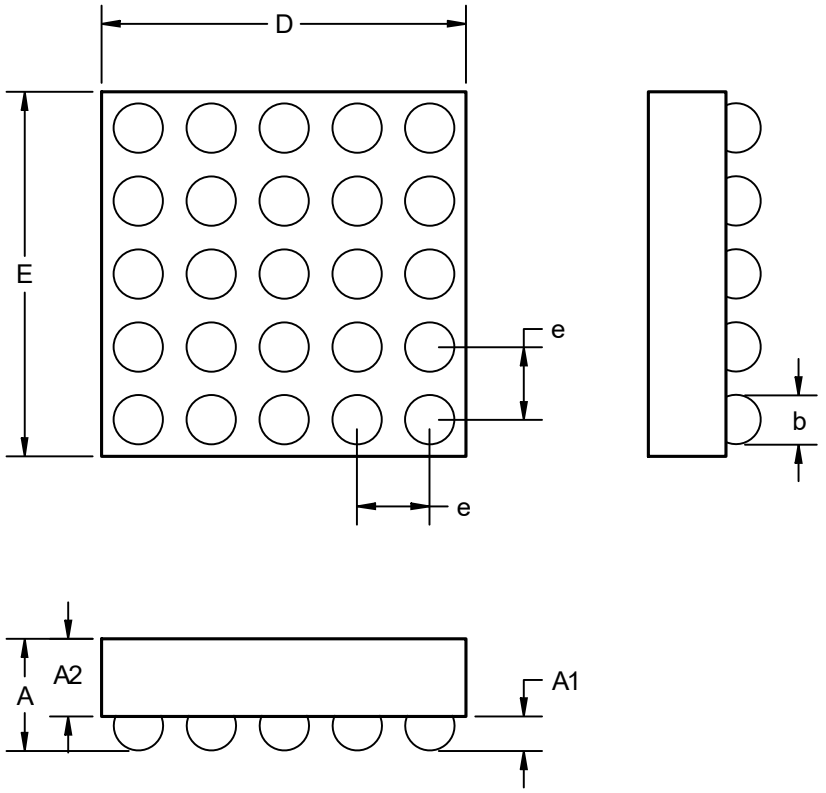


Figure 19.

Package Dimension

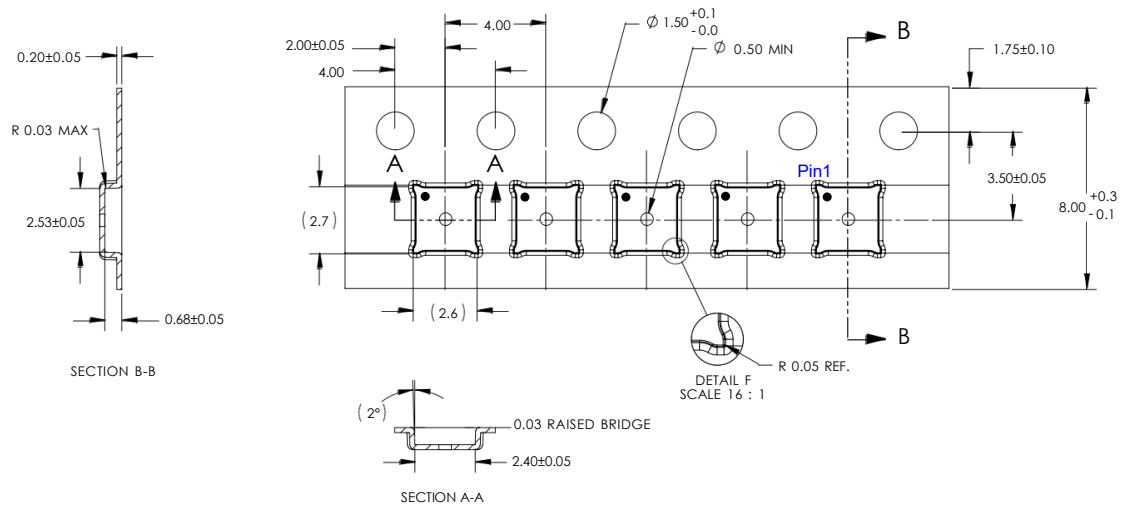
WLCSP25



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.427	0.475	0.523
A1	0.130	0.150	0.170
A2	0.297	0.325	0.353
b	0.195	0.215	0.235
D	2.270	2.300	2.330
E	2.100	2.130	2.160
e	0.400BSC		

Tape Information



Unit: mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-04-17	Original Version	Tianqh	Yumf	Liujy
1.1	2026-09-02	Add packaging	Tianqh	Yumf	Liujy