Dot Matrix LED Driver with Key Scanning

General Description

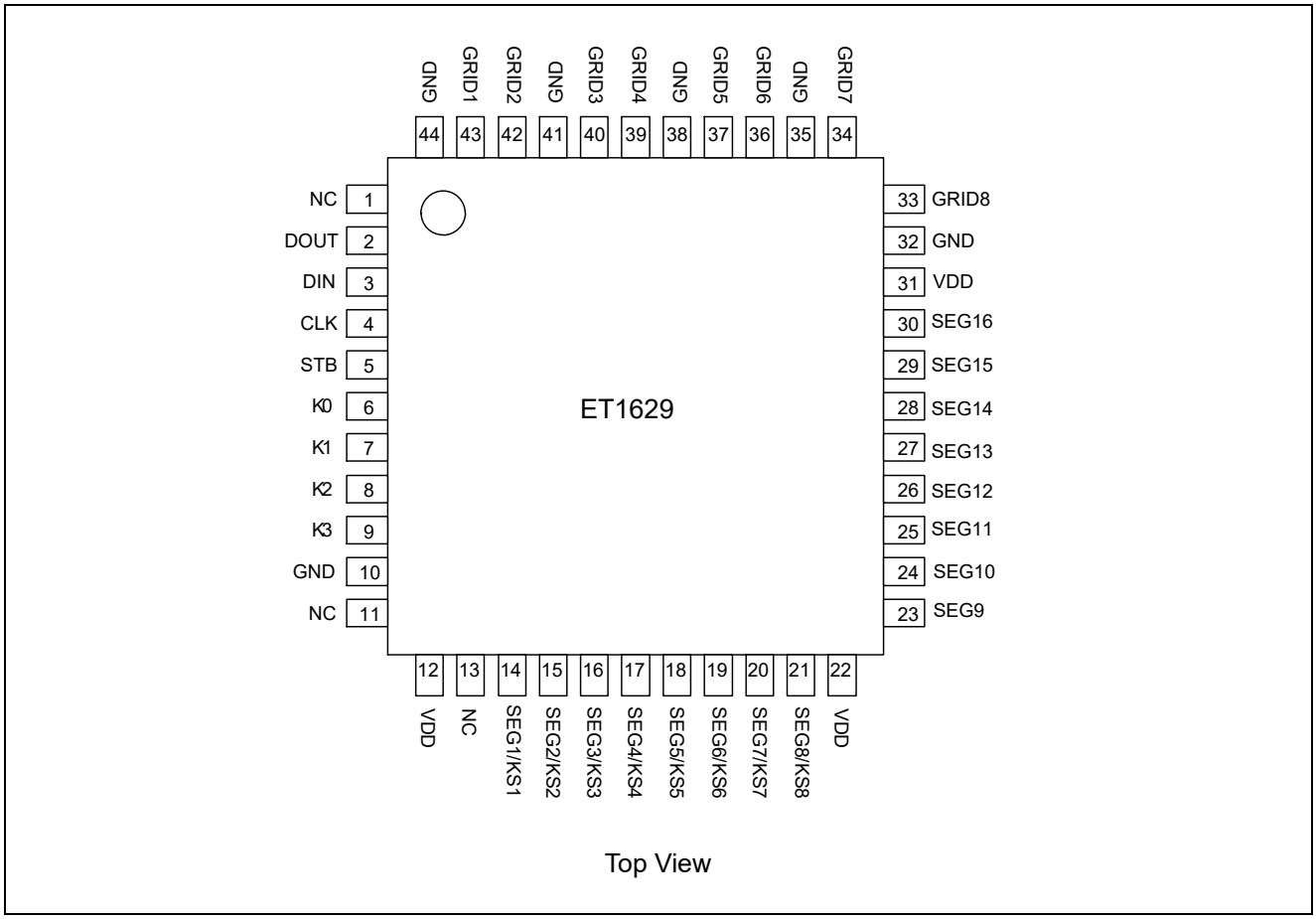
ET1629 is a high reliability matrix LED driver IC with 16 segments output (SEG), 8 commons output (GRID), display memory, control circuit, key scan circuit , using 4-line serial interface communication.

It is suitable for small LED display driver.Package is LQFP44.

Features

- Display Mode: 16Segs × 8Grids
- Keyboard Scanning: 8 × 4 Matrix
- Gray adjustment: 8 duty Cycles
- 4 wire Serial Interface
- Built in RC Oscillation
- Built in Power on Reset
- Package: LQFP44

Pin Configuration

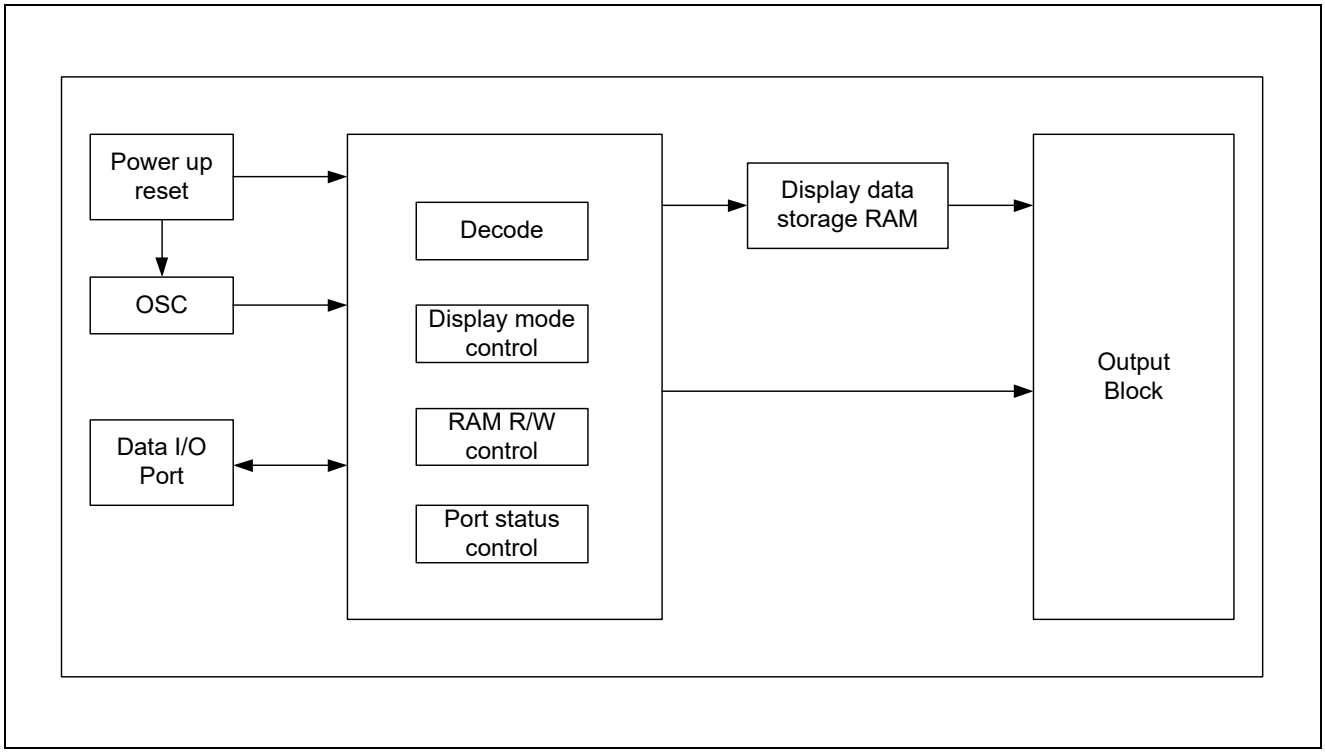


Top View

Pin Function

Pin No.	Symbol	I/O	Description
1,11,13	NC		NC
2	DOUT	O	Serial data output port.
3	DIN	I	Serial data input port.
4	CLK	I	Serial clock input port.
5	STB	I	Serial data strobe port.
6~9	K0~K3	I	Input data port for key matrix.
12,22,31	VDD	-	Power supply.
14~21	SEG1/KS1~SEG8/KS8	O	Segment output port, connect LED positive, also used as input for key scanning.
23~30	SEG9~SEG16	O	Segment output port, connected to LED positive.
33,34,36,37 39,40,42,43	GRID8~GRID1	O	Grid output port, connected to LED negative
10,32,35,38,41,44	GND	-	GND

Function Block Diagram



Functions Description

Command

When the STB port status changes from high to low, the bytes of the command (b7-b0) is input from the DIN port. If STB port is set to high for some reason during data or command transmission, serial communication is initialized and the data/command being input is considered invalid.

Command1：Display Mode Setting

ET1629's display mode format is following:

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
1	0	NC, fill in 0			0	0	0	Display duty cycle setting	Duty cycle is 1/16
1	0				0	0	1		Duty cycle is 2/16
1	0				0	1	0		Duty cycle is 4/16
1	0				0	1	1		Duty cycle is 10/16
1	0				1	0	0		Duty cycle is 11/16
1	0				1	0	1		Duty cycle is 12/16
1	0				1	1	0		Duty cycle is 13/16
1	0				1	1	1		Duty cycle is 14/16
1	0			0				Display ON/OFF setting	Display OFF
1	0			1					Display ON

Command2：Data Command Setting

ET1629's data command format is following:

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
0	1	NC, fill in 0				0	0	Data write mode	Display data input mode
0	1				0			Address increase mode	Automatic address increase
0	1				1				Fixed address
0	1			0				Test mode setting	Normal mode
0	1			1					Test mode

Command3：Display Address Setting

ET1629's display address format is following:

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Description
1	1	NC, fill in 0		0	0	0	0	Display address 00H
1	1			0	0	0	1	Display address 01H
1	1			0	0	1	0	Display address 02H
1	1			0	0	1	1	Display address 03H
1	1			0	1	0	0	Display address 04H
1	1			0	1	0	1	Display address 05H
1	1			0	1	1	0	Display address 06H
1	1			0	1	1	1	Display address 07H
1	1			1	0	0	0	Display address 08H
1	1			1	0	0	1	Display address 09H
1	1			1	0	1	0	Display address 0AH
1	1			1	0	1	1	Display address0BH
1	1			1	1	0	0	Display address 0CH
1	1			1	1	0	1	Display address 0DH
1	1			1	1	1	0	Display address 0EH
1	1			1	1	1	1	Display address 0FH

Note：Default data is 00H

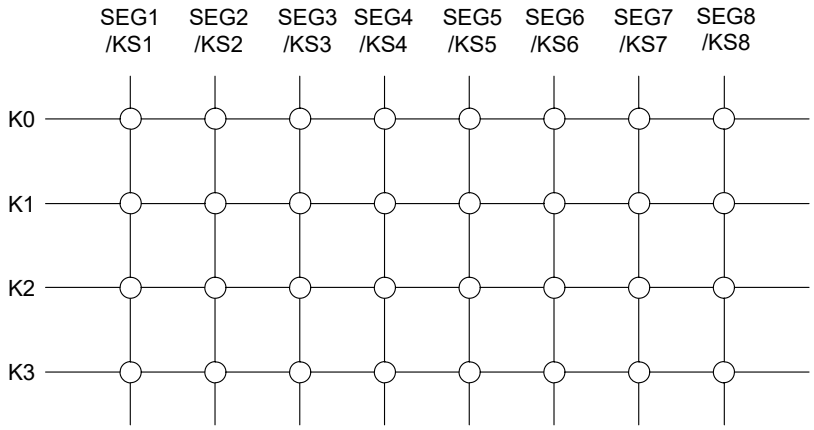
Address assignment：

SEG1~SEG4	SEG5~SEG8	SEG9~SEG12	SEG13~SEG16	GRID
00HL	00HU	01HL	01HU	GRID1
02HL	02HU	03HL	03HU	GRID2
04HL	04HU	05HL	05HU	GRID3
06HL	06HU	07HL	07HU	GRID4
08HL	08HU	09HL	09HU	GRID5
0AHL	0AHU	0BHL	0BHU	GRID6
0CHL	0CHU	0DHL	0DHU	GRID7
0EHL	0EHU	0FHL	0FHU	GRID8

Note：HL=B0、B1、B2、B3 , HU=B4、B5、B6、B7.

Key scan matrix and storage RAM

The key scan matrix of ET1629 is composed of an 8×4 array as shown below:



The key scan input data is stored as follows, and is read from the lowest bit (B0) using the READ command. The corresponding key scan data is shown in the table below:

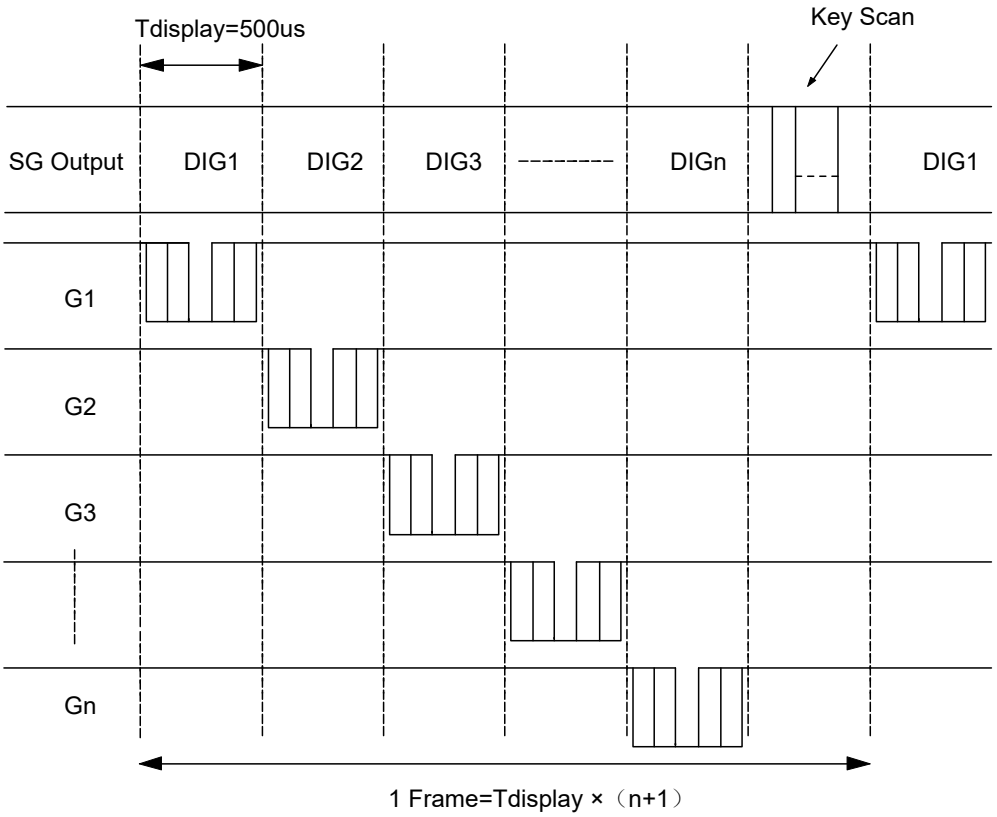
B0	B1	B2	B3	B4	B5	B6	B7	BYTE
K3	K2	K1	K0	K3	K2	K1	K0	
SG1/KS1				SG2/KS2				BYTE1
SG3/KS3				SG4/KS4				BYTE2
SG5/KS5				SG6/KS6				BYTE3
SG7/KS7				SG8/KS8				BYTE4

Read Order ↓

Note: ET1629 supports composite keys, but the same K * can only have one SEG/KS key pressed.

Display Timing

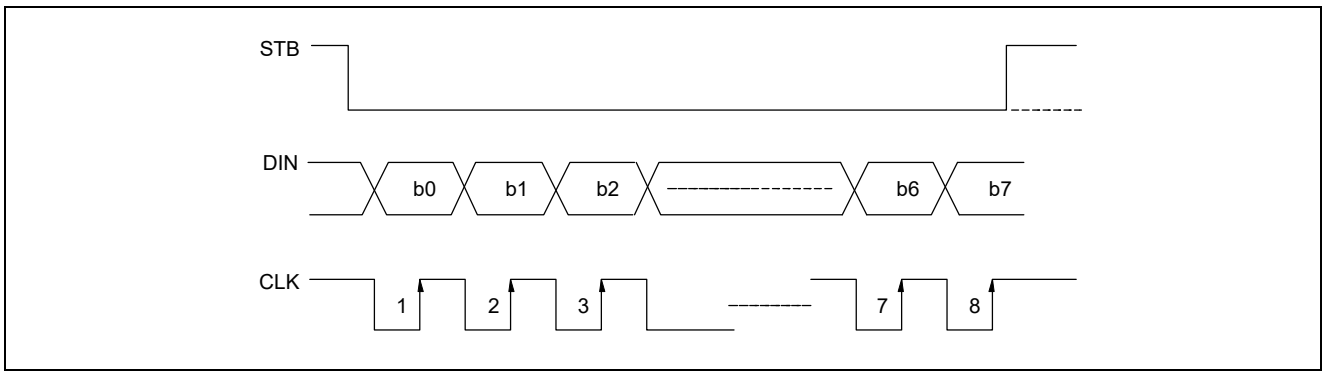
Display timing figure is following：



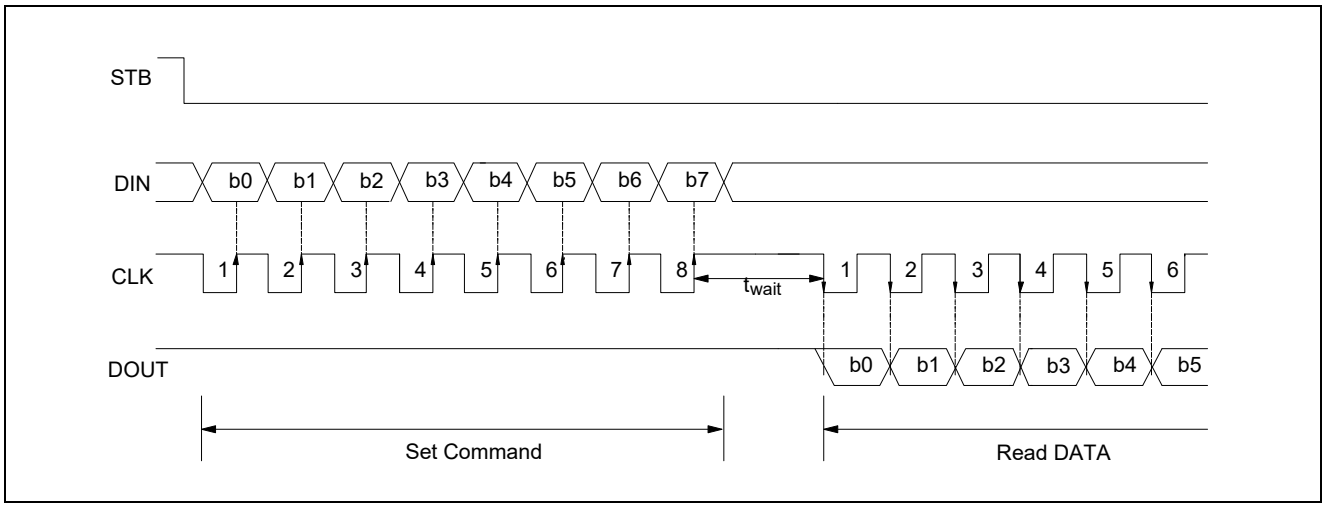
Serial Communication Format

The following figure shows the serial communication format of ET1629. It is recommended to connect a pull-up resistor (1K ~ 10K) to the DOUT port.

Transfer (data write operation)



Transfer (data read operation)

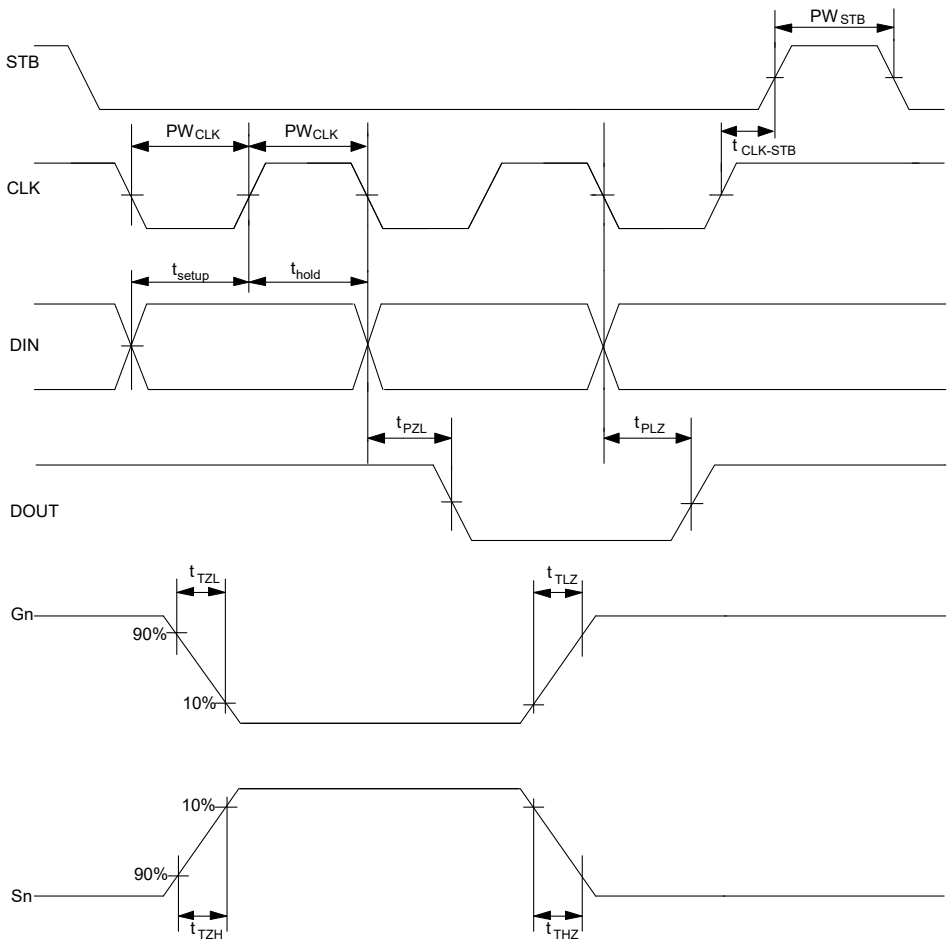


t_{wait}（Wait time）≥1μs

It should be noted that when reading data, the rising edge is the eighth clock of the instruction to the falling edge of the first clock of the subsequent data reading must be longer than or equal to 1us waiting time(T_{wait}).

Conversion Characteristic Waveform

ET1629's conversion characteristic waveform is following:



PW_{CLK}（clock pulse width）≥400ns

PW_{STB}（STB filter width）≥1μs

t_{setup}（data setup time）≥100ns

t_{hold}（data hold time）≥100ns

$t_{CLK-STB}$（clock filter time）≥1μs

t_{THZ}（dropping time）≤10μs

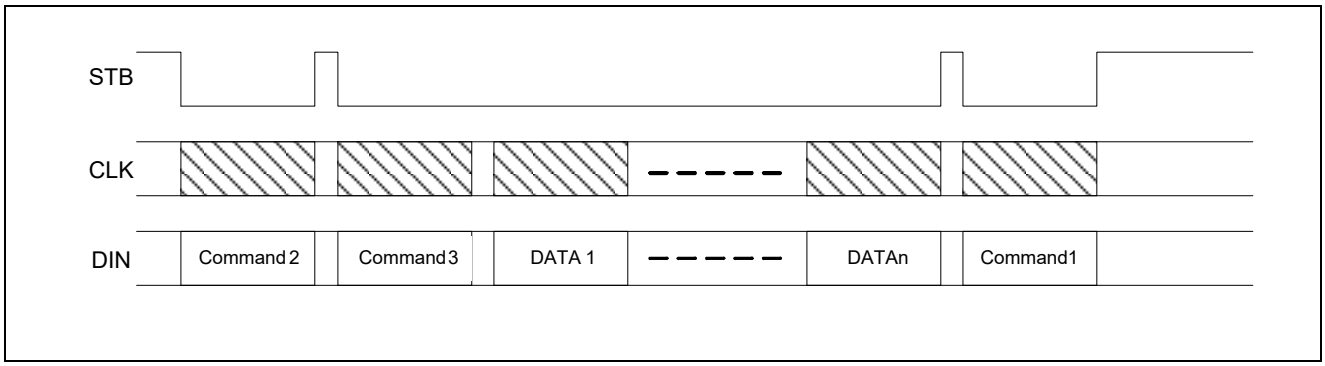
t_{TZH}（rising time）≤1μs

t_{TZL}<1μs

t_{TLZ}<10μs

Application

1. Continuous display data writing (Automatic address increase)



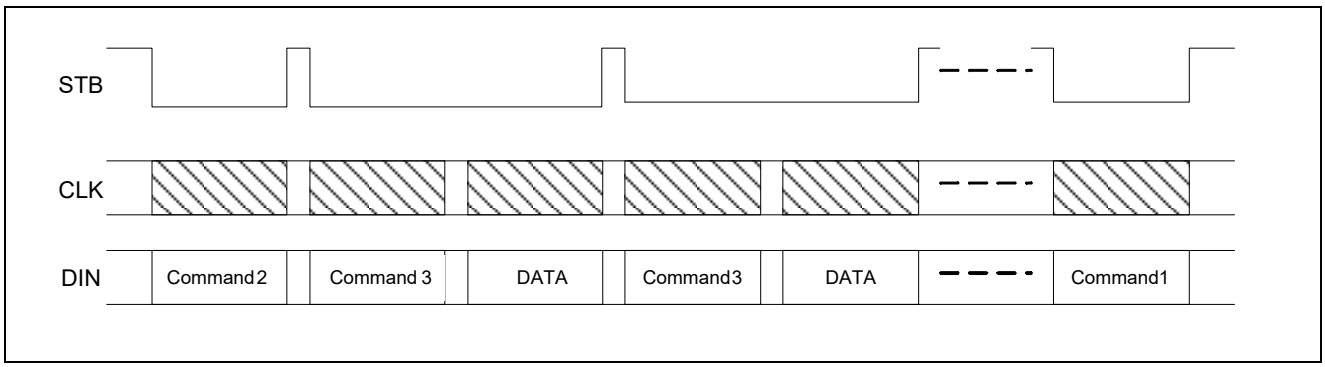
Command2：Data command setting

Command3：Address command setting

DATA1～n：Display data（MAX 16bytes）

Command1：Display mode setting

2. Single display data writing(fixed address mode)



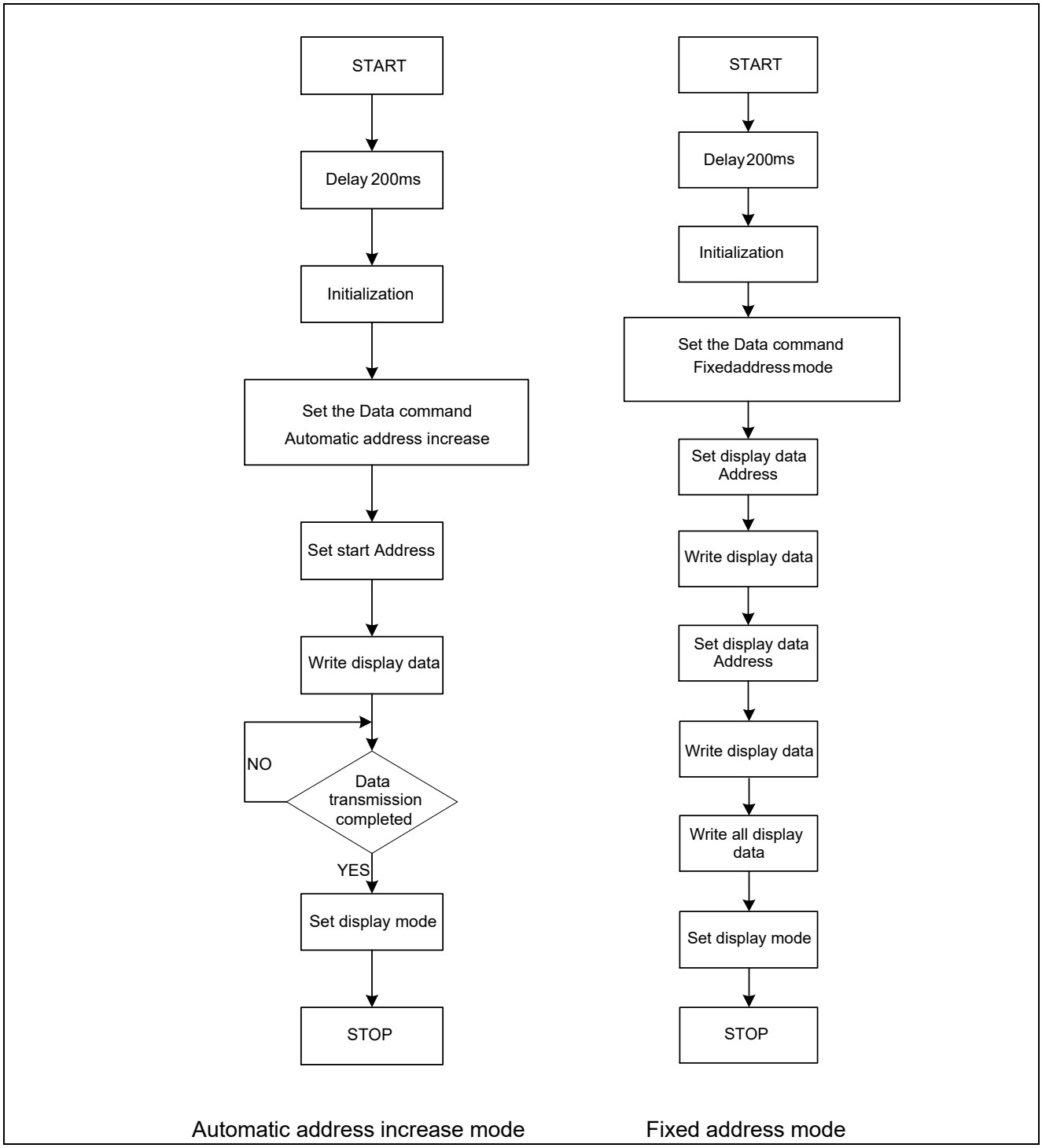
Command2：Data command setting

Command3：Address command setting

DATA：Display data

Command1：Display mode setting

Software Flow Diagram



When the IC is powered on for the first time, the contents of the display RAM are not defined, so be sure to clear the contents of the display RAM in the initialization setting.

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.5～+7	V
Logic Input Voltage	V_I	-0.5～V_{DD}+0.5	V
Driver Output Current	I_{OLGR}	+200	mA
	I_{OHSG}	-50	mA
Max Output Driver current	I_{TOTAL}	400	mA
Junction Temperature	T_J	-40～+150	°C
Storage Temperature	T_{STG}	-65～+150	°C

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Dynamic current (*)	I_{DD_DYN}			1	mA
High Level Input Voltage	V_{IH}	0.6V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}	0		0.25V_{DD}	V
Operating Temperature	T_A	-40		85	°C

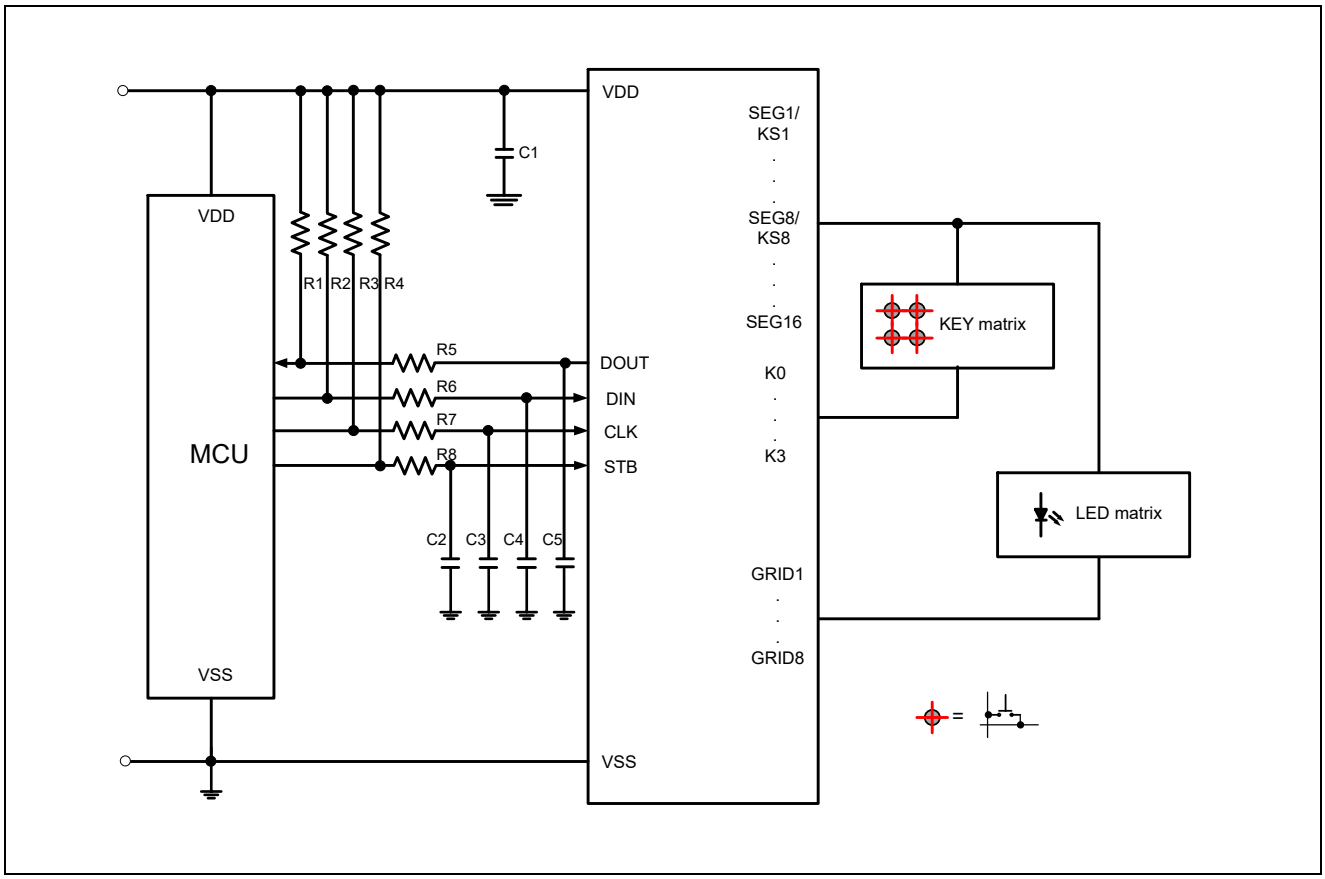
Note*：Set display mode command = 80H (display off & no load)

Electrical Characteristics

V_{DD} = 5V，GND = 0V，Ta = 25°C

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Output Current	I_{OHSG1}	V_O=V_{DD}-2V，SG1～SG16	-30	-40	-50	mA
	I_{OHSG2}	V_O=V_{DD}-3V，SG1～SG16	-40	-50	-60	mA
Low Level Output Current	I_{OLGR}	V_O=0.3V，GR1～GR8	80	110	—	mA
High Level Input Voltage	V_{IH}	—	0.6V_{DD}	—	5	V
Low Level Input Voltage	V_{IL}	—	0	—	0.25V_{DD}	V
Refresh Frequency	F_{FLASH}			200		Hz
K1～K3 Pull Down Resistor	R_{KN}	K1～K3, V_{DD}=5V		10		kΩ

Application Example



Notes：

1. This application circuit is only for reference.

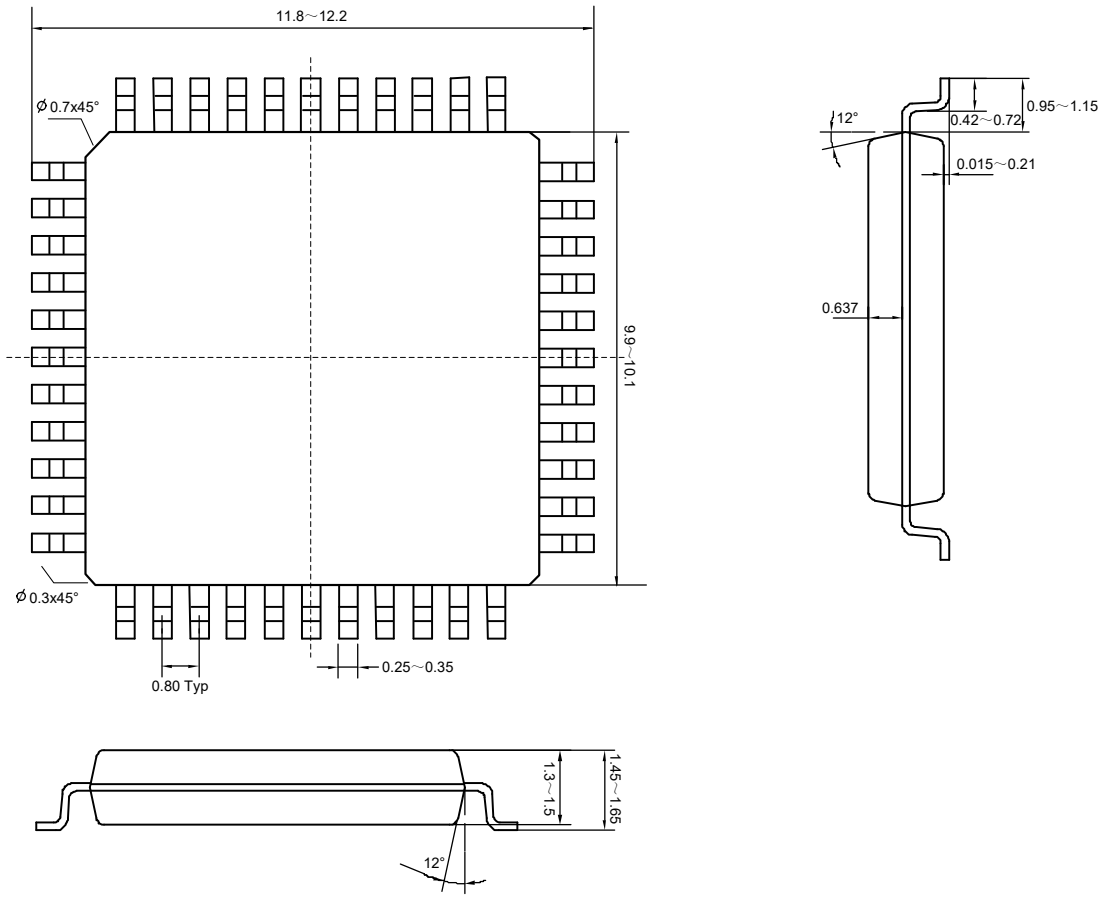
2. C1=1uF and should be placed as close as possible to the VDD.

3. R1~R4 = 4.7kΩ, R5~R8 = 100Ω, C2~C5 = 100pF.

4. The series resistance of the communication port and the capacitor for GND should be placed as close as possible to ET1629, and the resistance value and capacitance value should be adjusted according to the actual anti-interference requirements and verification results.

Package

LQFP44



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2020-02-24	Original Version	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.1	2024-5-15	Update Typeset	Shi Bo	Shi Liang Jun	Shi Bo