

## Voltage Detector IC

### General Description

The ET9823A is a micro-power voltage detector IC used to monitor the multiple power supplies in microprocessor or logic system. It has high-accuracy, low current consumption and adjustable delay. It performs supervisory function by sending out a reset signal whenever the VDD voltage falls below a present threshold level, and sending out another power detect signal whenever the VCC1, VCC2, or VCC3 power off. Once supplies recovered the threshold level, the reset and power detect signal will be released after a certain delay time controlled by external capacitor.

### Features

- Internal Fixed Threshold
- High Accuracy  $\pm 2\%$
- Low Supply Current  $3\mu\text{A}$
- N-Channel Open-Drain Output
- Low Function Supply Voltage 1.6V
- Delay Time controlled by External Capacitor
- Used to Multiple Supplies Application
- Fully Specified Over Temperature

### Applications

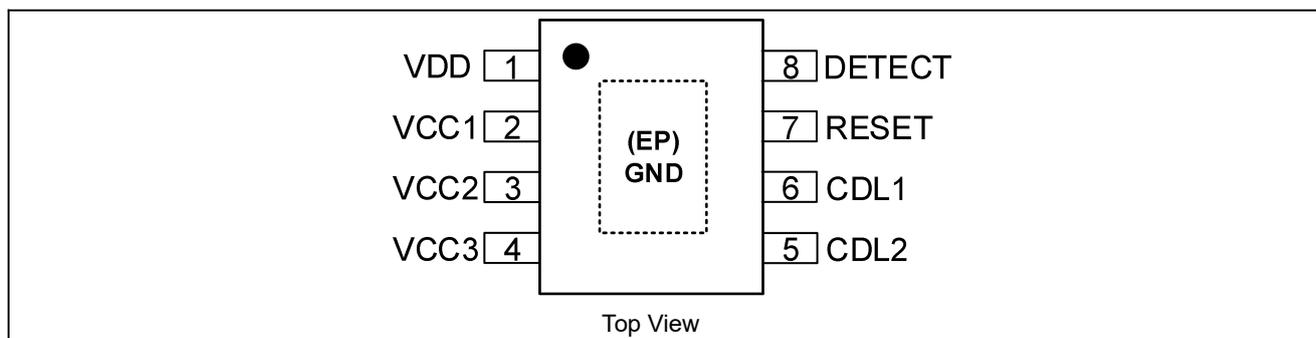
- Computers
- Intelligent Instruments
- Portable/Battery-Powered Equipment

# ET9823A

## Device information

Part No.	Package	Packing Option	MSL
ET9823A	ESOP8	Tape and Reel	3

## Pin Configuration

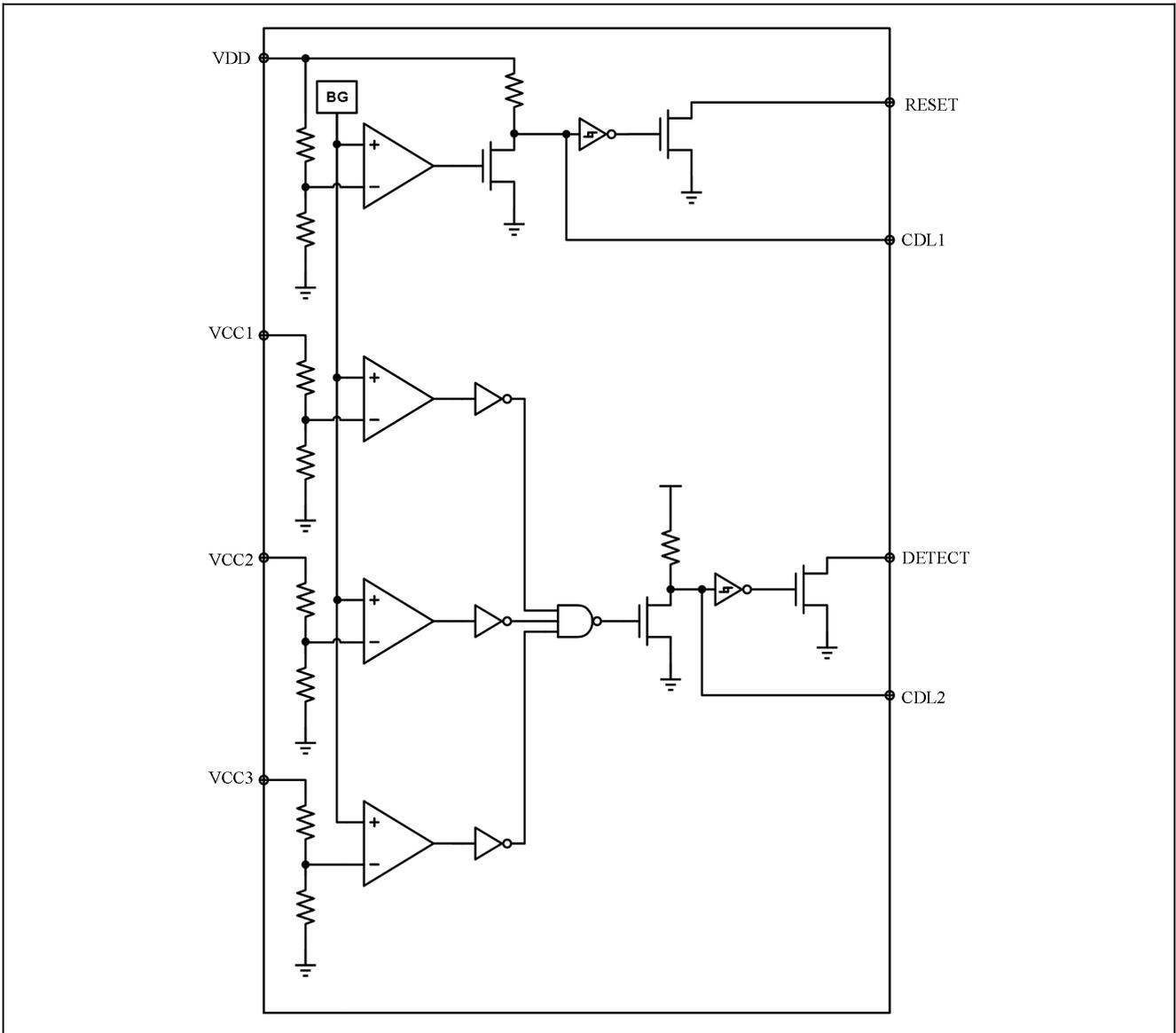


## Pin Function

Pin Number	Symbol	Descriptions
1	VDD	Power Pin
2	VCC1	Power Detect Pin VCC1
3	VCC2	Power Detect Pin VCC2
4	VCC3	Power Detect Pin VCC3
5	CDL2	External capacitor connection to set delay time
6	CDL1	External capacitor connection to set delay time
7	RESET	VDD low voltage output
8	DETECT	VCCx voltage detect output
EP	GND	Ground

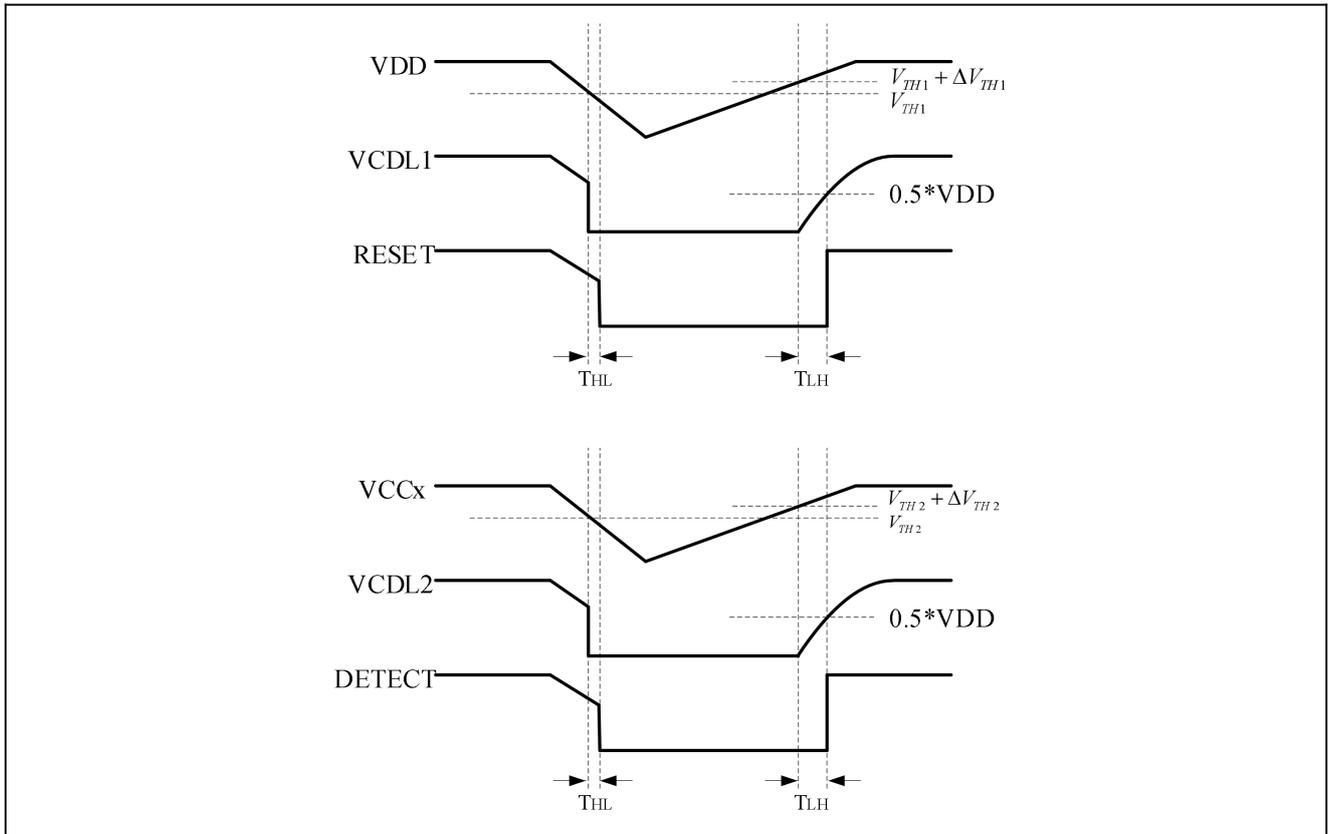
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## Block Diagram



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## Timing Diagram



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## Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are only stress ratings, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	VDD Pin Voltage	-0.3 to 6	V
V <sub>CC</sub>	VCCx Pin Voltage	-0.3 to 6	V
V <sub>RESET</sub>	RESET Pin Voltage	-0.3 to 6	V
V <sub>DETECT</sub>	DETECT Pin Voltage	-0.3 to 6	V
V <sub>CDL1</sub>	CDL1 Pin Voltage	-0.3 to 6	V
V <sub>CDL2</sub>	CDL2 Pin Voltage	-0.3 to 6	V
V <sub>ESD</sub>	ESD susceptibility HBM (Human Body Mode) <sup>(1)</sup>	±2000	V
T <sub>STG</sub>	Storage Temperature Range	-55 to +150	°C
T <sub>A</sub>	Operating Temperature Range	-40 to +125	°C
T <sub>R</sub>	Reflow Temperature	+260	°C

**Note1:** Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

## Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
R <sub>θJA</sub>	ESOP8	Thermal Characteristics, Thermal Resistance, Junction-to-Air	75	°C/W

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## Electrical Characteristics

(Unless Otherwise Specified  $T_A = -40$  to  $125^\circ\text{C}^{(2)}$ )

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{TH1}$	VDD Reset Threshold	$VDD=H \rightarrow L, T_A=25^\circ\text{C}, R_{PU}=470\text{k}\Omega$	2.842	2.9	2.958	V
$V_{TH2}$	VCCx Power Detect Threshold	$VCCx=H \rightarrow L, T_A=25^\circ\text{C}, R_{PU}=470\text{k}\Omega$	3.92	4	4.08	V
$V_{OPL}$	Operating Voltage Range	Power supply VDD, VCCx	1.6	-	6	V
$I_{DD1}$	Supply Current when ON	$VDD=V_{TH1}-0.2\text{V}=2.7\text{V},$ $VCCx=V_{TH2}-0.2\text{V}=3.8\text{V}$	-	3.0	8.0	$\mu\text{A}$
$I_{DD2}$	Supply Current when OFF	$VDD=V_{TH1}+2\text{V}=4.9\text{V},$ $VCCx=V_{TH2}+2\text{V}=6\text{V}$	-	2.5	7.0	$\mu\text{A}$
$\Delta V_{TH1}$	VDD Threshold Voltage Accuracy	$V_{TH1}=2.9\text{V}$	-2	-	2	%
$\Delta V_{TH2}$	VCCx Threshold Voltage Accuracy	$V_{TH2}=4\text{V}$	-2	-	2	%
$V_{RESETL}$	RESET output Voltage Low	$VDD=2.4\text{V}, I_{SINK}=3.6\text{mA}$	-	-	0.2	V
$V_{DETECTL}$	DETECT Output Voltage Low	$VCCx=3.7\text{V}, VDD=2.4\text{V}$ $I_{SINK}=3.6\text{mA}$	-	-	0.2	V
$\Delta V_{HYS1}$	$V_{TH1}$ Hysteresis Voltage Accuracy	$T_A=-40$ to $125^\circ\text{C}, R_{PU}=470\text{k}\Omega$	$0.03^*$ $V_{TH1}$	$0.045^*$ $V_{TH1}$	$0.06^*$ $V_{TH1}$	V
$\Delta V_{HYS2}$	$V_{TH2}$ Hysteresis Voltage Accuracy	$T_A=-40$ to $125^\circ\text{C}, R_{PU}=470\text{k}\Omega$	$0.03^*$ $V_{TH2}$	$0.045^*$ $V_{TH2}$	$0.06^*$ $V_{TH2}$	V
RDL1	RESET Output Delay Resistor	$VDD=V_{TH1} \times 1.1, VCDL1=0.5\text{V},$ $T_A=25^\circ\text{C}$	9	10	12	$\text{M}\Omega$
RDL2	DETECT Output Delay Resistor	$VCCx=V_{TH2} \times 1.1, VCDL2=0.5\text{V},$ $T_A=25^\circ\text{C}$	10	12	15	$\text{M}\Omega$
$V_{CTH1}$	CDL1 pin Threshold Voltage	$VDD=V_{TH1} \times 1.1, T_A=25^\circ\text{C},$ $R_{PU}=470\text{k}\Omega$	$VDD \times 0.42$	$VDD \times 0.50$	$VDD \times 0.65$	V
$V_{CTH2}$	CDL2 pin Threshold Voltage	$VCCx=V_{TH2} \times 1.1, T_A=25^\circ\text{C},$ $R_{PU}=470\text{k}\Omega, VDD=V_{TH1} \times 1.1$	$VDD \times 0.42$	$VDD \times 0.50$	$VDD \times 0.65$	V
$I_{CDL1}$	CDL1 pin Output Discharge Current	$VCDL1=0.1\text{V}, VDD=1\text{V}$	20	250	500	$\mu\text{A}$
$I_{CDL2}$	CDL2 pin Output Discharge Current	$VCDL2=0.1\text{V}, VDD=1\text{V}$	20	250	500	$\mu\text{A}$

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## Electrical Characteristics(Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{LH1}$	RESET propagation delay time	CDL1 pin floating	50	70	200	us
$T_{LH1b}$	RESET delay time2	CDLY=1nF <sup>(3)</sup>	5	9	13	ms
$T_{LH2}$	DETECT propagation delay time	CDL2 pin floating	50	70	200	us
$T_{LH2b}$	DETECT delay time2	CDLY=1nF <sup>(3)</sup>	6	10.8	15.6	ms
$I_{Leak1}$	RESET Leak Current when OFF	$V_{RESET}=6V, T_A=-40$ to $85^{\circ}C$	-	-	0.1	uA
		$V_{RESET}=6V, T_A=85$ to $125^{\circ}C$	-	-	1	uA
$I_{Leak2}$	DETECT Leak Current when OFF	$V_{DETECT}=6V, T_A=-40$ to $85^{\circ}C$	-	-	0.1	uA
		$V_{DETECT}=6V, T_A=85$ to $125^{\circ}C$	-	-	1	uA

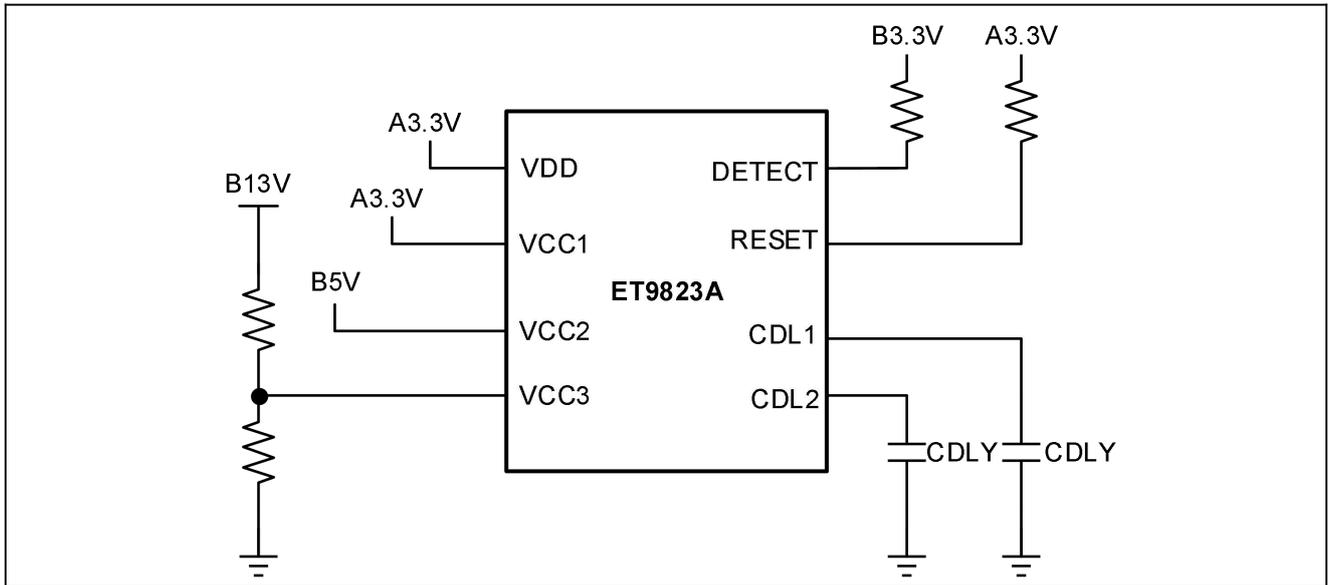
**Note2:**Production testing done at  $T_A=25^{\circ}C$ , limits over temperature guaranteed by design.

**Note3:**CDLY is CDL pin external capacitor ,capacitor tolerance  $\pm 10\%$ .

**R<sub>PU</sub>:** Pull-up resistor

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## Application Circuit



When power pin VDD reaches threshold voltage ( $V_{TH1}$ ) from high to low, RESET pin changes from high to low. When any power pin VCC1, VCC2 and VCC3 ramp down over the threshold voltage ( $V_{TH2}$ ), DETECT pin changes from high to low. This circuit can set delay time controlled by the external capacitor at the rise of power pin.

$$T_{LH} = CDLY \times RCT \times \ln\left(\frac{VDD}{VDD - VCTH}\right)$$

$T_{LH}$ : time until the voltage of CDL pin rises to  $0.5 \times VDD$  after VDD rises up and beyond the release voltage..

RCT: CDL pin internal impedance.

Note: There's some difference between real tested delay time and principle equation.

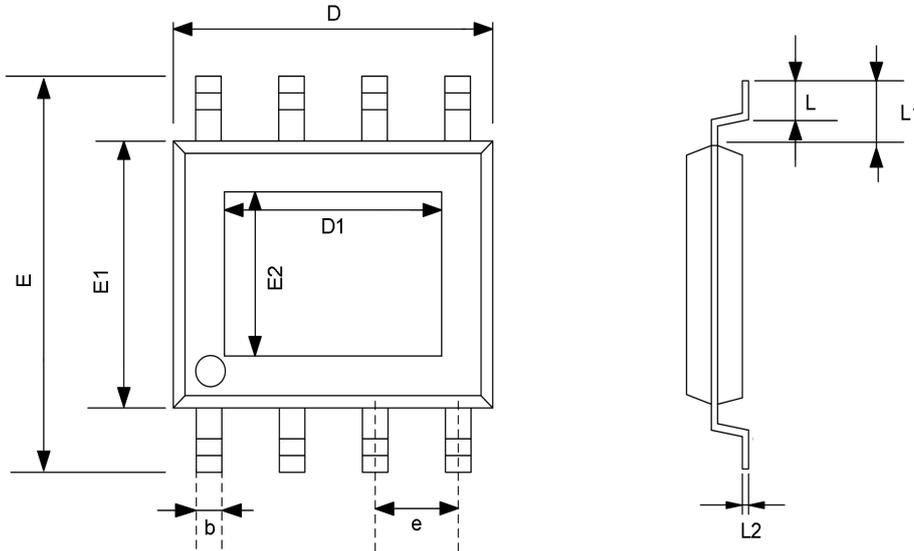
Open drain type need pull-up resistor connected to VDD or other power supply.

Because the resistor connected inside VCC3 pin is about  $20M\Omega$ , suggest that the low side resistor of external resistor divider is smaller than  $20k\Omega$  for accuracy.

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## Package Dimension

ESOP8



COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	-	-	1.75
A1	0.00	-	0.15
A2	1.30	1.40	1.50
b	0.31	-	0.50
c	0.20	-	0.24
D	4.80	-	5.00
E	5.80	6.00	6.20
D1	3.30 REF		
E1	3.80	-	4.00
E2	2.41 REF		
e	1.27 BSC		
L	0.40	-	0.80
L1	1.05 REF		
L2	0.25 REF		



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## Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2025-5-19	Preliminary Version	Huyt	Tangyx	Liujiy
1.0	2025-11-11	Original Version	Huyt	Chenh	Liujiy
1.1	2025-12-8	Update $I_{Leak}$ Test Conditions	Huyt	Chenh	Liujiy