I²C Controlled Single Cell 5 A Fast Charger for High Input Voltage and Adjustable Voltage USB On-the-Go Boost Mode

General Description

The ET95603 is a highly-integrated 5 A switch mode battery charge management and system power path management device for single cell Li-Ion and Li polymer battery. The devices support high input voltage fast charging. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase.

Features

- High-Efficiency 5 A, 1.5 MHz, Switch Mode Buck Charger
  - 93% Charge Efficiency at 2 A and 91% Charge Efficiency at 3 A Charge Current
  - Optimize for High Voltage Input (9 V / 12 V)
  - Low Power PFM Mode for Light Load Operations
- USB On-The-Go (OTG) with Adjustable Output from 4.5 V to 5.5 V
  - Selectable 500 kHz / 1.5 MHz Boost Converter with up-to 2.4 A Output
  - 93% Boost Efficiency at 5 V at 1 A Output
  - Accurate Current Limit Mode Overcurrent Protection
  - Support down-to 2.5 V Battery
  - Support PWM only or PFM/PWM control for Light Load Efficiency
- Single Input to Support USB Input and Adjustable High Voltage Adapters
  - Support 3.9 V to 14.5 V Input Voltage Range
  - Input Current Limit (100 mA to 3.1 A with 50 mA resolution) to Support USB2.0, USB3.0 standard and High Voltage Adapters
  - Maximum Power Tracking by Input Voltage Limit up to 14.5 V for Wide Range of Adapters
  - Auto Detect USB SDP, CDP, DCP, and Non standard Adapters
- Resistance Compensation (IRCOMP) from Charger Output to Cell Terminal
- Highest Battery Discharge Efficiency with 16-mΩ Battery Discharge MOSFET up to 13 A
- Integrated ADC for System Monitor (Voltage, Temperature, Charge Current)
- Narrow VDC (NVDC) Power Path Management
  - Instant-On Works with No Battery or Deeply Discharged Battery

  - Ideal Diode Operation in Battery Supplement Mode
- BATFET Control to Support Ship Mode, Wake Up and Full System Reset
- Flexible Autonomous and I^2C Mode for Optimal System Performance
- High Integration Includes all MOSFETs, Current Sensing and Loop Compensation
- 8 μA Low Battery Leakage Current to Support Ship Mode
- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±5% Charge Current Regulation
  - ±7.5% Input Current Regulation
- Safety
  - Battery Temperature Sensing for Charge and Boost Mode
  - Thermal Regulation and Thermal Shutdown

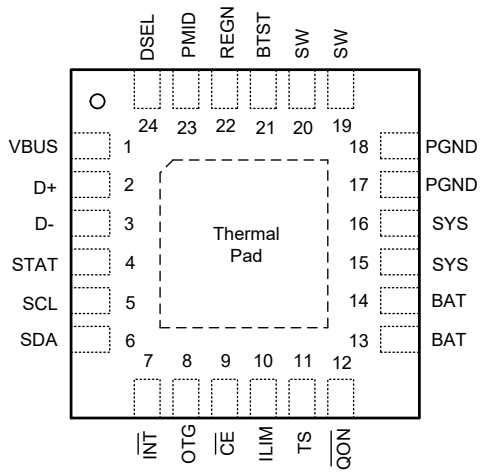
Applications

- Smart Phones
- Tablet PC
- Portable Internet Devices

Device Information

PART NUMBER	PACKAGE	BODY SIZE(NOM)
ET95603	WQFN24	4.00mm x 4.00mm

Pin Configuration



Top View

Pin Functions

Pin		TYPE[1]	DESCRIPTION
NAME	NO.		
VBUS	1	P	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1 μF ceramic capacitor from VBUS to PGND and place it as close as possible to IC.
D+	2	AIO	Positive line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter. The pin can be configured as output driver by DP_DAC register bits when input source is plugged-in or during OTG mode.
D-	3	AIO	Negative line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter. The pin can be configured as output driver by DM_DAC register bits when input source is plugged-in or during OTG mode.
STAT	4	DO	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10 kΩ resistor. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin blinks in 1 Hz. The STAT pin function can be disabled when STAT_DIS bit is set.
SCL	5	DI	I^2C Interface clock. Connect SCL to the logic rail through a 10 kΩ resistor.
SDA	6	DIO	I^2C Interface data. Connect SDA to the logic rail through a 10 kΩ resistor.
INT	7	DO	Open-drain Interrupt Output. Connect the INT to a logic rail via 10 kΩ resistor. The INT pin sends active low, 256 μs pulse to host to report charger device status and fault.
OTG	8	DI	Active high enable pin during boost mode. The boost mode is activated when OTG_CONFIG =1 and OTG pin is high.
CE	9	DI	Active low Charge Enable pin. Battery charging is enabled when CHG_CONFIG = 1 and CE pin = Low. CE pin must be pulled High or Low.

Pin Functions (Continued)

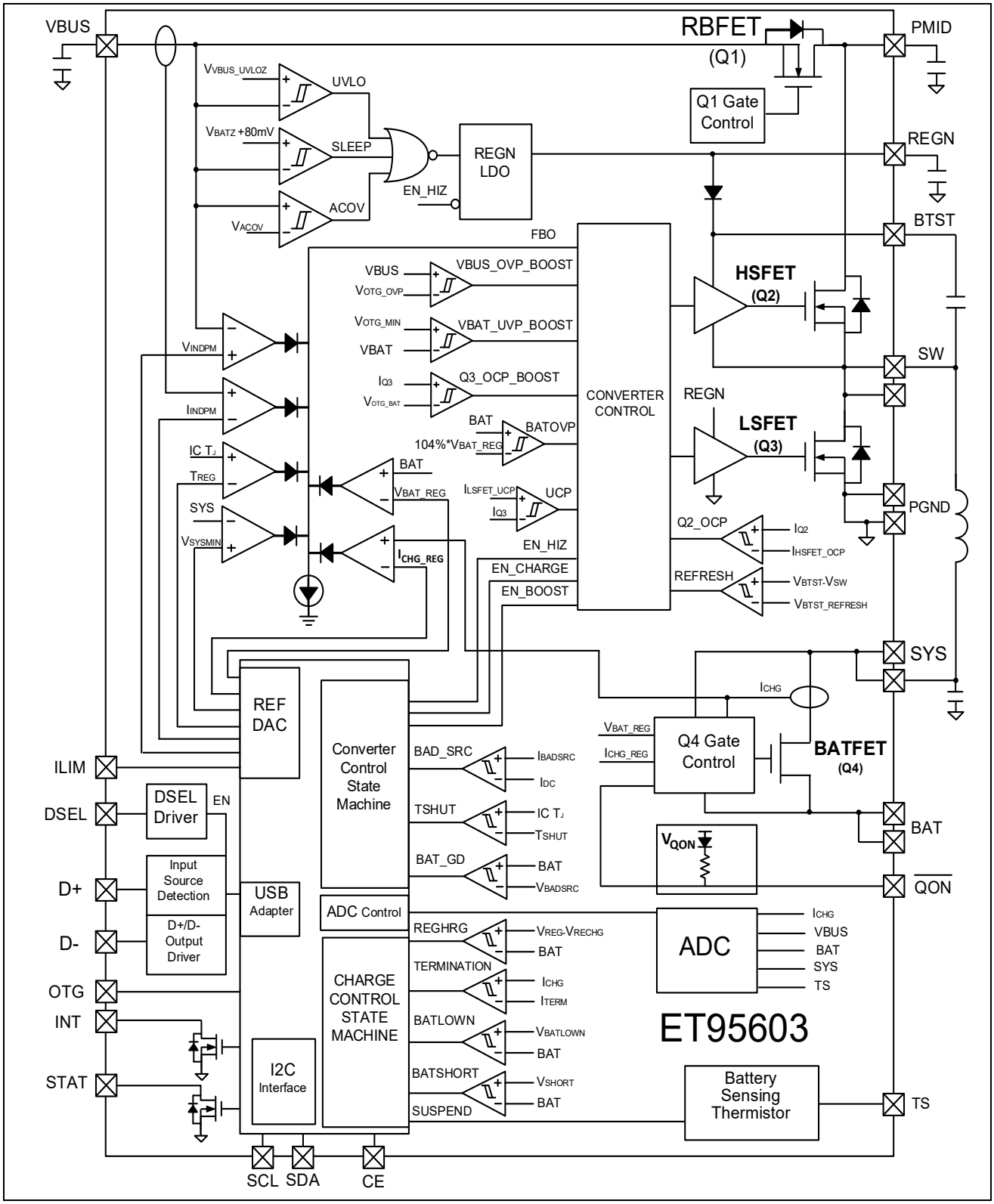
Pin		TYPE[1]	DESCRIPTION
NAME	NO.		
ILIM	10	AI	Input current limit Input. ILIM pin sets the maximum input current and can be used to monitor input current ILIM pin sets the maximum input current limit by regulating the ILIM voltage at 0.8 V. A resistor is connected from ILIM pin to ground to set the maximum limit as $I_{INMAX} = K_{ILIM}/R_{ILIM}$. The actual input current limit is the lower limit set by ILIM pin (when EN_ILIM bit is high) or IIINLIM register bits. Input current limit of less than 500 mA is not support on ILIM pin. ILIM pin can also be used to monitor input current when the voltage is below 0.8V. The input current is proportional to the voltage on ILIM pin and can be calculated by $I_{IN} = (K_{ILIM} \times V_{ILIM}) / (R_{ILIM} \times 0.8)$. The ILIM pin function can be disabled when EN_ILIM bit is 0.
TS	11	AI	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor.
QON	12	DI	BATFET enable/reset control input. When BATFET is in ship mode, a logic low of $t_{SHIPMODE}$ (typical 1sec) duration turns on BATFET to exit shipping mode. When VBUS is not plugged-in, a logic low of t_{QON_RST} (typical 15sec) duration resets SYS (system power) by turning BATFET off for t_{BATFET_RST} (typical 0.3sec) and then re-enable BATFET to provide full system power reset. The pin contains an internal pull-up to maintain default high logic.
BAT	13,14	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10 μF closely to the BAT pin.
SYS	15,16	P	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage. Connect a 20 μF closely to the SYS pin.
PGND	17,18	P	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.

Pin Functions (Continued)

Pin		TYPE[1]	DESCRIPTION
NAME	NO.		
SW	19,20	P	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047 μF bootstrap capacitor from SW to BTST.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the anode of the boost-strap diode. Connect the 0.047 μF bootstrap capacitor from SW to BTST.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost-strap diode. Connect a 4.7 μF (10 V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS pin.
PMID	23	P	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Given the total input capacitance, put 1 μF on VBUS to PGND, and the rest capacitance on PMID to PGND.
DSEL	24	DO	Active high D+/D- multiplexer selection control. Connect a 47 nF (6V rating) ceramic capacitor from DSEL to analog GND. The pin is normally low. During input source type detection, the pin drives high to indicate the device D+/D- detection is in progress and needs to take control of D+, D- signals. When detection is completed, the pin keeps high when DCP or HVDCP is detected. The pin returns to low when other input source type is detected.The pin returns to low when other input source type(SDP or CDP) is detected.
Thermal Pad		P	Exposed pad beneath the IC for heat dissipation. Always solder Thermal Pad to the board, and have vias on the Thermal PAD plane star-connecting to PGND and ground plane for high-current power converter.

Note1: AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power

Block Diagram



Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(2)]

Symbol	Parameter	Min	Max	Unit
Voltage Range (with respect to GND)	VBUS (converter not switching)	-2	22	V
	PMID (converter not switching)	-0.3	22	V
	STAT	-0.3	20	V
	DSEL	-0.3	7	V
	BTST	-0.3	20	V
	SW	-2	16	V
	SW (peak for 10 ns duration)	-3	16	V
	BAT, SYS(converter not switching)	-0.3	6	V
	SDA, SCL, INT, OTG, REGN, TS, CE, QON	-0.3	7	V
	D+, D-	-0.3	7	V
	BTST to SW	-0.3	7	V
	PGND to GND	-0.3	0.3	V
	ILIM	-0.3	5	V
Output Sink Current	INT, STAT		6	mA
	DSEL		2	mA
Junction temperature	Junction temperature	-40	150	°C
Storage temperature range, Tstg	Storage temperature Range	-65	150	°C

Note2: Stresses beyond those listed under Absolute maximum Ratings may cause permanent damage to the device. These are stress ratings only,which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

ESD Ratings

Symbol	Parameter	Conditions	Value	Unit
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[3]	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[4]	± 250	

Note3: JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

Note4: JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input voltage	3.9		14.5[5]	V
I_{IN}	Input current (VBUS)			3.1	A
I_{SYS}	Output current (SW)			5	A
V_{BAT}	Battery voltage			4.608	V
I_{BAT}	Fast charging current			5	A
	Discharging current with internal MOSFET	Up to 10 (continuous)			A
		13(peak) (Up to 1sec duration)			A
T_A	Operating ambient temperature	-40		85	°C

Note5: The inherent switching noise voltage spikes should not exceed the absolute maximum voltage rating on either the BTST or SW pins. A tight layout minimizes switching noise.

Thermal information

Symbol	Thermal Metric[6]	ET95603 RTW (QFN) 24 Pins	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	31.8	°C/W
$R_{\theta JC(top)}$	Junction to case (top) thermal resistance	27.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

Note6: For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Electrical Characteristics

V_{VAC_UVLOZ} < V_{VAC} < V_{VAC_OV} and V_{VAC} > V_{BAT} + V_{SLEEP}, T_J = -40 °C to 125 °C and T_J = 25 °C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS) in buck mode	V_{BAT} = 4.2 V, V_{BUS} < $V_{AC-UVLOZ}$, leakage between BAT and VBUS, T_J < 85 °C			5	μA
I_{BAT}	Battery discharge current (BAT) in buck mode	HIZ Mode, No VBUS, BATFET Disabled(REG09[5]=1), battery monitor disabled, T_J =25°C		8	16	μA
I_{BAT}	Battery discharge current (BAT, SW, SYS)	High-Z mode, no VBUS, BATFET enabled (REG09[5]=0), battery monitor disabled, T_J =25°C		35	70	μA
I_{VBUS_HIZ}	Input supply current (VBUS) in buck mode	V_{VBUS} = 5 V, High-Z Mode, V_{BAT}>3.5V, battery monitor disabled		37	74	μA
I_{VBUS_HIZ}	Input supply current (VBUS) in buck mode	V_{VBUS} = 12 V, High-Z Mode , V_{BAT}>3.5V, battery monitor disabled		43	86	μA
I_{VBUS}	Input supply current (VBUS) in buck mode	V_{BUS} > $V_{(UVLO)}$, V_{BUS} > V_{BAT}, converter not switching		1.5	3	mA
I_{VBUS}	Input supply current (VBUS) in buck mode	V_{VBUS} > V_{UVLO}, V_{VBUS} > V_{VBAT}, converter switching, V_{BAT} = 3.2 V, I_{SYS} = 0 A		3		mA
I_{VBUS}	Input supply current (VBUS) in buck mode	V_{VBUS} > V_{UVLO}, V_{VBUS} > V_{VBAT}, converter switching, V_{BAT} = 3.2 V, I_{SYS} = 0 A		3		mA
I_{BOOST}	Battery Discharge Current in boost mode	V_{BAT} = 4.2 V, boost mode, I_{VBUS} =0 A, converter switching		2		mA
VBUS, VAC AND BAT PIN POWER-UP						
V_{VBUS_OP}	VBUS operating range		3.9		14.5	V
V_{VBUS_UVLOZ}	VBUS for active I^2C, no battery		3.5			V
V_{SLEEP}	Sleep mode falling threshold		10	100	200	mV
V_{SLEEPZ}	Sleep mode rising threshold		100	250	400	mV

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ACOV}	VBUS over-voltage rising threshold			14.5		V
	VBUS over-voltage falling hysteresis			300		mV
V_{BAT_UVLOZ}	BAT for active I²C, no VBUS			2.6		V
V_{BAT_DPL}	Battery Depletion Falling Threshold		2.2	2.4	2.6	V
V_{BAT_DPLZ}	Battery Depletion Rising Threshold		2.4	2.6	2.8	V
V_{BUSMIN}	Bad adapter detection threshold			3.8		V
I_{BADSRC}	Bad adapter detection current source			30		mA
POWER-PATH						
V_{SYS}	Typical system regulation voltage	$I_{(SYS)}$ = 0 A, V_{BAT}> V_{SYS_MIN}, BATFET Disabled (REG09[5]=1)		V_{BAT} + 75mV		V
		$I_{(SYS)}$ = 0 A, V_{BAT} < V_{SYS_MIN}, BATFET Disabled (REG09[5]=1)		V_{SYS_MIN} + 150mV		V
V_{SYS_MIN}	Minimum DC system voltage output	V_{BAT}< V_{SYS_MIN}, SYS_MIN= 3.5 V (REG03[3:1]=101), I_{SYS}= 0 A	3.50	3.65		V
V_{SYS_MAX}	Maximum DC system voltage output	V_{BAT} = 4.4 V, SYS_MIN = 3.5V (REG03[3:1]=101), I_{SYS}= 0 A		4.475		V
$R_{ON(RBFET)}$	Top reverse blocking MOSFET(RBFET) on-resistance between VBUS and PMID	T_J=25°C		35		mΩ
$R_{ON(HSFET)}$	Top switching MOSFET(HSFET) on-resistance between PMID and SW	T_J=25°C		30		mΩ
$R_{ON(LSFET)}$	Bottom switching MOSFET(LSFET) on-resistance between SW and GND	T_J=25°C		30		mΩ
V_{FWD}	BATFET forward voltage in Supplement mode	BAT discharge current 10 mA		40		mV

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT_GD}	Battery good comparator rising threshold	V_{BAT} rising		3.5		V
$V_{BAT\_GD\_HYST}$	Battery good comparator falling threshold	V_{BAT} falling		100		mV
BATTERY CHARGER						
V_{BATREG_RANGE}	Typical Charge voltage program range		3.840		4.608	V
V_{BATREG_STEP}	Typical Charge voltage step			8		mV
V_{BATREG}	Charge voltage resolution accuracy	(REG06[7:2]=010111) V_{BAT} = 4.208 V, T_J = 25°C	-0.5		0.5	%
$I_{CHG\_REG\_RANGE}$	Typical fast charge current regulation range		0		5056	mA
$I_{CHG\_REG\_STEP}$	Typical fast charge current regulation step			64		mA
$I_{CHG\_REG\_ACC}$	Fast charge current regulation accuracy	V_{BUS}=5V, V_{BAT} = 3.8 V, I_{CHG} = 128mA, T_J = 25°C	90		166	mA
		V_{BUS}=5V, V_{BAT} = 3.8 V, I_{CHG} = 256mA, T_J = 25°C	205		307	mA
		V_{BUS}=5V, V_{BAT} = 3.8 V, I_{CHG} = 2048mA, T_J = 25°C	-5		5	%
$V_{BATLOWV}$	Battery LOWV falling threshold	Fast charge to precharge, BATLOWV (REG06[1]) = 1	2.75		3.05	V
	Battery LOWV rising threshold	Precharge to fast charge, BATLOWV (REG06[1])=1 (Typical 200-mV hysteresis)	3		3.3	V
I_{PRECHG_RANGE}	Precharge current range		64		1024	mA
I_{PRECHG}	Precharge current	V_{BAT}=2.6V, I_{PRECHG}=256mA	231		281	mA
I_{TERM_RANGE}	Termination current range		64		1024	mA
I_{TERM}	Termination current	I_{TERM} = 128 mA, I_{CHG}<= 1344 mA, V_{REG}=4.208V, T_J = 25°C		128		mA
		I_{TERM} = 128 mA, I_{CHG}> 1344 mA, V_{REG}=4.208V, T_J = 25°C	90		166	mA
		I_{TERM} = 256 mA, I_{CHG}<= 1344 mA, V_{REG}=4.208V, T_J = 25°C		256		mA
		I_{TERM} = 256 mA, I_{CHG}> 1344 mA, V_{REG}=4.208V, T_J = 25°C	192		320	mA

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SHORT}	Battery short voltage	V_{VBAT} falling	1.9		2.2	V
V_{SHORT_HYST}	Battery short voltage hysteresis	V_{VBAT} rising		200		mV
I_{SHORT}	Battery short current	V_{VBAT} < 2.2V		100		mA
V_{RECHG}	Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, REG04[0] = 0		100		mV
V_{RECHG}	Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, REG04[0] = 1		200		mV
$I_{SYSLOAD}$	System discharge load current	V_{SYS} = 4.2 V		30		mA
$R_{ON(BATFET)}$	SYS-BAT MOSFET (BATFET) on-resistance	T_J = 25°C		16		mΩ
INPUT VOLTAGE AND CURRENT REGULATION						
V_{INDPM_RANGE}	Typical Input voltage regulation range		4		15.3	V
V_{INDPM_STEP}	Typical Input voltage regulation step			100		mV
V_{INDPM_ACC}	Input voltage regulation accuracy	VINDPM = 4.4 V, 25°C	4.268		4.532	V
I_{INDPM_RANGE}	Typical Input current regulation range		100		3100	mA
I_{INDPM_STEP}	Typical Input current regulation step			50		mA
I_{INDPM_100}	Input current 100 mA regulation V_{BUS} = 5 V, current pulled from SW	IINLIM (REG00[5:0]) =100 mA	80		100	mA
I_{INDPM}	Input current regulation V_{BUS} = 5 V, current pulled from SW	USB500, IINLIM (REG00[5:0]) = 500 mA	400		500	mA
		USB900, IINLIM (REG00[5:0]) = 900 mA	750	825	900	mA
		Adapter 1.5 A, IINLIM (REG00[5:0]) = 1500mA	1350	1400	1500	mA
I_{IN_START}	Input current limit during system start-up	V_{SYS} = 2.2 V, IINLIM (REG00[5:0]) > = 200 mA		200		mA
K_{ILIM}	IINMAX = KILIM/RILIM	Input current regulation by ILIM pin = 1.5 A		390		AxΩ

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
D+/D- DETECTION						
$V_{(0P6\_VSRC)}$	D+/D– voltage source (0.6 V)	I(DP) < 1 mA; DP_DAC=010 or I(DM) < 1 mA; DM_DAC=010	0.5	0.6	0.7	V
$V_{(3P3\_VSRC)}$	D+/D– voltage source (3.3 V)	I(DP) < 1 mA; DP_DAC=110 or I(DM) < 1 mA; DM_DAC=110	2.7	3.3	3.45	V
$I_{(100UA\_ISINK)}$	D+/D– current sink		25	100	150	μA
$V_{(2P7\_VTH)}$	D+/D– comparator threshold for non-standard adapter detection (divider 1, 3, or 4)		2.42			V
$V_{(2P3\_VTH)}$	D+/D– comparator threshold for non-standard adapter detection (divider 1, 3)		2.18		2.42	V
$V_{(1P6\_VTH)}$	D+/D– comparator threshold for non-standard adapter detection (divider 2)		1.48		1.72	V
$V_{(0P35\_VTH)}$	D+/D– comparator threshold		0.25		0.4	V
$R_{(D-\_DWN)}$	D– pulldown for connection check			16		kΩ
BAT OVER-VOLTAGE/CURRENT PROTECTION						
V_{BATOVP}	Battery overvoltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		104		%
V_{BATOVP_HYST}	Battery overvoltage hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}		2		%
$I_{BAT(FET\_OCP)}$	System over-current threshold			13		A
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	REG08[1:0] = 11		120		°C
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature rising		160		°C
T_{SHUT_HYST}	Thermal Shutdown Hysteresis	Temperature falling		30		°C
JEITA Thermistor Comparator (BUCK MODE)						
V_{T1}	T1 (0 °C) threshold, Charge suspended T1 below this temperature.	As Percentage to V_{REGN}	72.5	73.5	74.5	%
V_{T1_HYS}	Charge back to ICHG/2 (REG04[6:0]) and VREG (REG06[7:2]) above this temperature.	As Percentage to V_{REGN}	71	72	73	%

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{T2}	T2 (10 °C) threshold, Charge back to I_{CHG}/2 and 4.2 V below this temperature	As percentage of V_{REGN}	67.5	68.5	69.5	%
V_{T2_HYS}	Charge back to ICHG (REG04[6:0]) and VREG (REG06[7:2]) above this temperature.	As Percentage to V_{REGN}	66	67	68	%
V_{T3}	T3 (45 °C) threshold, charge back to I_{CHG} and 4.05 V above this temperature.	As Percentage to V_{REGN}	43.5	44.5	45.5	%
V_{T3_HYS}	Charge back to ICHG (REG04[6:0]) and VREG (REG06[7:2]) below this temperature.	As Percentage to V_{REGN}	44.5	45.5	46.5	%
V_{T5}	T5 (60 °C) threshold, charge suspended above this temperature.	As Percentage to V_{REGN}	33.5	34.5	35.5	%
V_{T5_HYS}	Charge back to ICHG (REG04[6:0]) and VREG-200 mV (REG06[7:2]) below this temperature	As Percentage to V_{REGN}	35	36	37	%
COLD OR HOT THERMISTER COMPARATOR (BOOST MODE)						
V_{BCOLD}	Cold temperature threshold 1, TS pin voltage rising threshold	As percentage to V_{REGN} REG01[5] = 1 (Approximately –20°C w/ 103AT)	79	80	81	%
V_{BCOLD_HYS}	Cold temperature threshold 1, TS pin voltage falling threshold	As percentage to V_{REGN} REG01[5] = 1	78	79	80	%
V_{BHOT}	Hot temperature threshold 2, TS pin voltage falling threshold	As percentage to V_{REGN} REG01[7:6] = 10 (Approx. 65°C w/ 103AT)	30.5	31.5	32.5	%
V_{BHOT_HYS}	Hot temperature threshold 2, TS pin voltage rising threshold	As percentage to V_{REGN} REG01[7:6] =10	33.5	34.5	35.5	%

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PWM						
F_{SW}	PWM switching frequency, and digital clock	Oscillator frequency		1.5		MHz
D_{MAX}	Maximum PWM duty cycle			99		%
BOOST MODE OPERATION						
$V_{OTG\_REG\_RANGE}$	Typical boost mode regulation voltage range		4.55		5.55	V
$V_{OTG\_REG\_STEP}$	Typical boost mode regulation voltage step			64		mV
$V_{OTG\_REG\_ACC}$	Boost mode regulation voltage accuracy	I(VBUS) = 0 A, BOOSTV=4.998V (REG0A[7:4] = 0111)		±4		%
V_{OTG_BAT}	Minimum battery voltage to exit boost mode	BAT falling, MIN_VBAT_SEL= 0		2.85		V
		BAT falling, MIN_VBAT_SEL= 1		2.5		V
$V_{OTG\_BAT\_EN}$	Minimum battery voltage to enter boost mode	BAT rising, MIN_VBAT_SEL=0		3.15		V
		BAT rising, MIN_VBAT_SEL=1		2.8		V
I_{OTG}	Typical boost mode output current range		0.5		2.45	A
$I_{OTG\_OCP\_ACC}$	Boost mode RBFET over-current protection accuracy	BOOST_LIM = 1.2 A (REG0A[2:0] = 010)	1.2		1.7	A
V_{OTG_OVP}	Boost mode overvoltage threshold	Rising threshold		6.0		V
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 9 V, I_{REGN} = 40 mA		5		V
		V_{VBUS} = 5 V, I_{REGN} = 20 mA		4.7		V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 9 V, V_{REGN} = 3.8 V		50		mA
ANALOG-TO-DIGITAL CONVERTER (ADC)						
RES	Resolution	Rising threshold		7		bits
V_{BAT_RANGE}	Typical battery voltage range	V_{VBUS} > V_{BAT} + V_{SLEEP} or OTG mode is enabled	2.304		4.848	V
		V_{VBUS} < V_{BAT} + V_{SLEEP} and OTG mode is disabled	V_{SYS_MIN}		4.848	V

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT_RES}	Typical battery voltage resolution			20		mV
V_{SYS_RANGE}	Typical system voltage range	$V_{VBUS} > V_{BAT} + V_{SLEEP}$ or OTG mode is enabled	2.304		4.848	V
		$V_{VBUS} < V_{BAT} + V_{SLEEP}$ and OTG mode is disabled	V_{SYS_MIN}		4.848	V
V_{SYS_RES}	Typical system voltage resolution			20		mV
V_{VBUS_RANGE}	Typical V_{VBUS} voltage range	$V_{VBUS} > V_{BAT} + V_{SLEEP}$ or OTG mode is enabled	4		15.3	V
V_{VBUS_RES}	Typical V_{VBUS} voltage resolution			100		mV
I_{BAT_RANGE}	Typical battery charge current range	$V_{VBUS} > V_{BAT} + V_{SLEEP}$ and $V_{BAT} > V_{BAT\_SHORT}$	0		6.4	A
I_{BAT_RES}	Typical battery charge current resolution			50		mA
V_{TS_RANGE}	Typical TS voltage range		21		80	%
V_{TS_RES}	Typical TS voltage resolution			0.47		%
LOGIC I/O PIN (OTG, CE, QON)						
V_{IH}	Input high threshold level		1.3			V
V_{IL}	Input low threshold level				0.4	V
I_{IN_BIAS}	High Level Leakage Current	Pull-up rail 1.8 V			1	μA
V_{QON}	Internal /QON pull-up	Battery only mode		V_{BAT}-0.7		V
		Adapter insert mode		4.3		V
R_{QON}	Internal /QON pull-up resistance			200		kΩ
LOGIC I/O PIN (DSEL)						
V_{OL}	Output low threshold level	I_{OL} = 2 mA, C_{DSEL}= 47 nF			0.4	V
V_{OH}	Output high threshold level	I_{OH} = 5 mA, C_{DSEL}= 47 nF, non-switching, $I_{(REGN)}$ = 30 mA	4.5			V
LOGIC I/O PIN (INT, STAT)						
V_{OL}	Output low threshold level	Sink current = 5 mA, sink current			0.4	V
I_{OUT_BIAS}	High level leakage current	Pull-up rail 1.8 V			1	V

Electrical Characteristics (Continued)

I²C Interface (SCL, SDA)						
V_{IH}	Input high threshold level, SCL and SDA	Pull up rail 1.8 V	1.3			V
V_{IL}	Input t low threshold level	Pull up rail 1.8 V			0.4	V
V_{OL}	Output low threshold level	Sink current 5 mA			0.4	V
I_{BAIS}	High level leakage current	Pull up rail 1.8 V			1	μA

Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBUS/BAT POWER UP						
t_{BADSRC}	Bad adapter detection duration			30		ms
BAT OVER-VOLTAGE PROTECTION						
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			1		μs
BATTERY MONITOR						
t_{CONV}	Conversion time	CONV_RATE(REG02[6]) = 0		8		ms
QON AND SHIPMODE TIMING						
$t_{SHIPMODE}$	QON low time to turn on BATFET and exit ship mode	T_J = 25°C, DSB_QON(REG16[7])=0	1	1.7	2.7	s
		T_J = 25°C, DSB_QON(REG16[7])=1	2.72	3.4	4.08	s
t_{QON_RST}	QON low time to reset BATFET	T_J = 25°C	9.6	12	14.4	s
t_{BATFET_RST}	BATFET off time during full system reset	T_J = 25°C	384	480	576	ms
t_{SM_DLY}	Enter ship mode delay	T_J = 25°C, BATFET_DLY(REG09[3])=0	26.4	33	39.6	ms
		T_J = 25°C, BATFET_DLY(REG09[3])=1	8.4	10.5	12.6	s
I²C INTERFACE						
f_{SCL}	SCL clock frequency				400	kHz
DIGITAL CLOCK AND WATCHDOG TIMER						
t_{WDT}	REG05[4]=1	REGN LDO disabled	32	40		s

Detailed Description

The I²C Serial interface with charging and system settings makes the device a truly flexible solution.

The ET95603 is a highly-integrated 5 A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. It features fast charging with high input voltage support for a wide range of smartphone, tablet and portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. It also integrates Input Current Optimizer (ICO) and Resistance Compensation (IRCOMP) to deliver maximum charging power to battery. The solution is highly integrated with input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. It also integrates the bootstrap diode for the high-side gate drive and battery monitor for simplified system design. The I²C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port, and USB compliant adjustable high voltage adapter. To set the default input current limit, device uses the built-in USB interface, such as USB PHY device. The device is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. The device also meets USB On-the-Go (OTG) operation power rating specification by supplying 5 V (Adjustable 4.5 V - 5.5 V) on VBUS with current limit up to 2.4 A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This Supplemental Mode operation prevents overloading the input source.

The device initiates and completes a charging cycle without software control. It automatically detects the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle.

The charger provides various safety features for battery charging and system operations, including battery temperature negative thermistor monitoring, charging safety timer and overvoltage/overcurrent protections. The thermal regulation reduces charge current when the junction temperature exceeds 120°C (programmable). The STAT output reports the charging status and any fault conditions. The INT immediately notifies host when fault occurs.

The device also provides a 7-bit analog-to-digital converter (ADC) for monitoring charge current and input/battery/system (VBUS, BAT, SYS, TS) voltages.

Feature Description

Device Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage of VBUS and BAT. When VBUS rises above V_{VBUS_UVLOZ} or BAT rises above V_{BAT_UVLOZ} , the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold ($V_{BAT\_DPL\_RISE}$) , the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low R_{DSON} of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The device always monitors the discharge current through BATFET (Supplement Mode). When the system is overloaded or shorted ($I_{BAT} > I_{BATFET\_OCP}$), the device turns off BATFET immediately and set BATFET_DIS bit to indicate BATFET is disabled until the input source plugs in again or one of the methods described in BATFET Enable (Exit Shipping Mode) is applied to re-enable BATFET.

Device Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. Power Up REGN LDO
2. Poor Source Qualification
3. Input Source Type Detection is based on D+/ D- to set default input current limit (IINLIM) register or input source type.
4. Input Voltage Limit Threshold Setting (VINDPM threshold)
5. Converter Power-up

Power Up REGN Regulation(LDO)

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

- VBUS above V_{VBUS_UVLOZ}
- VBUS above V_{BAT} + V_{SLEEPZ} in buck mode or VBUS below V_{BAT} + V_{SLEEP} in boost mode
- After 220 ms delay is completed

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than I_{VBUS_HIZ} from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

Poor Source Qualification

After REGN LDO powers up, the device confirms the current capability of the input source. The input source must meet both of the following requirements in order to start the buck converter.

- VBUS voltage below V_{ACOV}
- VBUS voltage above $V_{VBUSMIN}$ when pulling I_{BADSRC} (typical 30 mA)

Once the input source passes all the conditions above, the status register bit VBUS_GD is set high and the INT pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

Input Source Type Detection

After the VBUS_GD bit is set and REGN LDO is powered, the charger device runs Input Source Type Detection when AUTO_DPDM_EN bit is set.

The ET95603 follows the USB Battery Charging Specification 1.2 (BC1.2) and to detect input source (SDP/CDP/DCP) and non-standard adapter through USB D+/D- lines. In addition, when USB DCP is detected, it initiates adjustable high voltage adapter handshake on D+/D-.

After input source type detection is completed, an INT pulse is asserted to the host. in addition, the following registers and pin are changed:

1. Input Current Limit (IINLIM) register is changed to set current limit
2. PG_STAT bit is set

The host can over-write IINLIM register to change the input current limit if needed. The charger input current is always limited by the lower of IINLIM register or ILIM pin at all-time.

When AUTO_DPDM_EN is disabled, the Input Source Type Detection is bypassed. The Input Current Limit(IINLIM) register, VBUS_STAT, and SPD_STAT bits are unchanged from previous values.

D+/D- Detection Sets Input Current Limit

The ET95603 contains a D+/D– based input source detection to set the input current limit automatically. The D+/D- detection includes standard USB BC1.2, non-standard adapter, and adjustable high voltage adapter detections. When input source is plugged-in, the device starts standard USB BC1.2 detections. The USB BC1.2 is capable to identify Standard Downstream Port (SDP), Charging Downstream Port (CDP), and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer of 500ms is expired, the non-standard adapter detection is applied to set the input current limit.

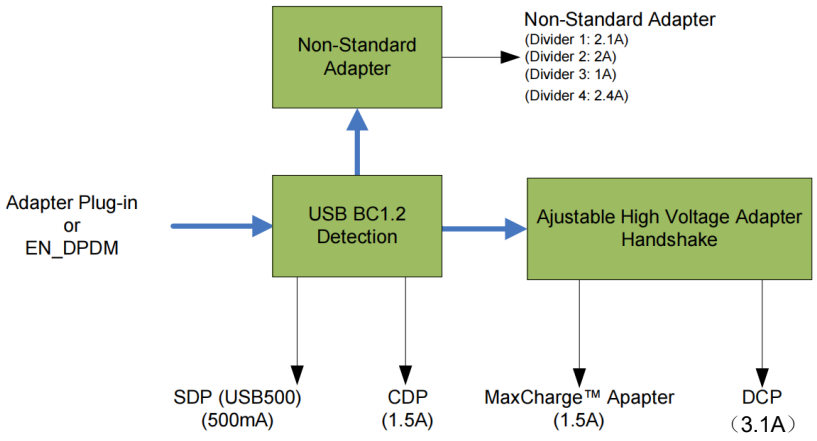


Figure 1. USB D+/D- Detection

Table1. Non-Standard Adapter Detection

Non-Standard Adapter	D + Threshold	D - Threshold	Input Current Limit (A)
Divider 1	V_{D+} within V_{2P7_VTH}	V_{D-} within V_{2P0_VTH}	2.1
Divider 2	V_{D+} within V_{1P2_VTH}	V_{D-} within V_{1P2_VTH}	2
Divider 3	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P7_VTH}	1
Divider 4	V_{D+} within V_{2P7_VTH}	V_{D-} within V_{2P7_VTH}	2.4

After the Input Source Type Detection is done, an INT pulse is asserted to the host. In addition, the following registers including Input Current Limit register (IINLIM), VBUS_STAT, and SDP_STAT are updated as below:

Table2. ET95603 Result

D+/ D- DETECTION	INPUT CURRENT LIMIT (IINLIM)	SDP_STAT	VBUS_STAT
USB SDP (USB500)	500 mA	1	001
USB CDP	1.5 A	1	010
USB DCP	3.1 A	1	011
Divider 3	1 A	1	110
Divider 1	2.1 A	1	110
Divider 4	2.4 A	1	110
Divider 2	2 A	1	110
Unknown Adapter	500 mA	1	101

Force Input Current Limit Detection

In host mode, the host can force the device to run by setting FORCE_DPDM bit. After the detection is completed, FORCE_DPDM bit returns to 0 by itself and Input Result is updated.

Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device supports wide range of input voltage limit (3.9V – 14.5 V) for high voltage charging and provides two methods to set Input Voltage Limit (VINDPM) threshold to facilitate autonomous detection.

1. Absolute VINDPM (FORCE_VINDPM=1)

   By setting FORCE_VINDPM bit to 1, the VINDPM threshold setting algorithm is disabled. Register VINDPM is writable and allows host to set the absolute threshold of VINDPM function.

2. Relative VINDPM based on VINDPM_OS registers (FORCE_VINDPM=0) (Default)

When FORCE_VINDPM bit is 0 (default), the VINDPM threshold setting algorithm is enabled. The VINDPM register is read only and the charger controls the register by using VINDPM Threshold setting algorithm The algorithm allows a wide range of adapter (V_{VBUS_OP}) to be used with flexible VINDPM threshold. After Input Voltage Limit Threshold is set, an INT pulse is generated to signal to the host.

Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current limit is forced to the lower of 200 mA or IINLIM register setting. After the system rises above 2.2 V, the device limits input current to the IILIM register (ICO_EN = 0) or IDPM_LIM register (ICO_EN = 1).

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal sawtooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the PMID voltage to cancel out any loop gain variation due to a change in input voltage.

In order to improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

Boost Mode Operation From Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 500 mA (BOOST_LIM bits = 000) output requirement. The maximum output current is up to 2.4 A. The boost operation can be enabled if the conditions are valid:

1. BAT above BAT_{LOWV}
2. VBUS less than BAT+V_{SLEEP} (in sleep mode)
3. Boost mode operation is enabled (OTG pin HIGH and OTG_CONFIG bit = 1)
4. Voltage at TS (thermistor) pin is within range configured by Boost Mode Temperature Monitor as configured by B_{HOT} and B_{COLD} bits

5. After 30 ms delay from boost mode enable

In boost mode, the device employs a 500 kHz or 1.5 MHz (selectable using BOOST_FREQ bit) step-up switching regulator based on system requirements. To avoid frequency change during boost mode operations, write to boost frequency configuration bit (BOOST_FREQ) is ignored when OTG_CONFIG is set.

During boost mode, the status register VBUS_STAT bits is set to 111, the VBUS output is 5V by default (selectable via BOOSTV register bits) and the output current can reach up to 2.4 A, selected via I^2C (BOOST_LIM bits). The boost output is maintained when BAT is above VOTG_BAT threshold.

Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car charger. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS_MIN bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5 V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of BATFET. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

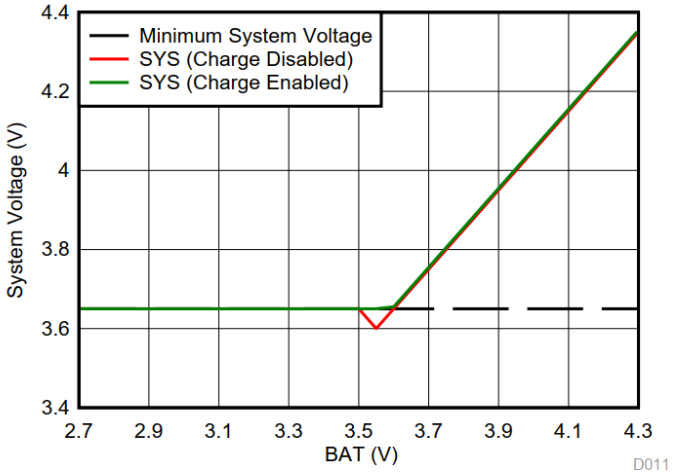


Figure 2. V_{SYS} vs V_{BAT}

Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IINLIM or IDPM_LIM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the Supplement Mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VDPM_STAT (VINDPM) and/or IDPM_STAT (IINDPM) is/are set high. Figure 3. shows the DPM response with 9V/1.2A adapter, 3.2-V battery, 2.8-A charge current and 3.4-V minimum system voltage setting.

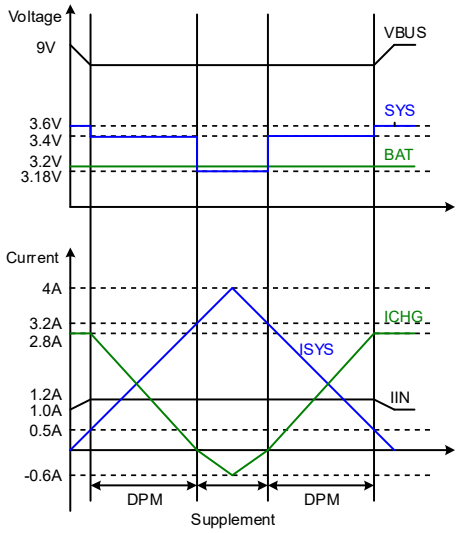


Figure 3. DPM Response

Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET VDS stays at 40 mV when the current is low. This prevents oscillation from entering and exiting the Supplement Mode. As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce RDS(ON) until the BATFET is in full conduction. At this point onwards, the BATFET VDS linearly increases with discharge current. BATFET turns off to exit Supplement Mode when the battery is below battery depletion threshold.

Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 5.0 A charge current for high capacity tablet battery. The 16mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

Autonomous Charging Cycle

With battery charging is enabled (CHG_CONFIG bit = 1 and CE pin is low), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table 3. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I^2C.

Table3. Charging Parameter Default Setting

DEFAULT MODE	ET95603
Charging voltage	4.208 V
Charging current	2.048 A
Pre-charge current	128 mA
Termination current	256 mA
Temperature profile	JEITA
Safety timer	12 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled by setting CHG_CONFIG bit, ICHG register is not 0 mA
- No thermistor fault on TS
- No safety timer fault
- BATFET is not forced to turn off (BATFET_DIS bit = 0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and device not in DPM mode or thermal regulation. When a full battery voltage is discharged below recharge threshold (threshold selectable via VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, either CE pin or CHG_CONFIG bit can initiate a new charging cycle.

The STAT output indicates the charging status of charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting STAT_DIS bit. In addition, the status register (CHRG_STAT) indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is completed, an INT is asserted to notify the host.

Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and regulates current / voltage.

Table4. Charging Current Setting

V_{BAT}	CHARGING CURRENT	REG DEFAULT SETTING	CHRG_STAT
< 2 V	$I_{BATSHORT}$	-	01
2 V to 3 V	I_{PRECHG}	128 mA	01
> 3 V	I_{CHG}	2048 mA	10

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. in this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

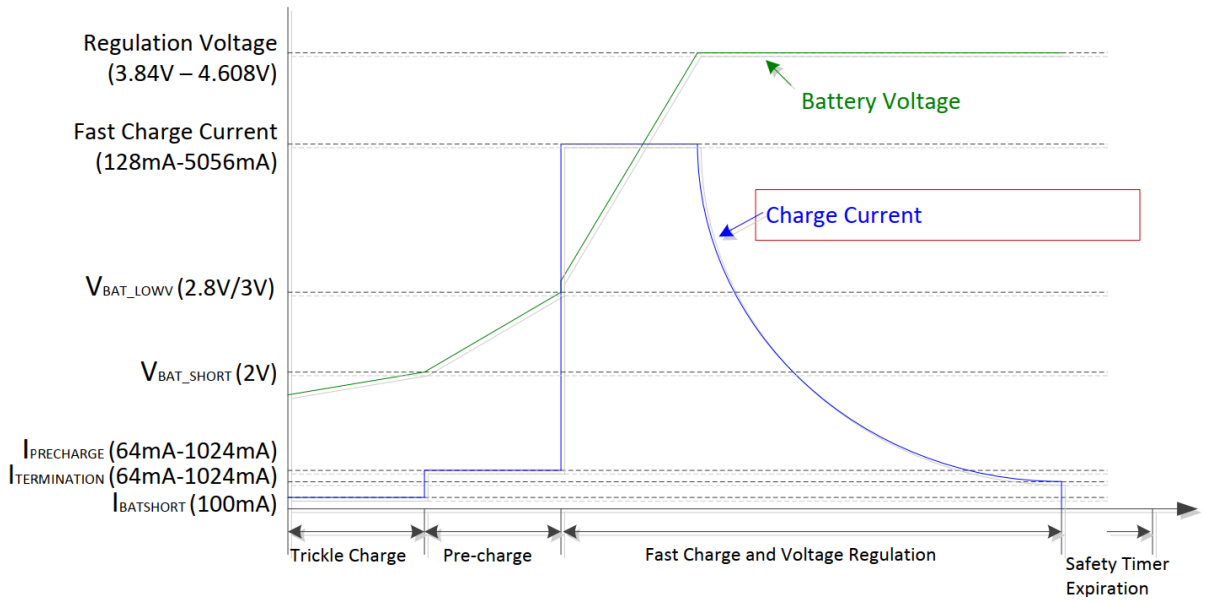


Figure 4. Battery Charging Profile

Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

When termination occurs, the status register CHRG_STAT is set to 11, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

Resistance Compensation (IRCOMP)

For high current charging system, resistance between charger output and battery cell terminal such as board routing, connector, MOSFETs and sense resistor can force the charging process to move from constant current to constant voltage too early and increase charge time. To speed up the charging cycle, the device provides resistance compensation (IRCOMP) feature which can extend the constant current charge time to delivery maximum power to battery.

The device allows the host to compensate for the resistance by increasing the voltage regulation set point based on actual charge current and the resistance as shown below. For safe operation, the host should set the maximum allowed regulation voltage register (VCLAMP) and the minimum resistance compensation (BATCOMP).

$$V_{REG\_ACTUAL} = VREG + \min(I_{CHRG\_ACTUAL} \times BATCOMP, V_{CLAMP}) \quad (1)$$

Thermistor Qualification

JEITA Guideline Compliance in Charging Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

The device continuously monitors battery temperature by measuring the voltage between the TS pins and ground, typically determined by a negative temperature coefficient thermistor (NTC) and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1–T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range. At cool temperature (T1–T2), JEITA recommends the charge current to be reduced to at least half of the charge current or lower. At warm temperature (T3–T5), JEITA recommends charge voltage below nominal charge voltage.

The device provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3–T5) can be 200 mV below charge voltage (JEITA_VSET=0). The current setting at cool temperature (T1–T2) can be further reduced to 20% or 50% of fast charge current (JEITA_ISET bit).

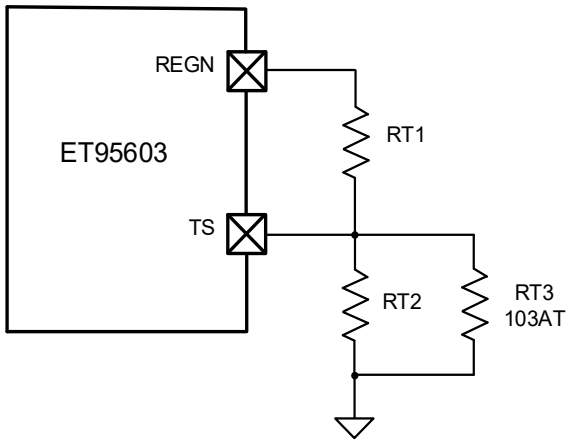


Figure 5. TS Resistor Network

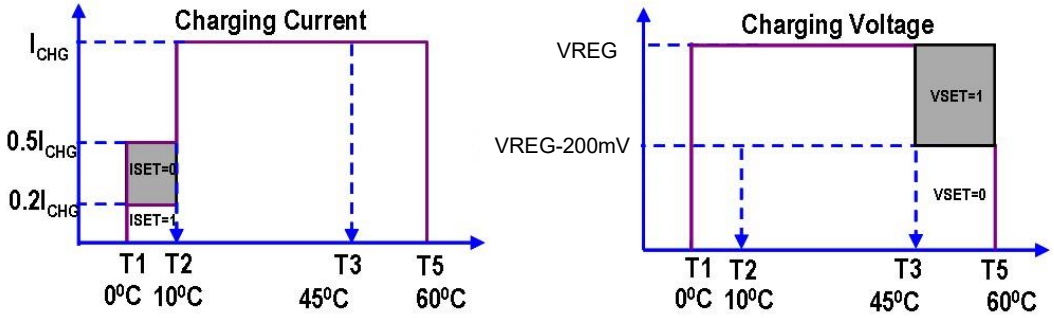


Figure 6. Charging Values

Assuming a 103AT NTC thermistor on the battery pack as shown in Figure 5, the value RT1 and RT2 can be determined by using Equation 2:

$$RT2 = \frac{V_{REGN} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{V_{REGN}}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{V_{REGN}}{VT1} - 1\right)}$$

$$RT1 = \frac{\frac{V_{REGN}}{VT1} - 1}{\frac{1}{RT1} + \frac{1}{RTH_{COLD}}} \quad (2)$$

Select 0 °C to 60 °C range for Li-ion or Li-polymer battery:

- RTH_{COLD} = 27.28 kΩ
- RTH_{HOT} = 3.02 kΩ
- RT1 = 5.24 kΩ
- RT2 = 30.31 kΩ

JEITA Guideline Compliance During Boost Mode

For battery protection during boost mode, the device monitors the battery temperature to be within the V_{BCOLDx} to V_{BHOT2} thresholds unless boost mode temperature is disabled by setting BHOT bits to 11. When temperature is outside of the temperature thresholds, the boost mode is suspended. Once temperature is within thresholds, the boost mode is recovered.

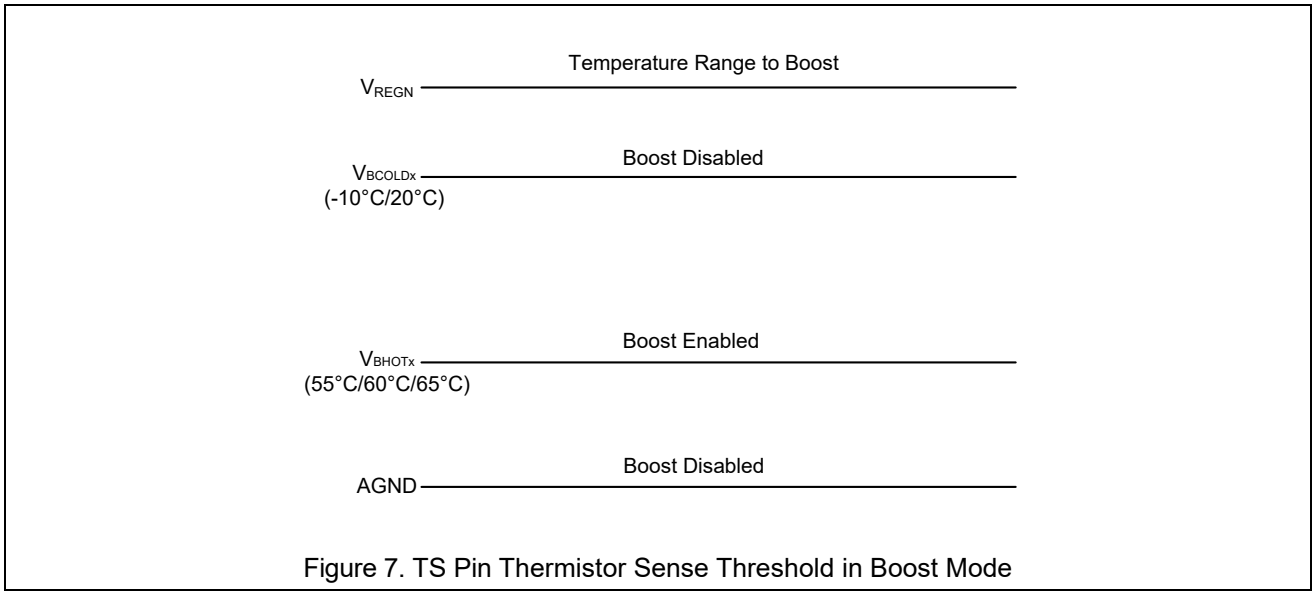


Figure 7. TS Pin Thermistor Sense Threshold in Boost Mode

Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 4 hours when the battery is below $V_{BATLOWV}$ threshold. The user can program fast charge safety timer through I^2C (CHG_TIMER bits). When safety timer expires, the fault register CHRG_FAULT bits are set to 11 and an INT is asserted to the host. The safety timer feature can be disabled via I^2C by setting EN_TIMER bit.

During input voltage, current or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IDPM_STAT = 1) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This half clock rate feature can be disabled by writing 0 to TMR2X_EN bit.

Battery Monitor

The device includes a battery monitor to provide measurements of VBUS voltage, battery voltage, system voltage, thermistor ratio, and charging current, and charging current based on the device modes of operation. The measurements are reported in Battery Monitor Registers (REG0E-REG12). The battery monitor can be configured as two conversion modes by using CONV_RATE bit: one-shot conversion (default) and 1 second continuous conversion.

For one-shot conversion (CONV_RATE = 0), the CONV_START bit can be set to start the conversion. During the conversion, the CONV_START is set and it is cleared by the device when conversion is completed. The conversion result is ready after tCONV (maximum 1 second).

For continuous conversion (CONV_RATE = 1), the CONV_RATE bit can be set to initiate the conversion. During active conversion, the CONV_START is set to indicate conversion is in progress. The battery monitor provides conversion result every 1 second automatically. The battery monitor exits continuous conversion mode when CONV_RATE is cleared.

When battery monitor is active, the REGN power is enabled and can increase device quiescent current. In battery only mode, the battery monitor is only active when V_{BAT} > SYS_MIN setting in REG03.

Table 5. Battery Monitor Modes of Operation

PARAMETER	REGISTER	MODES OF OPERATION			
		CHARGE MODE	BOOST MODE	DISABLE CHARGE MODE	BATTERY ONLY MODE
Battery Voltage (V_{BAT})	REG0E	Yes	Yes	Yes	Yes
System Voltage (V_{SYS})	REG0F	Yes	Yes	Yes	Yes
Temperature (TS) as percentage of REGN	REG10	Yes	Yes	Yes	Yes
VBUS Voltage (V_{VBUS})	REG11	Yes	Yes	Yes	NA
Charge Current (I_{BAT})	REG12	Yes	NA	NA	NA

Status/Control Outputs (STAT, INT and DSEL)

Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED as shown in Table 6. The STAT pin function can be disable by setting STAT_DIS bit.

Table 6. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input overvoltage, TS fault, timer fault, input or system overvoltage). Boost Mode suspend (due to TS Fault)	blinking at 1 Hz

Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT pulse notifies the system on the device operation. The following events will generate 256 μs INT pulse.

- USB/adapter source identified (through DSEL or DPDM detection, with OTG pin)
- Good input source detected
  - – VBUS above battery (not in sleep)
  - – VBUS below V_{ACOV} threshold
  - – VBUS above $V_{VBUSMIN}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Input removed
- Charge Complete
- Any FAULT event in REG0C

When a fault occurs, the charger device sends out INT and keeps the fault state in REG0C until the host reads the fault register. Before the host reads REG0C and all the faults are cleared, the charger device would not send any INT upon new faults. To read the current fault status, the host has to read REG0C two times consecutively. The 1st read reports the pre-existing fault register status and the 2nd read reports the current fault register status.

D+/D- Multiplexer Selection Control

The DSEL pin is normally grounded and pulled-up by internally to 5V during input source type detection (when DPDM_EN=1 or FORCE_DPDM=1). The pin is normally low and drives high to indicate the D+/D- detection is in progress. When detection is completed, the pin maintains high logic when DCP or HVDCP is detected. The pin returns to logic low when other input source type is detected. In addition, while input source is plugged in or during OTG mode, the FORCE_DSEL bit can be set to force the DSEL pin to change from low to high regardless of input source type detected. When in battery discharge mode (not in OTG), the DSEL pin is always low.

BATFET(Q4) Control

BATFET Disable Mode (Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host set BATFET_DIS bit, the charger can turn off BATFET immediately or delay by t_{SM_DLY} as configurated by BATFET_DLY bit.

BATFET Enable (Exit Shipping Mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET_DIS, one of the following events can enable BATFET to restore system power:

1. Plug in adapter
2. A logic high to low transition on QON pin with $t_{SHIPMODE}$ deglitch time to enable BATFET to exit shipping mode

BATFET Full System Reset

The BATFET functions as a load switch between battery and system when input source is not plugged-in. By changing the state of BATFET from off to on, system connects to SYS can be effectively have a power-on-reset. The QON pin supports push-button interface to reset system power without host by change the state of BATFET.

When the QON pin is driven to logic low for t_{QON_RST} (typical 15 seconds) while input source is not plugged in and BATFET is enabled (BATFET_DIS=0), the BATFET is turned off for t_{BATFET_RST} and then it is re-enabled to reset system power. This function can be disabled by setting BATFET_RST_EN bit to 0.

D+/D- Output Driver

The device provides independent controlled voltage output drivers on D+ and D- pins to interface or emulate non-standard adapters when input source is plugged-in or OTG mode is enabled. The D+/D- drivers are disabled in high impedance mode (HiZ) by default or when DP_DAC or DM_DAC bits are set to 000. The drivers are enabled and controlled independently with predefined voltage threshold when DP_DAC and DM_DAC bits are set to values between 001 to 110.

When input source is plugged-in, the output drivers control (DP_DAC and DM_DAC) are reset to HiZ (000) to execute USB BC1.2 and built-in handshake during the input source type detection. The host is recommended to change DP_DAC and DM_DAC settings after input source type detection when VBUS_STAT/PG_STAT bits are updated.

When OTG mode is enabled, the drivers can be enabled to provide electrical signature on D+/D- to emulate USB non-standard adapters (Divider 1- 4) as shown in Table 1.

Input Current Limit on ILIM

For safe operation, the device has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (3)$$

The actual input current limit is the lower value between ILIM setting and register setting (IINLIM). For example, if the register setting is 111111 for 3.1 A, and ILIM has a 260 Ω resistor (KILIM = 390 max.) to ground for 1.5 A, the input current limit is 1.5 A. ILIM pin can be used to set the input current limit rather than the register settings when EN_ILIM bit is set. The device regulates ILIM pin at 0.8 V. If ILIM voltage exceeds 0.8 V, the device enters input current regulation (Refer to Dynamic Power Management section).

The ILIM pin can also be used to monitor input current when EN_ILIM is enabled. The voltage on ILIM pin is proportional to the input current. ILIM pin can be used to monitor the input current following Equation 4:

$$I_{IN} = \frac{K_{ILIM} \times V_{ILIM}}{R_{ILIM} \times 0.8V} \quad (4)$$

For example, if ILIM pin is set with 260 Ω resistor, and the ILIM voltage is 0.4 V, the actual input current 0.615A - 0.75 A (based on KILM specified). If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 0.8 V. If ILIM pin is short, the input current limit is set by the register.

The ILIM pin function can be disabled by setting EN_ILIM bit to 0. When the pin is disabled, both input current limit function and monitoring function are not available.

Thermal Regulation and Thermal Shutdown

Thermal Protection in Buck Mode

The device monitors the internal junction temperature TJ to avoid overheat the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds the preset thermal regulation limit (TREG bits), the device lowers down the charge current. The wide thermal regulation range from 60ºC to 120ºC allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds T_{SHUT}. The fault register CHRG_FAULT is set to 10 and an INT is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is below T_{SHUT_HYS}.

Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC surface temperature exceeds T_{SHUT}, the boost mode is disabled (converter is turned off) by setting OTG_CONFIG bit low and BATFET is turned off. When IC surface temperature is below T_{SHUT_HYS}, the BATFET is enabled automatically to allow system to restore and the host can re-enable OTG_CONFIG bit to recover.

Voltage and Current Monitoring in Buck and Boost Mode

Voltage and Current Monitoring in Buck Mode

The device closely monitors the input and system voltage, as well as HSFET current for safe buck and boost mode operations.

Input Overvoltage (ACOV)

The input voltage for buck mode operation is V_{VBUS_OP}. If VBUS voltage exceeds V_{ACOV}, the device stops switching immediately. During input over voltage (ACOV), the fault register CHRG_FAULT bits sets to 01. An INT is asserted to the host.

System Overvoltage Protection (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. When SYSOVP is detected, the converter stops immediately to clamp the overshoot.

Voltage and Current Monitoring in Boost Mode

The device closely monitors the VBUS voltage, as well as RBFET and LSFET current to ensure safe boost mode operation.

VBUS Overcurrent Protection

The charger device closely monitors the RBFET (Q1), and LSFET (Q3) current to ensure safe boost mode operation. During overcurrent condition when output current exceed (IOTG_OCP) the device operates in current limit mode for protection.The output voltage decreases as the output current increases until it drops to OTG_UVP(＜4V or VSYS), and the chip exits boost mode. When overcurrent condition is detected the fault register bit BOOST_FAULT is set high to indicate fault in boost operation. An INT is also asserted to the host.

Boost Mode Overvoltage Protection

When the VBUS voltage rises above regulation target and exceeds VOTG_OVP, the device enters overvoltage protection which stops switching, clears OTG_CONFIG bit and exits boost mode. At Boost overvoltage duration, the fault register bit (BOOST_FAULT) is set high to indicate fault in boost operation. An INT is also asserted to the host.

Battery Protection

Battery Overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register BAT_FAULT bit goes high and an INT is asserted to the host.

Battery Over-Discharge Protection

When battery is discharged below V_{BAT_DPL}, the BATFET is turned off to protect battery from over discharge. To recover from over-discharge, an input source is required at VBUS. When an input source is plugged in, the BATFET turns on. Thy is charged with $I_{BATSHORT}$ (typically 100 mA) current when the $V_{BAT} < V_{SHORT}$, or precharge current as set in I_{PRECHG} register when the battery voltage is between V_{SHORT} and $V_{BATLOWV}$.

System Overcurrent Protection

When the system is shorted or significantly overloaded (I_{BAT} > I_{BATOP}) so that its current exceeds the overcurrent limit, the device latches off BATFET. Section BATFET Enable (Exit Shipping Mode) can reset the latch-off condition and turn on BATFET.

Serial Interface

The device uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I²C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6AH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG14. Register read beyond REG14 (0x14) returns 0xFF. The I²C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

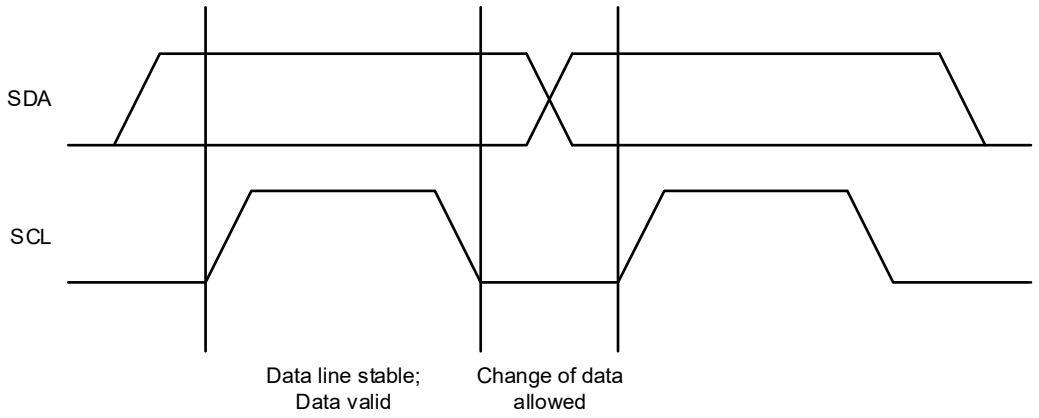


Figure 8. Bit Transfer on the I²C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

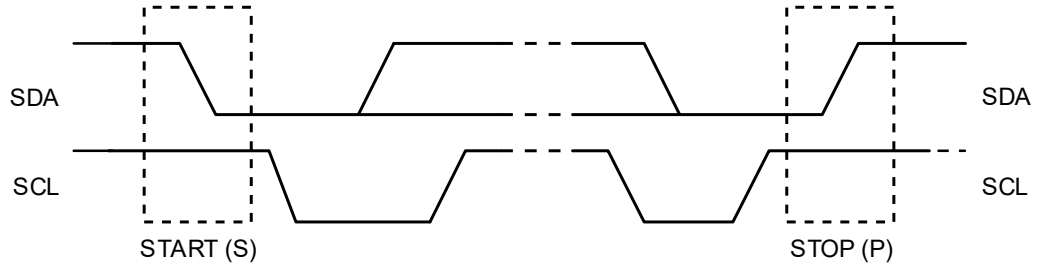


Figure 9. START and STOP conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

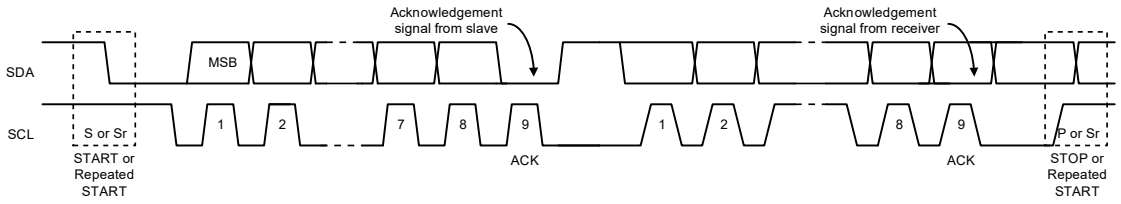


Figure 10. Data Transfer on the I²C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse,this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

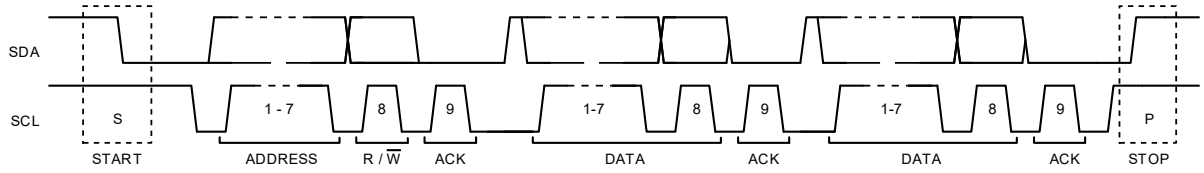


Figure 11. Complete Data Transfer

Single Read and Write

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

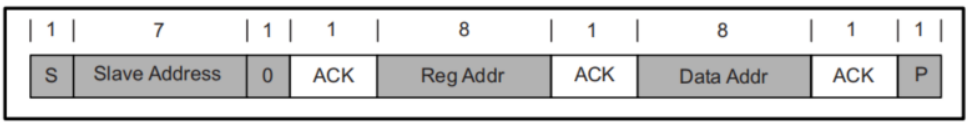


Figure 12. Single Write

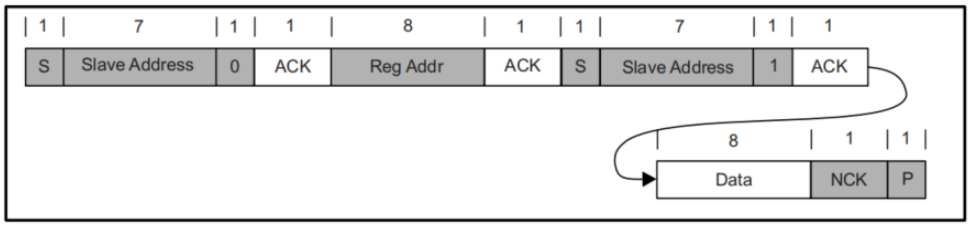


Figure 13. Single Read

Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG14 except REG0C.

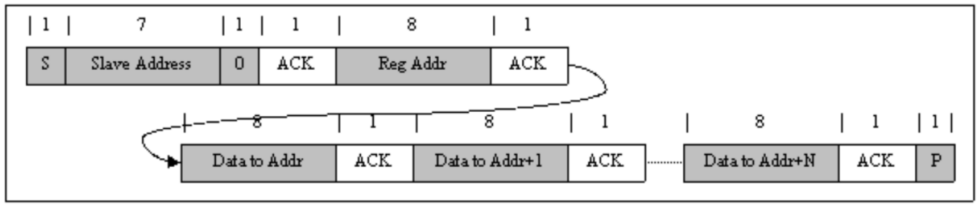


Figure 14. Multi_Write

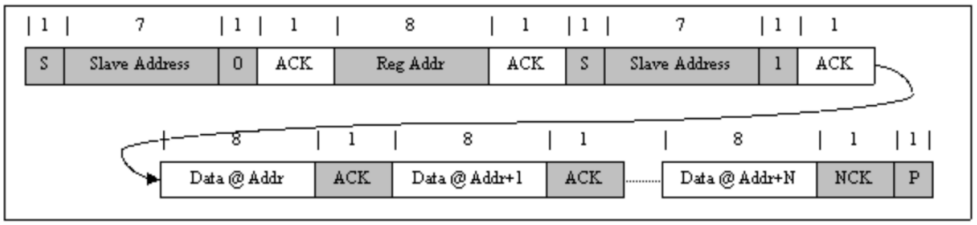


Figure 15. Multi_Read

REG0C is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG0C reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REG0C for the second time. The only exception is NTC_FAULT which always reports the actual condition on the TS pin. In addition, REG0C does not support multi-read and multi-write.

Device Functional Modes

Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WATCHDOG_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG_FAULT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings.

In default mode, the device keeps charging the battery with 12 hours fast charging safety timer. At the end of the 12 hours, the charging is stopped and the buck converter continues to operate to supply system load. Any write command to device transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits=00.

When the watchdog timer (WATCHDOG_FAULT bit = 1) is expired, the device returns to default mode and all registers are reset to default values except IINLIM, VINDPM, VINDPM_OS, BATFET_RST_EN, BATFET_DLY, and BATFET_DIS bits.

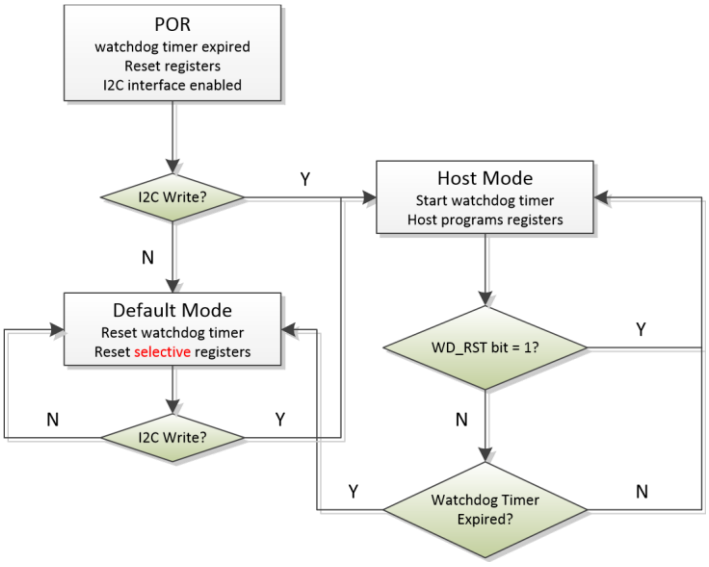


Figure 16. Watchdog Timer Flow Chart

Register Maps

I²C Slave Address: 6AH(1101010B+R/W)

REG00 (address = 00) [reset = 00001000]

REG00 Field Descriptions

Bit	Field	POR	Type[6]	Reset	Description	
7	EN_HIZ	0	R/W	by REG_RST by Watchdog	Enable HIZ Mode 0 - Disable 1 - Enable	
6	EN_ILIM	0	R/W	by REG_RST	Enable ILIM Pin 0 - Disable 1 - Enable	
5	IINLIM[5]	0	R/W	by REG_RST	1600 mA	Input Current Limit Offset: 100 mA Range: 100 mA (000000) - 3.1 A (111111) Default: 500 mA (001000), Input current value (n:6 bits) 0-1.65A：IINLIM=100+n x 50 (mA) 1.7-3.1A：IINLIM=n x 50-50 (mA) (Actual input current limit is the lower of I²C or ILIM pin) IINLIM bits are changed automatically after input source type detection is completed USB Host SDP = 500 mA USB CDP = 1.5 A USB DCP = 3.1 A Adjustable High Voltage DCP = 1.5 A Unknown Adapter = 500 mA Non-Standard Adapter = 1A/2A/2.1A/2.4A
4	IINLIM[4]	0	R/W	by REG_RST	800 mA	
3	IINLIM[3]	1	R/W	by REG_RST	400 mA	
2	IINLIM[2]	0	R/W	by REG_RST	200 mA	
1	IINLIM[1]	0	R/W	by REG_RST	100 mA	
0	IINLIM[0]	0	R/W	by REG_RST	50 mA	

Note6: LEGEND: R/W = Read/Write; R = Read only

REG01 (address = 01) [reset = 10100110]

REG01 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	BHOT[1]	1	R/W	by REG_RST by Watchdog	Boost Mode Hot Temperature Monitor Threshold 00 – V_{BHOT1} Threshold (34.5%) 01 – V_{BHOT0} Threshold (37.5%) 10 – V_{BHOT2} Threshold (31.5%) 11 – Disable boost mode thermal protection	
6	BHOT[0]	0	R/W	by REG_RST by Watchdog		
5	BCOLD	1	R/W	by REG_RST by Watchdog	Boost Mode Cold Temperature Monitor Threshold 0 – V_{BCOLD0} Threshold (77%) 1 – V_{BCOLD1} Threshold (80%)	
4	VINDPM_OS[4]	0	R/W	by REG_RST	1600mV	Input Voltage Limit Offset Default: 600 mV (00110) Range: 0 mV – 3100 mV When VBUS at noLoad is ≤ 6V, the VINDPM_OS is used to calculate VINDPM threshold When VBUS at noLoad is > 6V, the VINDPM_OS multiple by 2 is used to calculate VINDPM threshold.
3	VINDPM_OS[3]	0	R/W	by REG_RST	800mV	
2	VINDPM_OS[2]	1	R/W	by REG_RST	400mV	
1	VINDPM_OS[1]	1	R/W	by REG_RST	200mV	
0	VINDPM_OS[0]	0	R/W	by REG_RST	100mV	

REG02 (address = 02) [reset = 00010001]

REG02 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	CONV _START	0	R/W	by REG_RST by Watchdog	ADC Conversion Start Control 0 – ADC conversion not active (default). 1 – Start ADC Conversion. This bit is read-only when CONV_RATE=1. The bit stays high during ADC conversion and during input source detection.
6	CONV _RATE	0	R/W	by REG_RST by Watchdog	ADC Conversion Rate Selection 0 – One shot ADC conversion (default), 1 – Start 1s Continuous Conversion.
5	BOOST _FREQ	0	R/W	by REG_RST by Watchdog	Boost Mode Frequency Selection 0 – 1.5MHz 1 – 500kHz
4	ICO_EN	1	R/W	by REG_RST	Enable Input Current Limit Optimization (ICO) 0 – Disable 1 – Enable
3	HVDCP_EN	0	R/W	by REG_RST	High Voltage DCP Enable 0 – Disable HVDCP handshake (default) 1 – Enable HVDCP handshake
2	Reserved	0	R	NA	Reserved
1	FORCE _DPDM	0	R/W	by REG_RST by Watchdog	Force D+/D- Detection 0 – Not in D+/D- or PSEL detection 1 – Force D+/D- detection.
0	DPDM_EN	1	R/W	by REG_RST	D+/D- Detection Enable 0 – Disable D+/D- or DSEL detection when VBUS is plugged-in 1 – Enable D+/D- or DSEL detection when VBUS is plugged-in

REG03 (address = 03) [reset =00011010]

REG03 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	BAT _LOADEN	0	R/W	by REG_RST by Watchdog	Battery Load ($I_{BATLOAD}$) Enable 0 – Disable 1 – Enable	
6	WD_RST	0	R/W	NA	I^2C Watchdog Timer Reset 0 – Normal 1 – Reset (Back to 0 after timer reset)	
5	OTG _CONFIG	0	R/W	by REG_RST by Watchdog	Boost (OTG) Mode Configuration 0 – OTG Disable 1 – OTG Enable	
4	CHG _CONFIG	1	R/W	by REG_RST by Watchdog	Charge Enable Configuration 0 – Charge Disable 1 – Charge Enable	
3	SYS _MIN[2]	1	R/W	by REG_RST	0.4V	Minimum System Voltage Limit Offset: 3.0V Range: 3.0V – 3.7V Default: 3.5V (101)
2	SYS _MIN[1]	0	R/W	by REG_RST	0.2V	
1	SYS _MIN[0]	1	R/W	by REG_RST	0.1V	
0	MIN_VBAT _SEL	0	R/W	by REG_RST	Minimum Battery Voltage (falling) to exit boost mode 0 – 2.85V (default) 1 – 2.5V	

REG04 (address = 04) [reset = 00100000]

REG04 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	Reserved	0	R	NA	Reserved	
6	ICHG[6]	0	R/W	by REG_RST by Watchdog	4096mA	Fast Charge Current Limit Offset: 0mA Range:0mA(0000000)–5056mA(1001111) Default: 2048mA (0100000) Note: ICHG=0000000 (0mA) disables charge ICHG > 1001111 (5056mA) is clamped to register value 1001111 (5056mA)
5	ICHG[5]	1	R/W	by REG_RST by Watchdog	2048mA	
4	ICHG[4]	0	R/W	by REG_RST by Watchdog	1024mA	
3	ICHG[3]	0	R/W	by REG_RST by Watchdog	512mA	
2	ICHG[2]	0	R/W	by REG_RST by Watchdog	256mA	
1	ICHG[1]	0	R/W	by REG_RST by Watchdog	128mA	
0	ICHG[0]	0	R/W	by REG_RST by Watchdog	64mA	

REG05 (address = 05) [reset = 00010011]

REG05 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	IPRECHG[3]	0	R/W	by REG_RST by Watchdog	512mA	Precharge Current Limit Offset: 64mA Range: 64mA – 1024mA Default: 128mA (0001)
6	IPRECHG[2]	0	R/W	by REG_RST by Watchdog	256mA	
5	IPRECHG[1]	0	R/W	by REG_RST by Watchdog	128mA	
4	IPRECHG[0]	1	R/W	by REG_RST by Watchdog	64mA	
3	ITERM[3]	0	R/W	by REG_RST by Watchdog	512mA	Termination Current Limit Offset: 64mA Range: 64mA – 1024mA Default: 256mA (0011)
2	ITERM[2]	0	R/W	by REG_RST by Watchdog	256mA	
1	ITERM[1]	1	R/W	by REG_RST by Watchdog	128mA	
0	ITERM[0]	1	R/W	by REG_RST by Watchdog	64mA	

REG06 (address = 06) [reset = 01011110]

REG06 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	VREG[5]	0	R/W	by REG_RST by Watchdog	512mV	Charge Voltage Limit Offset: 3.840V Range: 3.840V – 4.608V (110000) Default: 4.208V (010111)
6	VREG[4]	1	R/W	by REG_RST by Watchdog	256mV	
5	VREG[3]	0	R/W	by REG_RST by Watchdog	128mV	
4	VREG[2]	1	R/W	by REG_RST by Watchdog	64mV	
3	VREG[1]	1	R/W	by REG_RST by Watchdog	32mV	
2	VREG[0]	1	R/W	by REG_RST by Watchdog	16mV	
1	BATLOWV	1	R/W	by REG_RST by Watchdog	Battery Low Threshold (Wakeup Charge to Fast Charge) 0 – 2.8V 1 – 3.15V	
0	VRECHG	0	R/W	by REG_RST by Watchdog	Battery Recharge Threshold (below VREG) 0 – 100mV 1 – 200mV	

REG07 (address = 07) [reset = 10011101]

REG07 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	EN_TERM	1	R/W	by REG_RST by Watchdog	Enable Charge Termination 0 – Disable 1 – Enable
6	STAT_DIS	0	R/W	by REG_RST by Watchdog	STAT Pin Disable 0 – Enable STAT pin function 1 – Disable STAT pin function
5	WATCHDOG [1]	0	R/W	by REG_RST by Watchdog	I^2C Watchdog Timer Setting 00 – Disable watchdog timer 01 – 40s (default) 10 – 80s 11 – 160s
4	WATCHDOG [0]	1	R/W	by REG_RST by Watchdog	
3	EN_TIMER	1	R/W	by REG_RST by Watchdog	Charging Safety Timer Enable 0 – Disable 1 - Enable
2	CHG _TIMER[1]	1	R/W	by REG_RST by Watchdog	Fast Charge Timer Setting 00 – 5 hrs 01 – 8 hrs 10 – 12 hrs 11 – 20 hrs
1	CHG _TIMER[0]	0	R/W	by REG_RST by Watchdog	
0	JEITA_ISET	1	R/W	by REG_RST by Watchdog	JEITA Low Temperature Charge Current Setting 0 – 50% of CC 1 – 20% of CC

REG08 (address = 08) [reset = 00000011]

REG08 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	BAT_COMP[2]	0	R/W	by REG_RST by Watchdog	80mΩ	IR Compensation Resistor Setting Range: 0 – 140mΩ Default: 0mΩ (000)
6	BAT_COMP[1]	0	R/W	by REG_RST by Watchdog	40mΩ	
5	BAT_COMP[0]	0	R/W	by REG_RST by Watchdog	20mΩ	
4	VCLAMP[2]	0	R/W	by REG_RST by Watchdog	128mV	IR Compensation Resistor Setting Offset: 0mV Range: 0 – 224mV Default: 0mV (000)
3	VCLAMP[1]	0	R/W	by REG_RST by Watchdog	64mV	
2	VCLAMP[0]	0	R/W	by REG_RST by Watchdog	32mV	
1	TREG[1]	1	R/W	by REG_RST by Watchdog	Thermal Regulation Threshold 00 – Disable	
0	TREG[0]	1	R/W	by REG_RST by Watchdog	01 - 80°C 10 - 100°C 11 - 120°C	

REG09 (address = 09) [reset = 01000100]

REG09 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	Reserved	0	R	NA	Reserved
6	TMR2X_EN	1	R/W	by REG_RST by Watchdog	Safety Timer Setting during DPM or Thermal Regulation 0 – Safety timer not slowed by 2X during input DPM or thermal regulation 1 – Safety timer slowed by 2X during input DPM or thermal regulation
5	BATFET_DIS	0	R/W	by REG_RST	Force BATFET off to enable ship mode 0 – Allow BATFET turn on, 1 – Force BATAFET off
4	JEITA_VSET	0	R/W	by REG_RST by Watchdog	JEITA High Temperature Charge Voltage Setting 0 – Set Charge Voltage to VREG-200mV during JEITA high temperature 1 – Set Charge Voltage to VREG during JEITA high temperature
3	BATFET_DLY	0	R/W	by REG_RST	BATFET turn off delay when BATET_DIS bit is set 0 – Add 33ms delay time 1 – Add 10s delay time
2	BATFET_RST_EN	1	R/W	by REG_RST	BATFET full system reset enable 0 – Disable BATFET full system reset 1 – Enable BATFET full system reset
1	Reserved	0	R	NA	Reserved
0	Reserved	0	R	NA	Reserved

REG0A (address = 0A) [reset = 01110011]

REG0A Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	BOOSTV[3]	0	R/W	by REG_RST	512mV	Boost Mode Voltage Regulation Offset: 4.55V Range: 4.55V – 5.51V Default: 4.998V (0111)
6	BOOSTV[2]	1	R/W	by REG_RST by Watchdog	256mV	
5	BOOSTV[1]	1	R/W	by REG_RST	128mV	
4	BOOSTV[0]	1	R/W	by REG_RST by Watchdog	64mV	
3	PFM _DIS	0	R/W	by REG_RST	PFM mode disable 0 – Allow PFM (default) 1 – Disable PFM	
2	BOOST_LIM[2]	0	R/W	by REG_RST	Boost Mode Current Limit 000: 0.5A 001: 0.75A 010: 1.2A 011: 1.4A 100: 1.65A 101: 1.875A 110: 2.15A 111: 2.45A Default: 1.4A (011)	
1	BOOST_LIM[1]	1	R/W	by REG_RST by Watchdog		
0	BOOST_LIM[0]	1	R/W	by REG_RST by Watchdog		

REG0B (address = 0B) [reset = 00000010]

REG0B Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	VBUS_STAT[2]	0	R	NA	VBUS Status register 000: No Input 001: USB Host SDP 010: USB CDP (1.5A) 011: USB DCP (3.1A) 100: Adjustable High Voltage DCP (1.5A) 101: Unknown Adapter (500mA) 110: Non-Standard Adapter (1A/2A/2.1A/2.4A) 111: OTG Note: Software current limit is reported in IINLIM register
6	VBUS_STAT[1]	0	R	NA	
5	VBUS_STAT[0]	0	R	NA	
4	CHRG_STAT[1]	0	R	NA	Charging Status 00 – Not Charging, 01 – Pre-charge (<VBATLOWV) 10 – Fast Charging, 11 – Charge Termination Done
3	CHRG_STAT[0]	0	R	NA	
2	PG_STAT	0	R	NA	Power Good Status 0 – Not Power Good, 1 – Power Good
1	SDP_STAT	1	R	NA	USB Input Status 0 – USB100 input is detected 1 – USB500 input is detected (this bit always read 1 when VBUS_STAT is not 001)
0	VSYS_STAT	0	R	NA	VSYS Regulation Status 0 – Not in VSYSMIN regulation (BAT>VSYSMIN) 1 – In VSYSMIN regulation (BAT<VSYSMIN)

REG0C (address = 0C) [reset = 10000000]

REG0C Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	WATCHDOG _FAULT	1	R	NA	I²C Watchdog Fault Status 0 – Normal 1 – Watchdog timer expiration
6	BOOST _FAULT	0	R	NA	Boost Mode Fault Status 0 – Normal 1 – VBUS overloaded in OTG, or VBUS OVP, or battery is too low in boost mode
5	CHRG _FAULT[1]	0	R	NA	Charger Fault Status 00 – Normal 01 – Input fault ($V_{BUS}>V_{ACOV}$ or $V_{BAT}<V_{BUS}<V_{BUSMIN}$ (typical 3.8V)) 10 – Thermal shutdown 11 – Charger Safety Timer Expiration
4	CHRG _FAULT[0]	0	R	NA	
3	BAT _FAULT	0	R	NA	Battery Fault Status 0 – Normal 1 – BATOVP ($V_{BAT}>V_{BATOVP}$)
2	NTC _FAULT[2]	0	R	NA	NTC Fault Status Buck Mode: 000 – Normal 010 – TS Warm 011 – TS Cool 101 – TS Cold 110 – TS Hot Boost Mode: 000 – Normal 101 – TS Cold 110 – TS Hot
1	NTC _FAULT[1]	0	R	NA	
0	NTC _FAULT[0]	0	R	NA	

REG0D (address = 0D) [reset = 00010010]

REG0D Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	FORCE _VINDPM	0	R/W	by REG_RST	VINDPM Threshold Setting Method 0 - Run Relative VINDPM Threshold 1 - Run Absolute VINDPM Threshold Note:Register is reset to default value when input source is plugged in.	
6	VINDPM[6]	0	R/W	by REG_RST	6400mV	Absolute VINDPM Threshold Offset: 2.6V Range: 4V (0001101) - 15.3V (1111111) Default: 4.4V (0010010) Note: Register is read only when FORCE_VINDPM=0 and can be written by internal control based on relative VINDPM threshold setting Register can be read/write when FORCE_VINDPM=1 Note: Register is reset to default value when input source is plugged in.
5	VINDPM[5]	0	R/W	by REG_RST	3200mV	
4	VINDPM[4]	1	R/W	by REG_RST	1600mV	
3	VINDPM[3]	0	R/W	by REG_RST	800mV	
2	VINDPM[2]	0	R/W	by REG_RST	400mV	
1	VINDPM[1]	1	R/W	by REG_RST	200mV	
0	VINDPM[0]	0	R/W	by REG_RST	100mV	

REG0E (address = 0E) [reset = 00000000]

REG0E Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	THERM_STAT	0	R	NA	Thermal Regulation Status 0 - Normal 1 - In Thermal Regulation	
6	BATV[6]	0	R	NA	1280mV	ADC conversion of Battery Voltage (V_{BAT}) Offset: 2.304V Range: 2.304V (0000000) - 4.848V (1111111) Default: 2.304V (0000000)
5	BATV[5]	0	R	NA	640mV	
4	BATV[4]	0	R	NA	320mV	
3	BATV[3]	0	R	NA	160mV	
2	BATV[2]	0	R	NA	80mV	
1	BATV[1]	0	R	NA	40mV	
0	BATV[0]	0	R	NA	20mV	

REG0F (address = 0F) [reset = 10000000]

REG0F Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	ACOV_TH[0]	1	R/W	by REG_RST	ACOV threshold: LV version: 0 - 5.5V 1 - 6.5V (5V input, default), HV version: 0 - 10.5V (9V input) 1 - 14.5V (12V input)	
6	SYSV[6]	0	R	NA	1280mV	ADC conversion of System Voltage (V_{SYS}) Offset: 2.304V Range: 2.304V (0000000) - 4.848V (1111111) Default: 2.304V (0000000)
5	SYSV[5]	0	R	NA	640mV	
4	SYSV[4]	0	R	NA	320mV	
3	SYSV[3]	0	R	NA	160mV	
2	SYSV[2]	0	R	NA	80mV	
1	SYSV[1]	0	R	NA	40mV	
0	SYSV[0]	0	R	NA	20mV	

REG10 (address = 10) [reset = 10000000]

REG10 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	ACOV_TH[1]	1	R/W	by REG_RST	ACOV threshold: 0 - LV version 1 - HV version	
6	TSPCT[6]	0	R	NA	29.76%	ADC conversion of TS Voltage (TS) as percentage of REGN Offset: 21% Range: 21% (0000000) - 80% (1111111) Default: 21% (0000000)
5	TSPCT[5]	0	R	NA	14.88%	
4	TSPCT[4]	0	R	NA	7.44%	
3	TSPCT[3]	0	R	NA	3.72%	
2	TSPCT[2]	0	R	NA	1.86%	
1	TSPCT[1]	0	R	NA	0.93%	
0	TSPCT[0]	0	R	NA	0.47%	

REG11 (address = 11) [reset = 00000000]

REG11 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	VBUS_GD	0	R	NA	VBUS Good Status 0 - Not VBUS attached 1 - VBUS attached	
6	VBUSV[6]	0	R	NA	6400mV	ADC conversion of VBUS voltage (V_{BUS}) Offset: 2.6V Range: 2.6V (0000000) - 15.3V (1111111) Default: 2.6V (0000000)
5	VBUSV[5]	0	R	NA	3200mV	
4	VBUSV[4]	0	R	NA	1600mV	
3	VBUSV[3]	0	R	NA	800mV	
2	VBUSV[2]	0	R	NA	400mV	
1	VBUSV[1]	0	R	NA	200mV	
0	VBUSV[0]	0	R	NA	100mV	

REG12 (address = 12) [reset = 00000000]

REG12 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	VREG_FT	0	R/W	by REG_RST by Watchdog	8mV	VREG Fine Tuning 0 = Disable (default) 1 = VREG+8mV
6	ICHGR[6]	0	R	NA	3200mA	ADC conversion of Charge Current (I_{BAT}) when $V_{BAT} > V_{BATSHORT}$ Offset: 0mA Range: 0mA (0000000) - 6350mA (1111111) Default: 0mA (0000000) Note: This register returns 0000000 for $V_{BAT} < V_{BATSHORT}$
5	ICHGR[5]	0	R	NA	1600mA	
4	ICHGR[4]	0	R	NA	800mA	
3	ICHGR[3]	0	R	NA	400mA	
2	ICHGR[2]	0	R	NA	200mA	
1	ICHGR[1]	0	R	NA	100mA	
0	ICHGR[0]	0	R	NA	50mA	

REG13 (address = 13) [reset = 00000000]

REG13 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	VDPM_STAT	0	R	NA	VINDPM Status 0 - Not in VINDPM 1 - VINDPM	
6	IDPM_STAT	0	R	NA	IINDPM Status 0 - Not in IINDPM 1 - IINDPM	
5	IDPM_LIM[5]	0	R	NA	1600mA	Input Current Limit in effect while Input Current Optimizer (ICO) is enabled Offset: 100mA Range: 100mA (000000) - 3.1A (111111) Input current value (n:6 bits) 0-1.65A：IINLIM=100+n x 50 (mA) 1.7-3.1A：IINLIM=n x 50-50 (mA)
4	IDPM_LIM[4]	0	R	NA	800mA	
3	IDPM_LIM[3]	0	R	NA	400mA	
2	IDPM_LIM[2]	0	R	NA	200mA	
1	IDPM_LIM[1]	0	R	NA	100mA	
0	IDPM_LIM[0]	0	R	NA	50mA	

REG14 (address = 14) [reset = 00011100]

REG14 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	REG_RST	0	R/W	NA	Register Reset 0 - Keep current register setting 1 - Reset to default register value and reset safety timer Note: Reset to 0 after register reset is completed
6	Reserved	0	R	NA	Reserved
5	PN[2]	0	R	NA	Part Number 011: ET95603
4	PN[1]	1	R	NA	
3	PN[0]	1	R	NA	
2	TS _PROFILE	1	R	NA	Temperature Profile 1 - JEITA (default)
1	Rev[1]	0	R	NA	Device Revision: 00
0	Rev[0]	0	R	NA	

REG15 (address = 15) [reset = 00000000]

REG15 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	DP_DAC[2]	0	R/W	by REG_RST	D+/D- Pin Output Driver 000 - HiZ mode (default) 001 - 0V (V_{0P0_VSRC}) 010 - 0.6V (V_{0P6_VSRC}) 011 - 1.2V (V_{1P2_VSRC}) 100 - 2.0V (V_{2P0_VSRC}) 101 - 2.7V (V_{2P7_VSRC}) 110 - 3.3V (V_{3P3_VSRC}) 111 - Reserved Register bits are reset to default value when input source is plugged and can be changed after D+/D- detection is competed.
6	DP_DAC[1]	0	R/W	by REG_RST	
5	DP_DAC[0]	0	R/W	by REG_RST	
4	DM_DAC[2]	0	R/W	by REG_RST	
3	DM_DAC[1]	0	R/W	by REG_RST	
2	DM_DAC[0]	0	R/W	by REG_RST	
1	EN_12V	0	R/W	by REG_RST	Enable 12V detection for HVDCP 0 - Disable 12V Detection (default) 1 - Enable 12V Detection
0	FORCE _DSEL	0	R/W	by REG_RST	DSEL Pin Control 0 - Allow DSEL pin inactive 1 - Force DSEL pin active

REG16 (address = 16) [reset = 01000000]

REG16 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	DBS_QON	0	R/W	by REG_RST	Debounce time for QON pull low to exit ship mode 0 - 1.7s 1 - 3.4s
6	DBS_SLEEP	1	R/W	by REG_RST	Debounce time for sleep mode falling edge 0 - 0us 1 - 14ms
5	DBS_ILOW	0	R/W	by REG_RST	Debounce time for ILOW (End-Of-Charge current detection) 0 - 250ms 1 - 1s
4	DBS_BATOVP	0	R/W	by REG_RST	BAT_OVP debounce time 0 - 10us 1 - 320us
3	DBS_BATOCP	0	R/W	by REG_RST	BAT_OCP debounce time To turn off OTG: 0 - 128us 1 - 1ms To turn off BATFET: 0 - 256us 1 - 2ms
2	DBS_OTGOUVP	0	R/W	by REG_RST	OTG OVP/UVP debounce time 0 - 8ms 1 - 50ms
1	DBS_BUSOCP	0	R/W	by REG_RST	OTG BUS_OCP debounce time 0 - 16ms 1 - 128us
0	DBS_LSOCP	0	R/W	by REG_RST	OTG LS_OCP debounce time 0 - 16 cycles 1 - 64 cycles

REG17 (address = 17) [reset = 00100000]

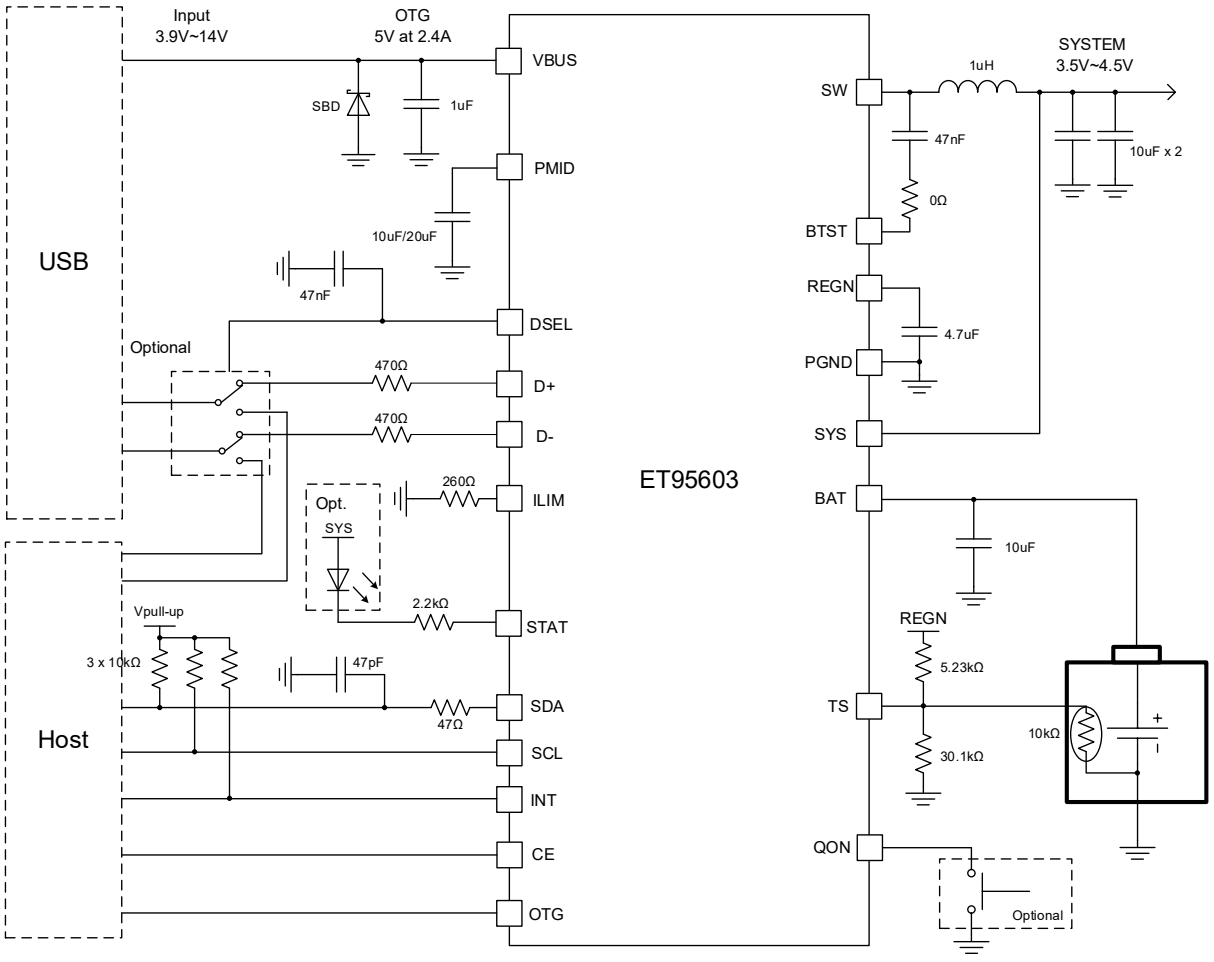
REG17 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	OPT_ILMT	0	R/W	by REG_RST	OTG OCP mode 0 – ILMT_OCP 1 – Hiccup-OCP
6	OPT_BATGD	0	R/W	by REG_RST	BAT_GD=0 automatically exit HIZ mode 0 – Disable 1 – Enable
5	OPT_IBUSLOW	1	R/W	by REG_RST	IBUSLOW=0 blanking sleep mode 0 – Disable 1 – Enable
4	OPT_Q1FULLON	0	R/W	by REG_RST	Q1 Full-on
3	TS_PIN_DIS	0	R/W	by REG_RST	Disable TS pin
2	OTG_PIN_DIS	0	R/W	by REG_RST	Disable OTG pin (only use OTG_CONFIG bit)
1	DRV_CAP	0	R/W	by REG_RST	DP/DM DAC driving capability 0 – 2mA 1 – 10mA
0	SINKI	0	R/W	by REG_RST	DP/DM sink current in BC1.2 detection 0 – 50uA 1 – 100uA

Application information

A typical application consists of the device configured as an I²C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphones and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

Typical Application Circuit



Recommended C1 = 10 µF (OTG ≤ 1.5 A) or 20 µF (OTG ≤ 2.4 A)

Figure 17. ET95603 with D+/D- Interface and USB On-The-Go (OTG)

Design Requirements

For this design example, use the parameters shown in Table 7.

Table7. Design Parameter

PARAMETER	VALUE
Input voltage range	3.9 V to 14.5 V
Input current limit	1.5 A
Fast charge current	5000m A
Output voltage	4.352V
V_{REF} system pullup voltage	1.8 V - 3.3V

Detailed Design Procedure

Inductor Selection

The device has 1.5 MHz switching frequency to allow the use of small inductor and capacitor values. The Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2) \times I_{RIPPLE} \quad (5)$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle (D = V_{BAT}/V_{VBUS}), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{BUS} \times D \times (1-D)}{fs \times L} \quad (6)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of (20 – 40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

Buck Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current IPMID occurs where the duty cycle is closest to 50% and can be estimated using:

$$I_{PMID} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (7)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25 V rating or higher capacitor is preferred for up to 14-V input voltage. 8.2-μF capacitance is suggested for typical of 3 A – 5 A charging current.

System Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current ICOUT is given:

$$I_{CSYS} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (8)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{SYS}}{8LC_{SYS}fs^2}\left(1 - \frac{V_{SYS}}{V_{BUS}}\right) \quad (9)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC. The charger device has internal loop compensator. To get good loop stability, 1 μH and minimum of 20 μF output capacitor is recommended. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R.

Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 4 V and 14 V input with at least 100-mA current rating connected to VBUS or a single-cell Li-Ion battery with voltage > VBATUVLO connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

Layout

Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see the Figure 18) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.

2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.

3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.

4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0 Ω resistor to tie analog ground to power ground.

5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.

6. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.

7. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.

8. Ensure that the number and sizes of vias allow enough copper for a given current path.

Layout Example

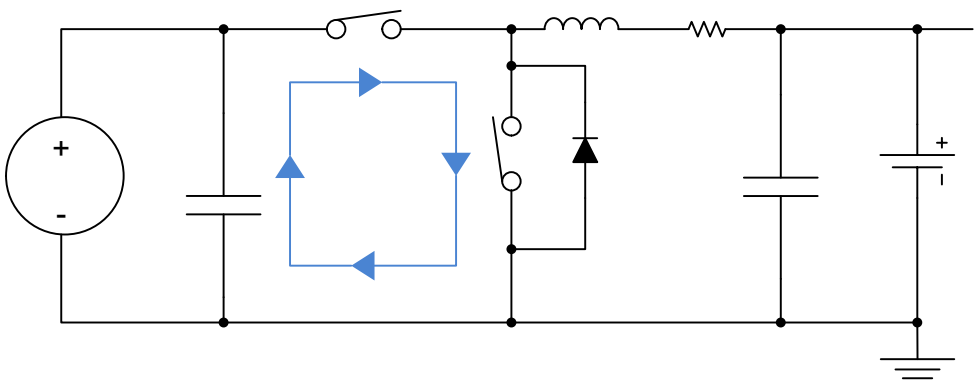
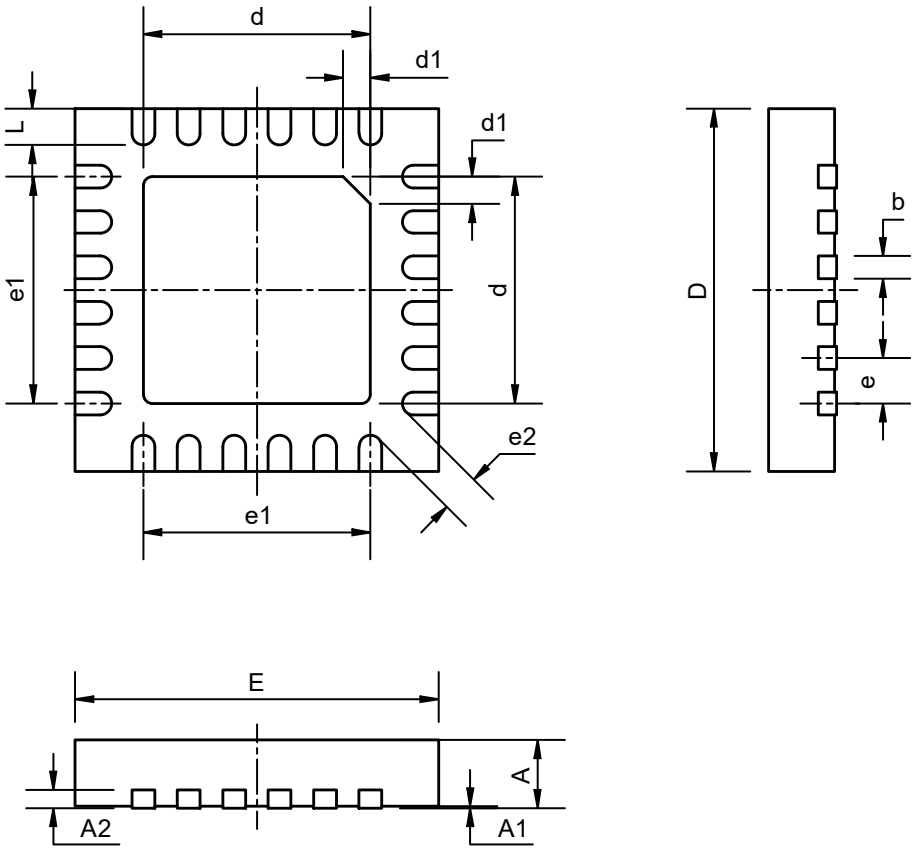


Figure 18. High Frequency Current Path

PACKAGE OUTLINE DIMENSIONS

WQFN24(4.00 mm x 4.00 mm)



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.18	0.20	0.25
b	0.18	0.25	0.30
D	3.90	4.00	4.10
d	2.60	2.70	2.80
d1	0.30	0.35	0.40
E	3.90	4.00	4.10
e	0.50 BSC		
e1	2.50 BSC		
e2	0.40	0.45	0.50
L	0.35	0.40	0.45

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-07-23	Official Version	Wang hao	Xia Yong Jie	Liu Jia Ying
1.1	2025-09-18	Update REG02 default value	Wang hao	Xia Yong Jie	Liu Jia Ying