100V Input, 3.5A Current Limit, Asynchronous

Step-down Converter

General Description

The ET8A35A1KP is a high voltage, high performance asynchronous step-down converter operates over a wide range input voltage 9V to 100V. The ET8A10AXKP integrates a 100V 100mΩ high-side MOSFET.

The ET8A35A1KP operates with fixed frequency peak current control with built-in compensation eliminates the need for external components. Cycle-by-cycle current limit in high-side MOSFET protects the converter in an overload condition. Hiccup mode protection is triggered if the over-current condition has persisted for longer than the present time.

The ET8A35A1KP is available in an ESOP8 package.

Features

- 9V to 100V Input Voltage Range
- 3.5A Current Limit
- 96% Peak Efficiency
- 500µA Operating Quiescent Current
- 9µA Shutdown Current
- 100V/100mΩ High-Side MOSFET
- Peak Current Mode Control
- 150kHz Fixed Frequency
- Internal Compensation for Ease of Use
- Up to 91% Duty Cycle
- 0.8V Voltage Reference
- Short Circuit Protection Function
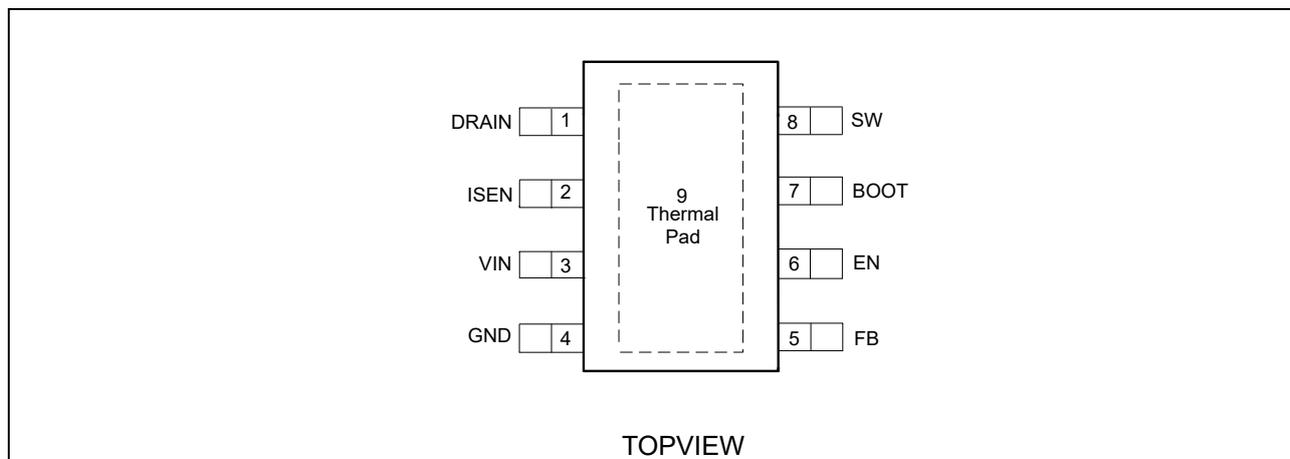- Thermal Shutdown Function
- Package:

Part No.	Package	Body Size	Packing Option
ET8A35A1KP	ESOP8	4.9mm×6.0mm	4000pcs/reel

Applications

- Charger in Vehicle
- Battery Chargers
- Power Adapter

ET8A35A1KP

Pin Configuration

TOPVIEW

Pin Function

Pin No.	Pin Name	Pin Function
1	DRAIN	Internal NMOS drain. This pin is connected to the drain of the internal upper NMOS.
2	ISEN	Current detection pin. Connect a thin wire between the ISEN and DRAIN pins, and place a filtering capacitor between this pin and GND. It is recommended to use a capacitance of 1uF.
3	VIN	Input supply. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
4	GND	Ground. GND should be placed as close to the output capacitor as possible to avoid the high-current switch paths. Connect the exposed pad to GND plane for optimal thermal performance.
5	FB	Feedback. Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.
6	EN	Enable input. Pull EN below the specified threshold to shut down the ET8A35A1KP. Pull EN above the specified threshold to enable the ET8A35A1KP.The EN pin must not be left floating.
7	BOOT	Bootstrap. Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when SW voltage is low.
8	SW	Switch node. SW is the output from the high-side switch. A low forward voltage schottky rectifier to ground is required. The rectifier must be placed close to SW to reduce switching spikes.
9	Thermal Pad	Heat dissipation path of die. Electrically connection to DRVIN pin for proper operation and optimized thermal performance.

ET8A35A1KP

Block Diagram
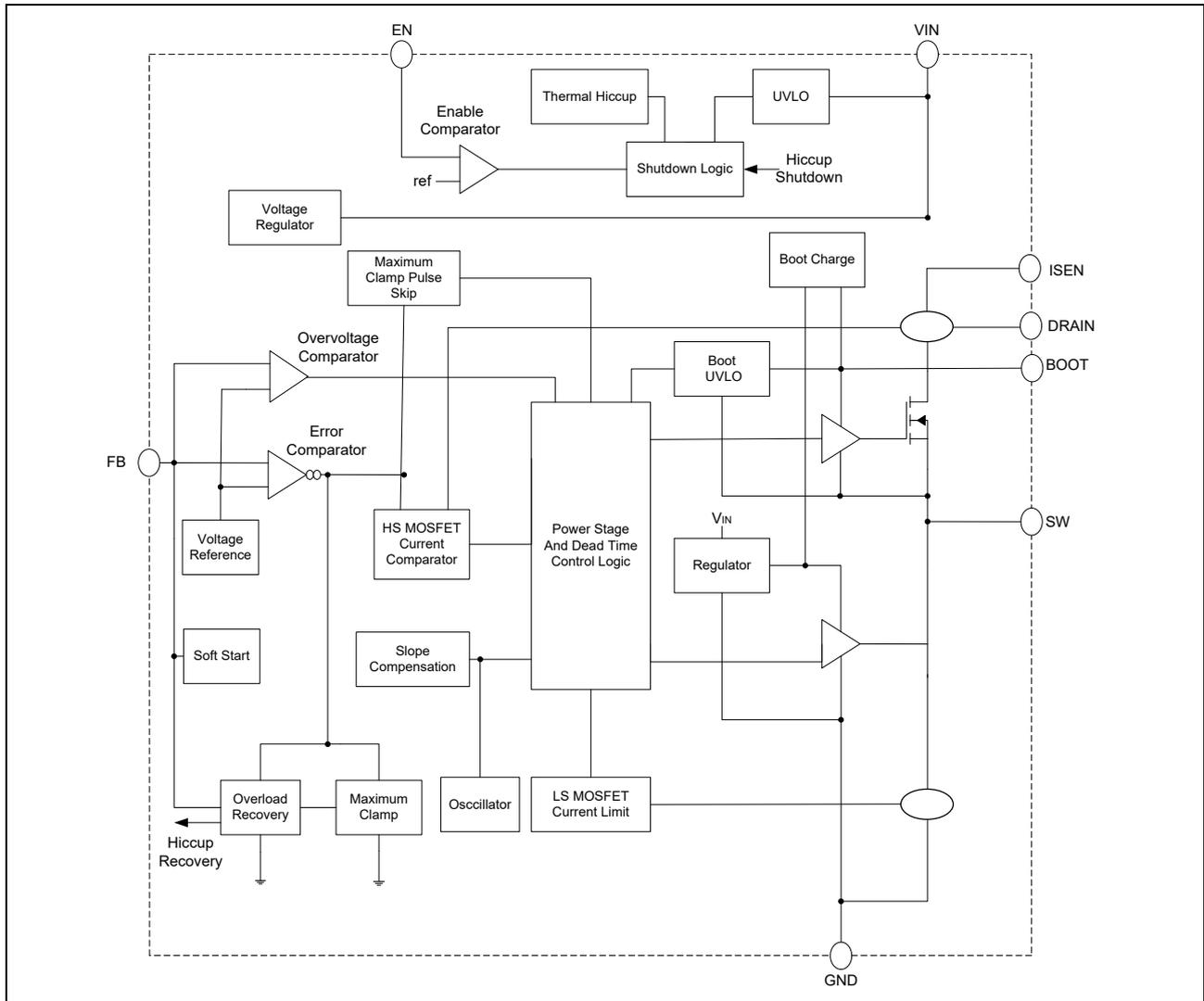
Absolute Maximum Ratings

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Symbol	Parameters	Min	Max	Unit
$V_{SW}, V_{EN}, V_{IN},$ $V_{ISEN}, V_{DRAIN},$	DRAIN,SW,EN,VIN,ISEN to GND Voltage Range	-0.3	110	V
$V_{FB},$	FB to GND Voltage Range	-0.3	7	V
V_{BOOT}	BOOT to GND Voltage Range	-0.3	110	V
	BOOT to SW Voltage Range	-0.3	5.5	V
T_{STG}	Storage Junction Temperature	-55	150	°C
V_{ESD}	HBM	-2	2	KV

ET8A35A1KP

Electrical Characteristics

(V_{IN}=48V, V_{OUT}=5V, Typical values are at. T_A=25°C unless otherwise noted)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Supply Voltage						
V_{IN}	Input Voltage		9	-	100	V
V_{IN_UVLO}	UVLO	V_{EN}=5V, V_{IN} Rising		8		V
$V_{UVLO(HYS)}$	UVLO Hysteresis	V_{EN}=5V, V_{IN} Rising		0.3		V
I_{SHDN}	Shutdown Supply Current	V_{EN}=0V, No Load		9		uA
I_Q	Input Quiescent Current	V_{FB}=1V		500		uA
Enable						
V_{EN}	Enable Threshold Voltage		-	2.2	-	V
V_{EN_UVLO}	Enable Threshold voltage Hysteresis		-	0.2	-	V
V_{EN_MAX}	EN Pin Voltage		100	-	-	V
FB Reference Voltage						
V_{FB}	FB Reference Threshold		-	0.8	-	V
$V_{FB（short）}$	Feedback Short Voltage		-	0.1	-	V
V_{FB2}	Feedback Short Voltage Hysteresis		-	0.12	-	V
Switching Frequency						
F	Switching Frequency	I_{OUT}=500mA	-	150	-	kHz
D_{MAX}	Maximum Duty Cycle	V_{IN}=12V	-	91	-	%
Peak Current Threshold Voltage						
V_{SEN}			-	120	-	mV
Thermal Shutdown						
T_{SD}	Thermal Shutdown Temp		-	130	-	°C
T_{SH}	Thermal Shutdown Temp Hysteresis		-	20	-	°C

Typical Characteristics

(At T_A=25ºC, V_{IN}=48V, V_{OUT}=12V, Unless Otherwise Noted)
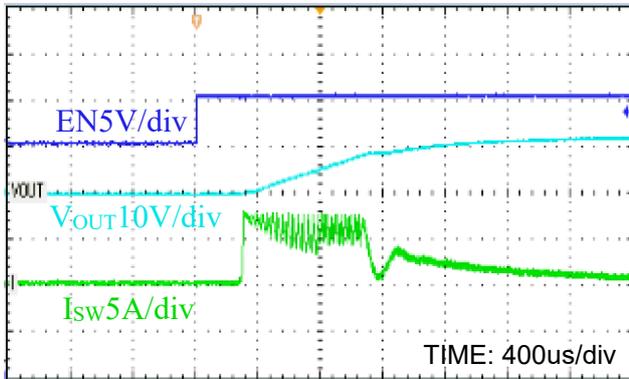
V_{IN}=48V EN=5V I_{OUT}=1A

Figure 1. EN Start up
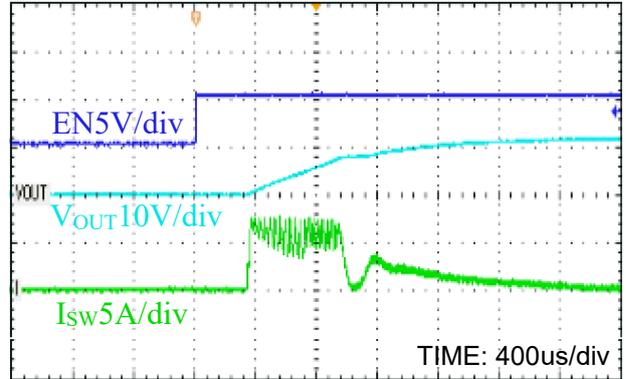
V_{IN}=48V EN=5V I_{OUT}=0A

Figure 2. EN Start up
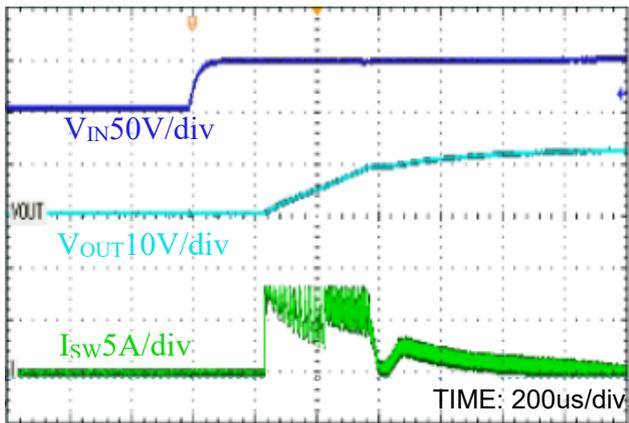
V_{IN}=48V I_{OUT}=0A

Figure 3. No load V_{IN} Start up
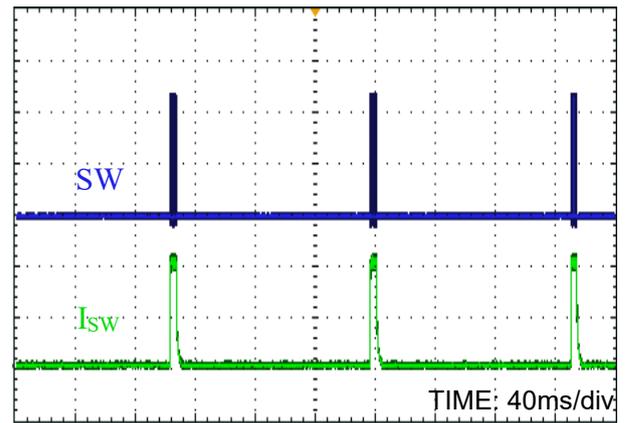
V_{IN}=48V

Figure 4. Short Circuit
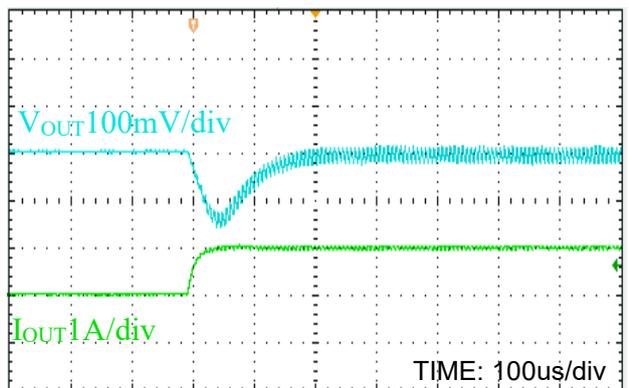
I_{OUT}=10mA~1A V_{IN}=48V

Figure 5. Load Transient
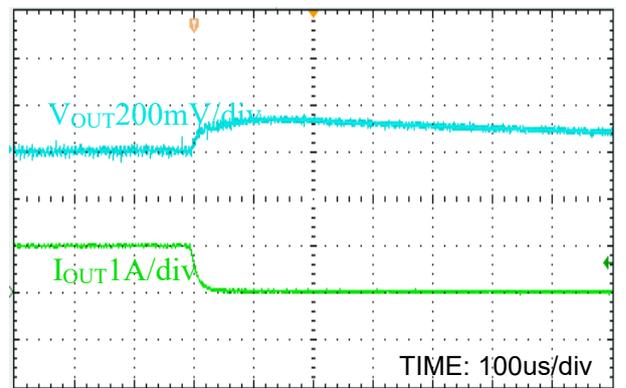
I_{OUT}=1A~10mA V_{IN}=48V

Figure 6. Load Transient

ET8A35A1KP

Application Circuits

Figure 7. Application Circuit 12V output with programmable UVLO

ID	Parameters	Type	Part Number	Vendor
U1		ESOP8	ET8A35A1KP	ETEK
C1	47uF	Capacitor,47uF,100V,20%,SMD	VP2A470M0810	HONOR
C3	10uF	Capacitor,10uF,10V,20%,0603	CL10A106MP8NNNC	SAMSUNG
C2	1uF	Capacitor,1uF,100V,10%,0805	CGA0805X7R105K101MT	HRE
C4	0.1uF	Capacitor,0.1uF,50V,10%,0603	CL10B104KB8NNNC	SAMSUNG
C8	100pF	Capacitor,100pF,50V,10%,0603	CC0603KRX7R9BB101	YAGEO
C6	330uF	Capacitor,330uF,25V,20%,SMD	GVT1V331M0810	HONOR
C7	10uF	Capacitor,10uF,25V,10%,0805	CL21A106KAYNNNE	SAMSUNG
C5	470pF	Capacitor,470pF,100V,10%,0805	FCC0805B471K101DT	FOJAN
R2	100K	Resistor,100K,1%,0603	RC0603FR-07100KL	YAGEO
R3	10K	Resistor,10K,1%,0603	RT0603BRD0710KL	YAGEO
R1	R035	Resistor,R035,5%, 1206 Alloy Resistor	LRAN12CFTR035	NCT
R5	43K	Resistor,43K,1%,0603	RC0603FR-0743KL	YAGEO
R6	3K	Resistor,3K,1%,0603	RC0603FR-073KL	YAGEO
R4	10R	Resistor,10R,5%,1206	RC1206JR-7W10RL	YAGEO
D1	3A	Diode,3A,100V	SS310FL	GOODWORK
L1	47uH	Inductance,47uH,3A	MWSA1004S-470MT	SUNLORD

Design Parameters	Example Value
Input Voltage	48V
Output Voltage	12V
Maximum Output Current	3.5A
Switching Frequency	150kHz
Start Input Voltage (Rising VIN)	24V
Stop Input Voltage (Falling VIN)	22V

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Application Circuits(Continued)
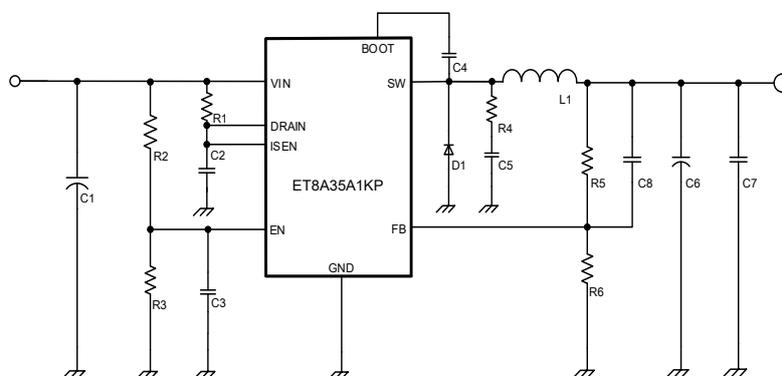
Figure 8. Application Circuit 5V output with programmable UVLO

ID	Parameters	Type	Part Number	Vendor
U1		ESOP8	ET8A35A1KP	ETEK
C1	47uF	Capacitor,47uF,100V,20%,SMD	VP2A470M0810	HONOR
C3	10uF	Capacitor,10uF,10V,20%,0603	CL10A106MP8NNNC	SAMSUNG
C2	1uF	Capacitor,1uF,100V,10%,0805	CGA0805X7R105K101MT	HRE
C4	0.1uF	Capacitor,0.1uF,50V,10%,0603	CL10B104KB8NNNC	SAMSUNG
C8	100pF	Capacitor,100pF,50V,10%,0603	CC0603KRX7R9BB101	YAGEO
C6	330uF	Capacitor,330uF,25V,20%,SMD	GVT1V331M0810	HONOR
C7	10uF	Capacitor,10uF,25V,10%,0805	CL21A106KAYNNNE	SAMSUNG
C5	470pF	Capacitor,470pF,100V,10%,0805	FCC0805B471K101DT	FOJAN
R2	100K	Resistor,100K,1%,0603	RC0603FR-07100KL	YAGEO
R3	10K	Resistor,10K,1%,0603	RT0603BRD0710KL	YAGEO
R1	R035	Resistor,R035,5%, 1206 Alloy Resistor	LRAN12CFTR035	NCT
R5	16K	Resistor,16K,1%,0603	RC0603FR-0716KL	YAGEO
R6	3K	Resistor,3K,1%,0603	RC0603FR-073KL	YAGEO
R4	10R	Resistor,10R,5%,1206	RC1206JR-7W10RL	YAGEO
D1	3A	Diode,3A,100V	SS310FL	GOODWORK
L1	47uH	Inductance,47uH,3A	MWSA1004S-470MT	SUNLORD

Design Parameters	Example Value
Input Voltage	48V
Output Voltage	5V
Maximum Output Current	3.5A
Switching Frequency	150kHz
Start Input Voltage (Rising VIN)	24V
Stop Input Voltage (Falling VIN)	22V

Overview

ET8A35A1KP is a high-voltage asynchronous buck chip with an input voltage of 9V to 100V. ET8A35A1KP can provide a peak current of 3.5A power transistor, with a peak efficiency of up to 96%. ET8A35A1KP adopts a fixed frequency peak current control mode and a built-in loop compensation circuit, which solves the problem of excessive external compensation components.

Over-Current Protection

The ET8A35A1KP implements current-mode control which uses the internal COMP voltage to control the turn on and the turnoff of the high-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared. When the peak switch current intersects the current reference the SW switch turns off.
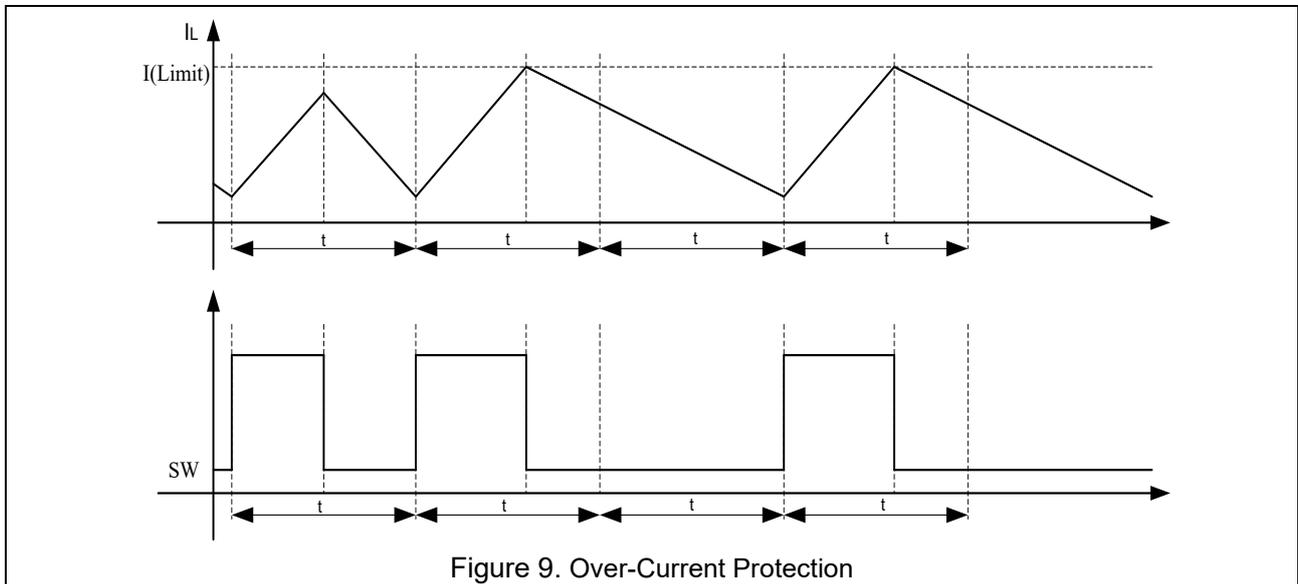
Figure 9. Over-Current Protection

Short Circuit Protection

The ET8A35A1KP has a short-circuit protection function. When the chip detects a short circuit at the output terminal, the system automatically lowers its frequency to 32kHz.

Output Voltage

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R5 resistance is 3KΩ. Use Equation 1 to calculate R5, V_{REF}=0.8V.

$$R5 = (\frac{V_{OUT}}{V_{REF}} - 1) \times R6 \tag{1}$$

Under Voltage Lock-Out

An external voltage divider network of R2 from the input to EN pin and R3 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold, V_{EN}=2.2V. Use Equation 2 to calculate.

$$R2 = (\frac{V_{UVLO}}{V_{EN}} - 1) \times R3 \tag{2}$$

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current. The peak-to-peak ripple current in the inductor ILPP can be calculated as in Equation 3.

$$I_{LPP} = \frac{V_{OUT} - (V_{IN} - V_{OUT})}{V_{IN} \times L \times F_{SW}} \tag{3}$$

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- F_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage is always used to calculate the minimum inductance required. Use Equation 4 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{F_{SW} \times LIR \times I_{OUT(MAX)}} \times (1 - \frac{V_{OUT}}{V_{IN(MAX)}}) \tag{4}$$

- L_{MIN} is the minimum inductance required
- F_{SW} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting inductor, choose its rated current especially the saturation current larger than peak current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 5 and Equation 6.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \tag{5}$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times (I_{LPP})^2} \tag{6}$$

- I_{LPEAK} is the inductor peak current

- I_{OUT} is the DC load current

- I_{LPP} is the inductor peak-to-peak current

- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of device which is typically 4A. The most conservative approach is to choose an inductor with saturation current greater than 4A. Because of the maximum I_{LPEAK} limited by device, maximum output current that can deliver depends on inductor current ripple. Thus, maximum desired output current affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to lower maximum output current.

Diode Selection

Requires an external catch diode between the SW pin and GND. The selected diode must have are verse voltage rating equal to or greater than VIN (max). The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 100V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the ET8A35A1KP.

For the example design, the SS310 Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the SS310FL is 0.67 volts at 3A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch.

The off-time of the internal switch is a function of the maximum input-voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g.1uF) with small package size (0805) to filter high frequency switching noise. Place the small size cap to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must have a ripple current rating greater than the maximum input current ripple. Use Equation 7 and Equation 8 and Equation 9 to calculate.

$$I_{CINRMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \tag{7}$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$I_{CINRMS} = 0.5 \times I_{OUT}$$ (8)

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$ (9)

- F_{SW} is the switching frequency
- C_{IN} is Input capacitor

Bootstrap Capacitor Selection

A 0.1F ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. Capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance. The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 10 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{8 \times F_{SW}^2 \times L \times C_{OUT} \times V_{IN}}$$ (10)

- $\triangle V_{OUT}$ is the output voltage ripple
- F_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Layout

Proper PCB layout is a critical for ET8A35A1KP stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Schottky diodes should be placed as close as possible to the SW pin and GND to minimize parasitic effects.

2. The pull-down feedback resistor loop at the FB pin end needs to be as small as possible.

3. The BOOT capacitor should be as close as possible to the BOOT and SW pins.

4. Connect the positive terminal of the ISEN pin capacitor to the ISEN pin with a thin wire.

5. The negative terminal of the ISEN pin capacitor is connected to the negative terminal of the output electrolytic capacitor through perforation.

6. If the output voltage is greater than 12V, it is recommended to add an RC absorption circuit to the SW pin, and a 1nF capacitor in a 51Ω series is recommended.

7. If the feedback resistor on FB is far away from the output capacitor, an output small patch capacitor filter can be added near the resistor as shown in C9 in Figure 10.
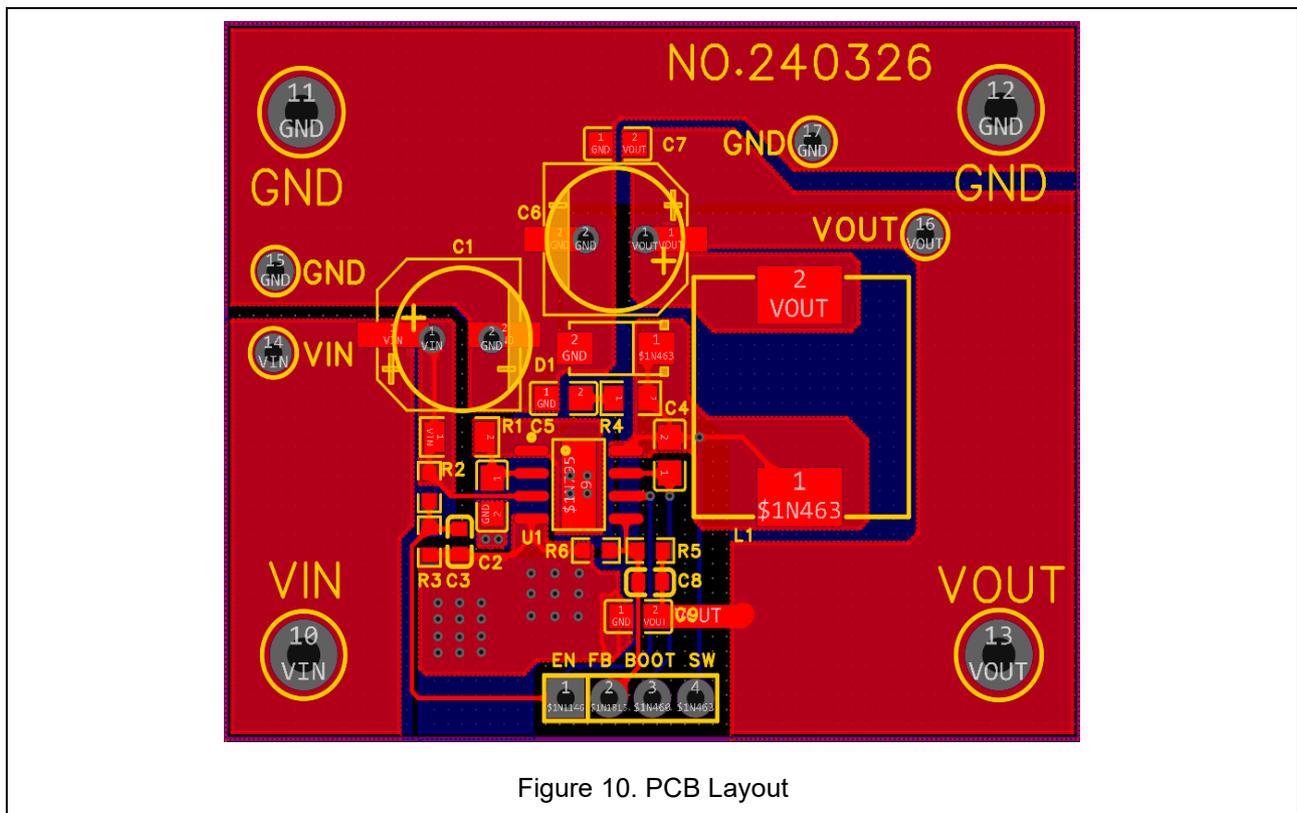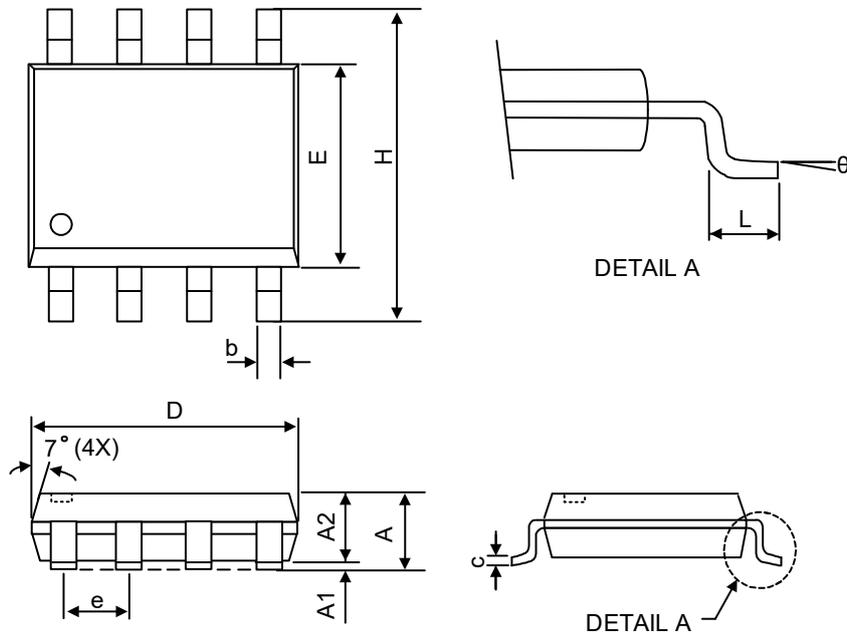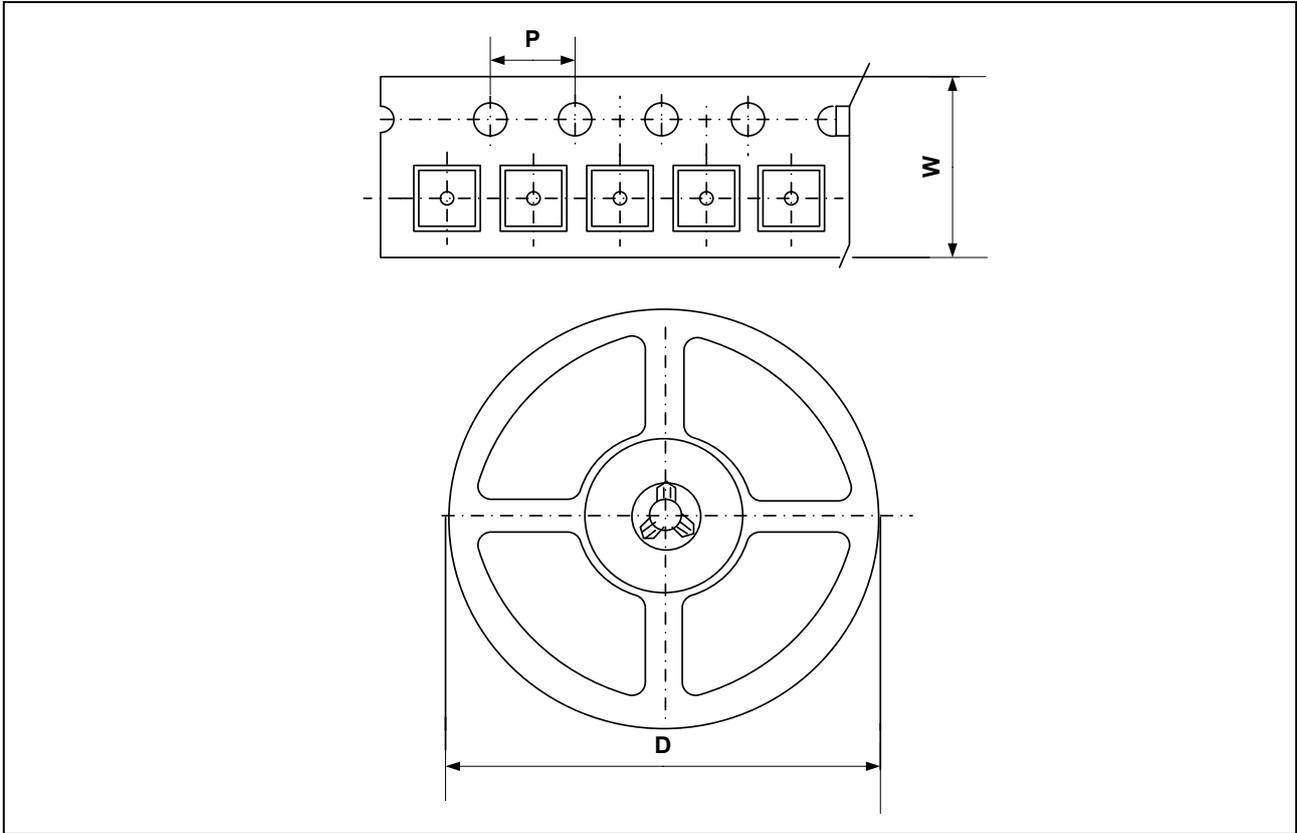

Figure 10. PCB Layout

Package Dimension

ESOP8

Symbol	Unit:mm		
	Min	Typ	Max
A	1.35	-	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.55
b	0.31	0.41	0.51
c	0.10	-	0.25
D	4.70	4.90	5.10
E	3.70	3.90	4.10
H	5.80	6.00	6.20
e	1.27BSC		
L	0.40	-	1.27
θ	0°	-	8°

ET8A35A1KP

Packing Information

Type	W(mm)	P(mm)	D(mm)	Qty (pcs)
ESOP8	12.0mm	4.0mm	330mm	4000pcs

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function& Spec Checking	Package& Tape Checking
1.0	2025-12-29	Initial Version	Caojiachen	Wuhesong	Liujiaying