24V, 3A, 650kHz, Synchronous Step-Down Converter with PG, SS, and Forced CCM

General Description

The ET81315 is a fully integrated high frequency, wide input voltage, 3A output synchronous buck convertor and uses synchronous mode operation for higher efficiency over the output current load range.

This convertor adopts adaptive constant-on-time (ACOT) structure, and provides a fast transient response. It also supports both low-equivalent series resistance (ESR) output capacitors and ultra-low ESR ceramic capacitors with no external compensation components.

The device has the full protection features, include the short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The ET81315 requires a minimal number of readily available, standard, external components and SOT-583 package is available.

Features

- 3A Converters Integrated 75mΩ and 40mΩ FET
- ACOT mode control with fast Load transient response
- Input Voltage Range: 4.2V to 24V
- FB voltage is 0.805V (TYP)
- Output Voltage Range:V_{FBTH} to 13V
- 200μA Low IQ with no Switch
- High-Efficiency Synchronous Mode Operation
- Forced PWM Operation(FCCM)
- 650kHz Switching Frequency
- Programmable Soft-Start Time
- Power Good (PG) Indication
- Start-up from Pre-Biased Output Voltage
- Cycle-by-Cycle Over-current Limit
- Hiccup-mode Over-current Protection
- Non-Latch UVP and TSD Protections
- Part No. and Package

Part No.	Package	Packing Option	MSL
ET81315	SOT-583 (2.1mm ×1.6mm)	Tape and Reel , 3K/Reel	3

Application

- Game Consoles
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- General Purposes

Pin Configuration

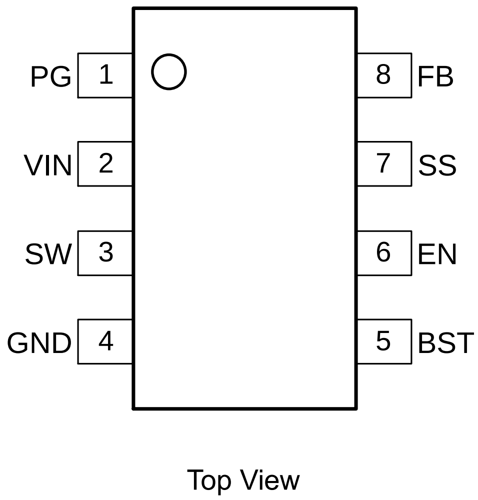

Figure 1. Pin Configuration

Pin Function

Pin Name	Pin No.	I/O	Description
PG	1	I	Power good output. The output of PG is an open drain.
VIN	2	I	Input voltage supply pin, also the drain terminal of high-side power NFET.
SW	3	O	Switch node connection between low-side NFET and high-side NFET.
GND	4	-	Ground pin of controller circuit, as well as source terminal of low-side power NFET. Connect sensitive VFB to this GND at a single point.
BST	5	O	Power supply of high-side NFET control circuit. Connect 1μF capacitor between VBST and SW pins.
EN	6	I	Enable pin. Must be pulled up to enable the device.
SS	7	O	Connect an external capacitor to SS program the soft-start time for the switch mode regulator.
FB	8	I	Output voltage feedback pin. Connect to output voltage with feedback resistor divider.

Block Diagram

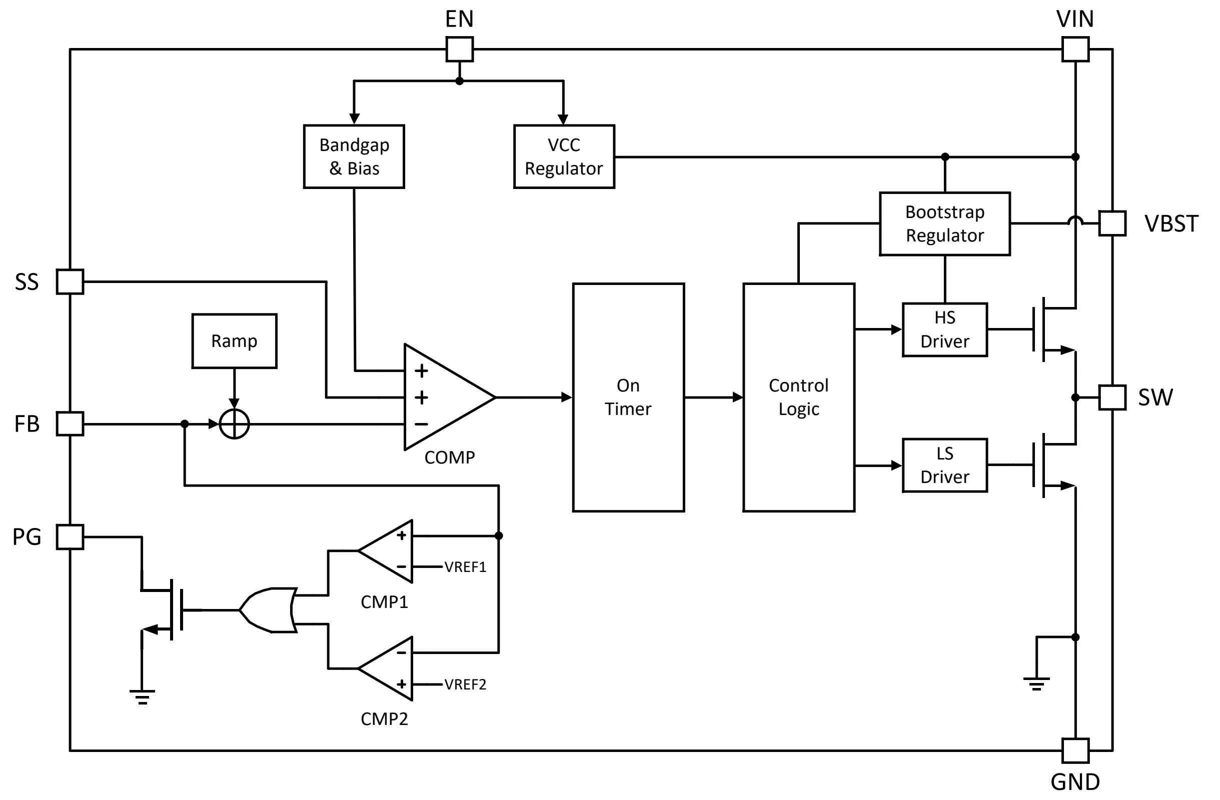

Figure 2. Block Diagram

Functional Description

Overview

The ET81315 is highly integrated, 3A synchronous Buck convertor. It employs adaptive constant on time (ACOT) mode, and supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of this device can reduce the output capacitance.

Adaptive Constant-On-Time Control

The main control mode of ET81315 is pulse width modulation (PWM) with ACOT structure. This control mode control can achieve pseudo-fixed frequency and stable operation with both low-ESR and ceramic output capacitors.

The high-side MOSFET is turned on at the beginning of each cycle. When one shot timer expires, the high-side power FET is turned off. This one shot duration is set proportional to input voltage, VIN, and inversely proportional to the output voltage, VO, to achieve pseudo-fixed frequency over the input voltage range, hence it is called adaptive constant on-time control. The one-shot timer is reset and the high-side power FET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is generated to emulate output ripple, eliminating the need for ESR of output capacitor.

FPWM Operation

The ET81315 operates in forced continuous conduction mode (CCM). In FPWM mode, the ET81315 keeps the switching frequency constant at light load condition. When the load current decreases, the high-side switch is not turned off even if the current of the high-side switch goes negative to keep the frequency constant. The output ripple is greatly reduced at light load compare with the PFM mode.

The ZCD threshold changes to positive with a typical -1.3A current limit which is named negative current limit (NOCL). When the inductor current hits the NOCL, the low side FET is turned off immediately and the high-side MOSFET is forced turning on after the dead time. In the next switching cycle, the inductor current ramps up again and then ramp down the same as the beginning.

Under-Voltage Lockout (UVLO)

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When input voltage increases up to the upper threshold of UVLO, it begins to switch.

Soft Start (SS)

The ET81315 features an external soft-start pin for programmable output voltage ramp-up time. The soft-start function prevents inrush current from affecting the ET81315 and its load during initial power-up. The soft-start time can be set by connecting an external capacitor, C_{SS}, between the SS pin and GND. An internal current source (typically I_{SS} = 8.0μA) charges C_{SS}, generating a ramp from 0V to $2V_{REF}$. The soft-start time can be calculated using Equation 1:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times 8.0\mu A}{2V_{REF}} \qquad (1)$$

Current Protectiona and Short-Circuit Protection (SCP)

The ET81315 over-current limit (OCL) is implemented by using cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET drain to source voltage during its on-state.

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During the on-state of high-side FET, the switch current increases at a linear rate determined by VIN, VOUT, and the inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current IOUT. If the monitored current is above the OCL level, the convertor keeps low-side FET on and prevents the creation of a new set pulse, even the voltage feedback loop requires one, until the current level decreases to OCL level or lower. In next switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the load current is higher than the current available from the convertor. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time and re-start after the hiccup time (typically 10ms).When the over current condition is removed, the output voltage returns to the regulated value.

Power Good (PG)

Power good (PG) indicates whether the output voltage is in the normal range or not compared to the internal reference voltage. PG is an open-drain structure and requires an external pull-up supply. During power-up, the power good output is pulled low. This indicates to the system to remain off and keep the load on the output to a minimum. This helps reduce inrush current during start-up.

The PG detection is triggered and PG pin floats after a 50us deglitch time. A pull-up resistor of 100kΩ is recommended.

When the soft start is finished, the output voltage is lower than 87% and higher than 120% of the internal reference voltage, the power good signal is pulled low.

When the soft start is finished, the output voltage is higher than 92% and lower than 107% of the internal reference voltage, the power good signal is pulled high.

The PG output is pulled low when EN is low, VIN is low, or OCP or over-temperature protection (OTP) is triggered.

Pre-Bias Start-Up

The ET81315 is designed with an internal soft-start. When the VIN is plugged in and the EN pin becomes high, the reference voltage of PWM comparator begins to rise from zero.

If the output capacitor is pre-biased at start-up, the device begins to switch and start ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme ensures that the converters ramp up smoothly into regulation point.

Thermal Shutdown

The device monitors the temperature of itself. If temperature exceeds the threshold value (typically 150°C), the device is shut off. When the temperature falls to about 130°C or below, the converter begins to switch.

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, VIN low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path initially to avoid any fault triggering. The internal supply rail is then pulled down.

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameters	Min	Max	Unit
V_{INPUT}	VIN Supply Voltage	-0.3	26	V
	SW Pin Switch Voltage (V_{SW})	-0.3	26	V
	SW Pin Voltage (10ns transient)	-6.5	28	V
	SW Pin Voltage (2us transient)	-0.6	26	V
	BST Pin Voltage		V_{SW}+5	V
	EN Pin Voltage	-0.3	26	V
	PG,SS,FB Pin Voltage	-0.3	4	V
V_{ESD}	Human Body Model (JEDEC JS-001)		±2000	V
	Charged Device Model (JEDEC JS-002)		±500	V
T_J	Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature	-65	+150	°C
T_L	Lead Temperature (Soldering, 10 sec)		+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameters	Min	Max	Unit
V_{IN}	Supply Voltage	4.2	24	V
V_{OUT}	Output Voltage	0.805	13	
T_J	Operating Junction Temperature	-40	125	°C
T_A	Ambient Temperature	-40	85	°C

Thermal Properties

Symbol	Parameters	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	60	°C/W

Electrical Characteristics

V_{IN} = 12V, T_J = -40°C to +125°C , typical value is tested at T_J = +25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{SHDN}	Supply current (shutdown)	V_{EN} = 0V			10	μA
I_Q	Supply current (quiescent)	V_{EN} = 2V, V_{FB} = 0.85V		200		μA
$R_{DS(ON)\_HS}$	HS switch on resistance	V_{BST-SW} = 3.3V		75		mΩ
$R_{DS(ON)\_LS}$	LS switch on resistance			40		mΩ
$I_{LIMIT\_LS\_OC}$	Low-side switching current limit OCP		2.8	4		A
I_{NC}	Negative current limit[(1)]	V_{OUT} = 3.3V, L = 1.5μH		-1.3		A
f_{SW}	Oscillator frequency	In CCM	485	650	815	kHz
t_{ON_MIN}	Minimum on time[(1)]			45		ns
t_{OFF_MIN}	Minimum off time[(1)]			190		ns
V_{REF}	Feedback voltage		789	805	821	mV
I_{FB}	Feedback current			10	80	nA
D_{Hiccup}	Hiccup duty cycle			12.5		%
V_{EN_RISING}	EN rising threshold		1.16	1.23	1.29	V
V_{EN_HYS}	EN hysteresis			100		mV
I_{EN}	EN input current	V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
V_{UVLO_RISE}	VIN under-voltage lockout threshold rising			4		V
V_{UVLO_HYS}	VIN under-voltage lockout threshold hysteresis			400		mV
PG_{UV_R}	Power good rising threshold UV		87	92	97	%V_{REF}
PG_{UV_F}	Power good falling threshold UV		82	87	92	%V_{REF}
PG_{OV_R}	Power good rising threshold OV		115	120	125	%V_{REF}
PG_{OV_F}	Power good falling threshold OV		102	107	112	%V_{REF}
$t_{PG\_Rise\_Delay}$	Power good rising delay			55		μs
$t_{PG\_Fall\_Delay}$	Power good falling delay			45		μs
V_{PG}	Power good sink current capability	PG is Low,Sink 1mA		0.13	0.4	V
I_{PG_LEK}	Power good leakage current	PG is Hi-Z			3	μA
I_{SS}	Soft-start current		5.6	8	10.4	μA
T_{SD}	Thermal shutdown[(1)]			150		°C
T_{HYS}	Thermal hysteresis[(1)]			20		°C

Note 1: Not production tested, design assurance.

Application and Implementation

Setting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. ETEK recommends using 1% tolerance or better divider resistors. Start by using Equation 2 to calculate VOUT.

If customers want to improve efficiency at very light loads,we recommend using larger value resistors. High value of resistor will be more susceptible to noise and voltage errors from the FB input current will be more noticeable.

$$V_{OUT} = 0.805 \times (1 + \frac{R1}{R2}) \quad (2)$$

The feedback circuit is shown in Figure 3.

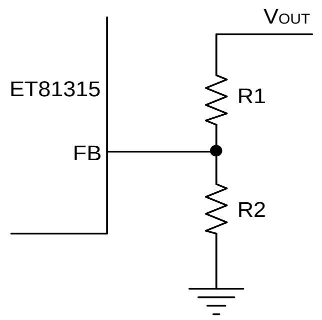


Figure 3: Feedback Network

Table 1 list the recommended parameters for common output voltages.

Table 1: Parameter Selection for Common Output Voltages, V_{IN} = 13V

V_{OUT} (V)	R1(kΩ)	R2 (kΩ)	C_{IN}(μF)	C_{OUT}(μF)	L1 (μH)
1.0	33	133	22	22×2	1.5
1.2	40.2	82	22	22×2	1.5
1.5	40.2	46.3	22	22×2	2.2
1.8	40.2	32.4	22	22×2	2.2
2.5	40.2	19.1	22	22×2	3.3
3.3	40.2	13	22	22×2	3.3
5.0	40.2	7.68	22	22×2	4.7

Selecting the Inductor

The inductor provides a constant current to the output load. Its inductance value directly affects DC-DC conversion efficiency, output voltage ripple, and other key performance metrics. The inductor ripple current is typically allowed to be 30% to 60% of the maximum load current. It is also recommended to choose an inductor with a higher saturation current to ensure system stability under varying temperature conditions.

The inductance value can be calculated using the following Equation 3:

$$L = \frac{V_{OUT}}{F_{SW} \times K \times I_{OUT\_MAX}} \times (1 - \frac{V_{OUT}}{V_{IN}}) = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated with Equation4:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

- K=Ratio of inductor ripple current to maximum output current (recommended between 20% and 40%)
- I_{OUT_MAX}=Maximum load current

△I_L=Inductor ripple current

Selecting the Input Capacitor

It is recommended to use 22uF×2 /35V MLCC capacitors as decoupling capacitors for the ET81315 input. Additionally, a 0.1uF MLCC capacitor should be connected in parallel between VIN and GND for high-frequency filtering.Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The RMS current for the C_{IN} capacitor can be calculated using the Equation 5:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The ripple current of the input capacitor can be calculated using the Equation 6:

$$C_{IN} = \frac{I_{OUT}}{F_{SW} \times \Delta V_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Selecting the Output Capacitor

The value of the output capacitor directly affects the stability of the ET81315 system and the magnitude of the output voltage ripple. Additionally, the effective performance of the capacitor depends on multiple parameters, such as dielectric material, package size, voltage rating, temperature, and output voltage. It is recommended to use high-voltage-rated, large-package X7R capacitors as the output capacitor.

The output voltage ripple can be calculated using the Equation 7:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (7)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance.

For simplification, the output voltage ripple can be estimated with Equation 8:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

The output voltage ripple caused by the ESR is very small. In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation9:

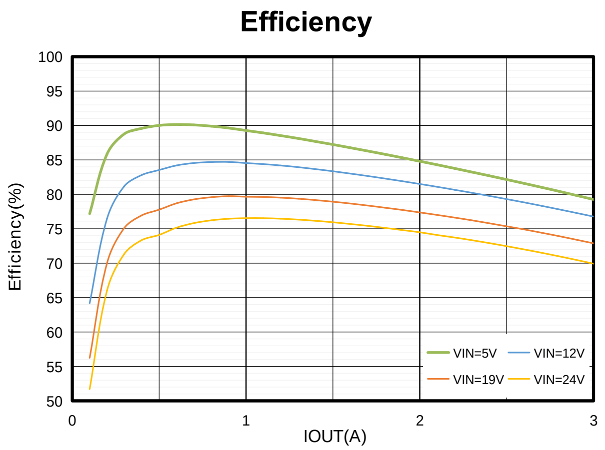
$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

Choose a larger output capacitor for a better load transient response, but be sure to consider the maximum output capacitor limitation in the design application. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time and will fail to regulate.

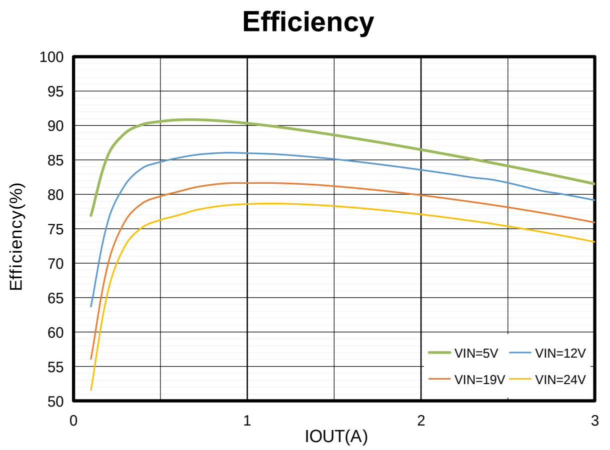
- L=Inductance Value
- R_{ESR}=Equivalent Series Resistance of the Inductor

Application Curves

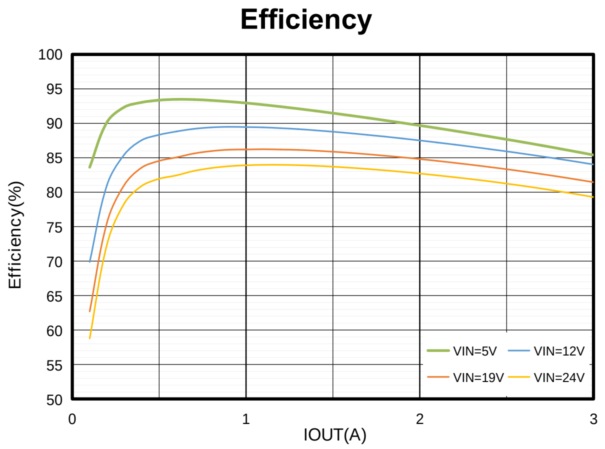
V_{IN} = 19V, F_{SW} = 650kHz, T_A = +25°C (unless otherwise noted).



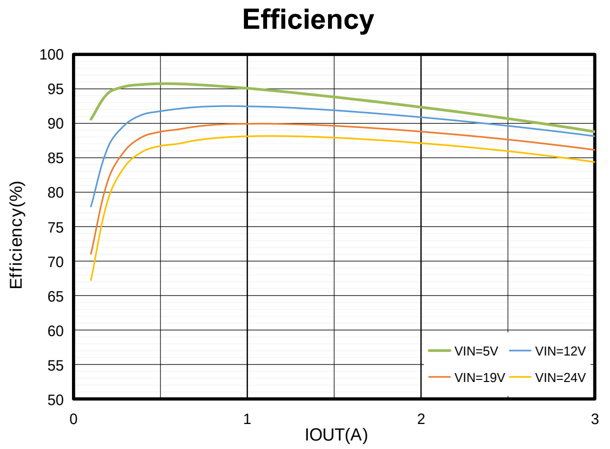
V_{OUT}=1V, L=1.5μH, DCR=7mΩ



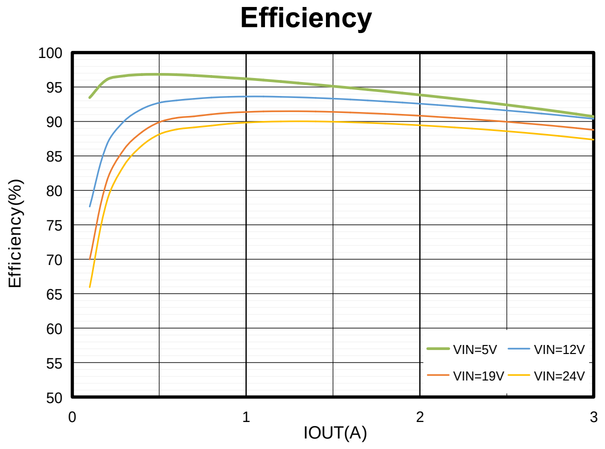
V_{OUT}=1.2V, L=1.5μH, DCR=7mΩ



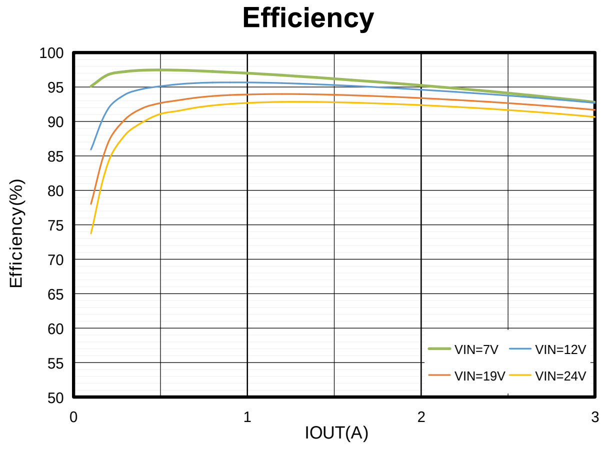
V_{OUT}=1.8V, L=2.2μH, DCR=15mΩ



V_{OUT}=2.5V, L=3.3μH, DCR=11.8mΩ



V_{OUT}=3.3V, L=3.3μH, DCR=11.8mΩ

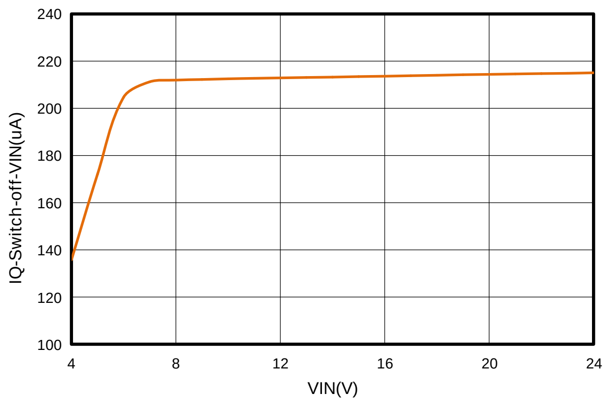


V_{OUT}=5.0V, L=4.7μH, DCR=20mΩ

Application Curves(Continued)

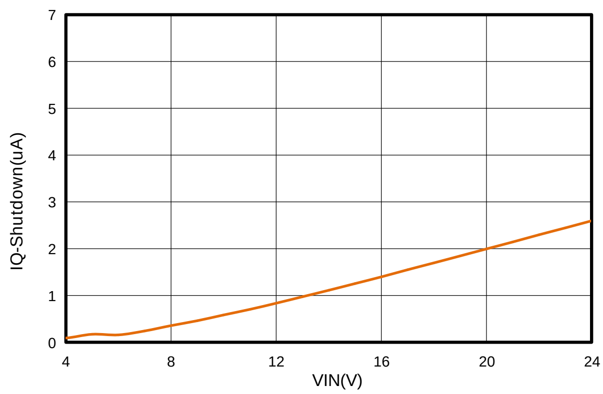
V_{IN} = 19V, F_{SW} = 650kHz, T_A = +25°C (unless otherwise noted).

Supply Current vs. Input Voltage



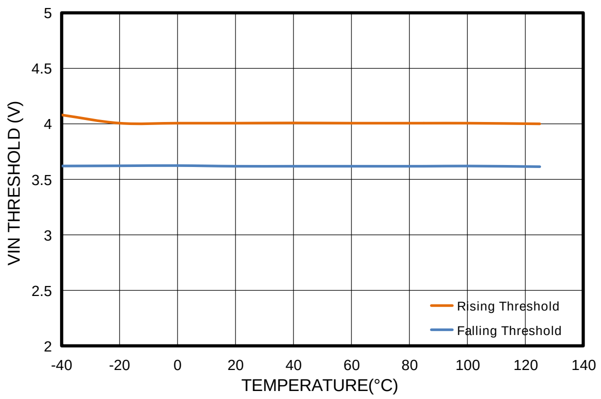
V_{EN}=2V, V_{FB}=0.85V

Disabled Supply Current vs. Input Voltage

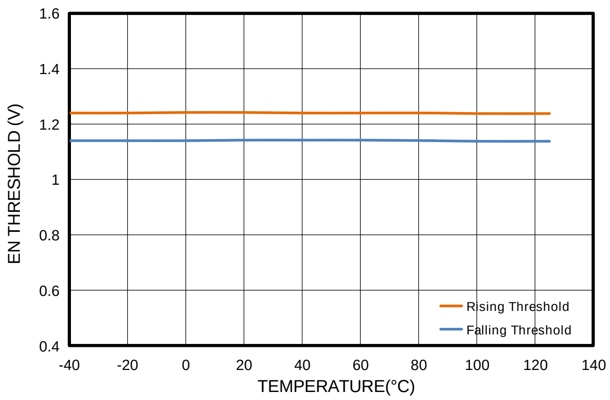


V_{EN}=0V

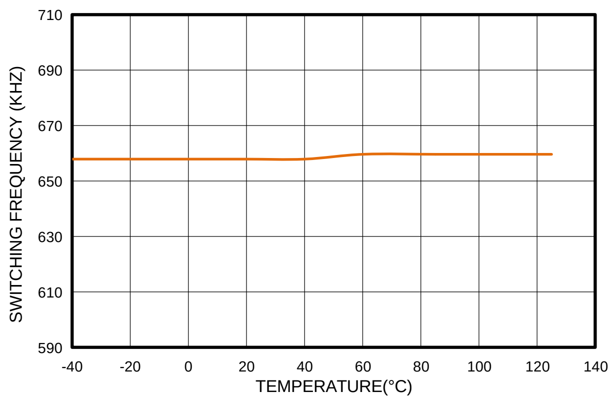
Input Voltage Threshold vs. Temperature



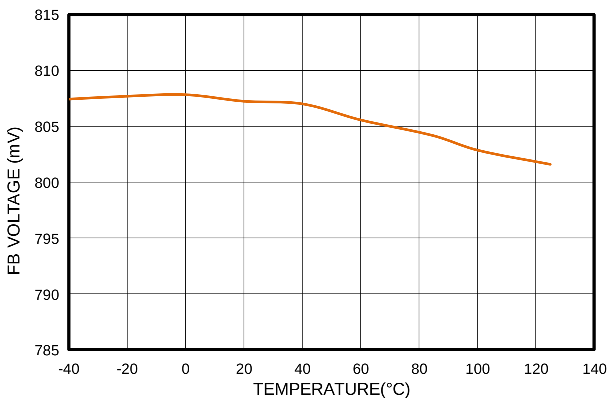
EN Threshold vs. Temperature



Switching Frequency vs. Temperature



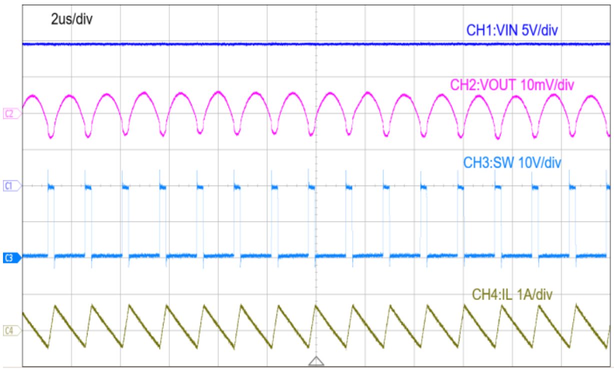
FB Voltage vs. Temperature



Application Curves(Continued)

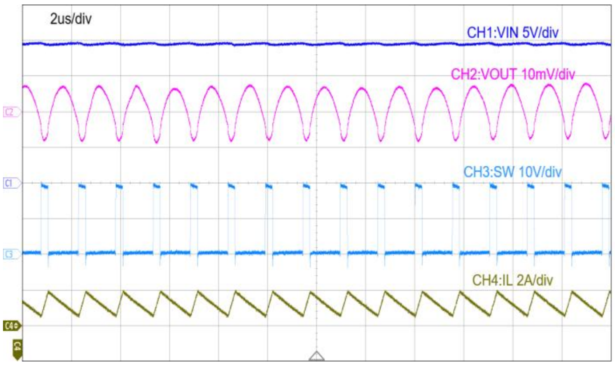
V_{IN} = 19V, F_{SW} = 650kHz, T_A = +25°C (unless otherwise noted).

Input/Output Ripple vs. I_{OUT} = 0A



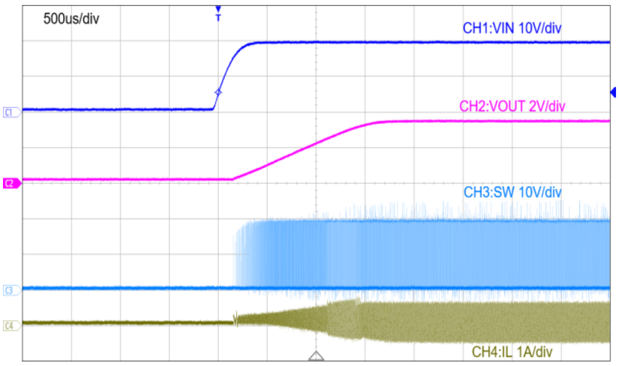
500us/div

Input/Output Ripple vs. I_{OUT} = 3A



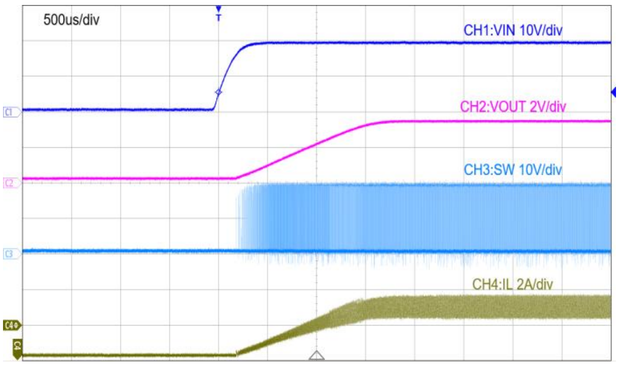
500us/div

Start-Up through Input Voltage vs. I_{OUT} = 0A



500us/div

Start-Up through Input Voltage vs. I_{OUT} = 3A



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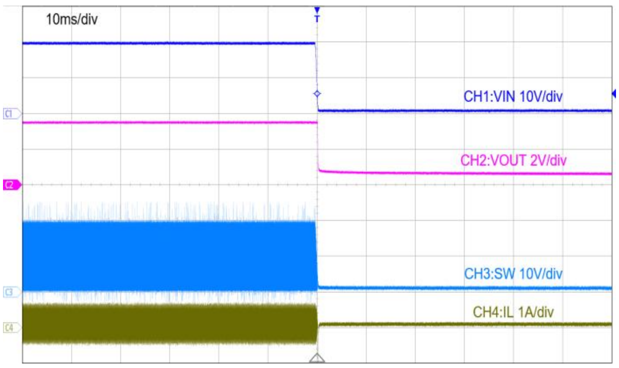
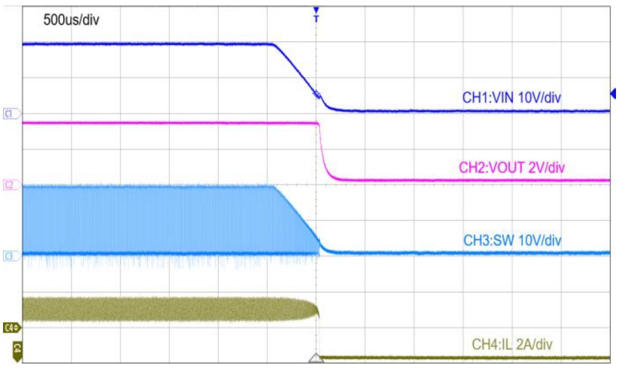
Shutdown through Input Voltage vs. I_{OUT} = 0A



10ms/div

Shutdown through Input Voltage vs. I_{OUT} = 3A

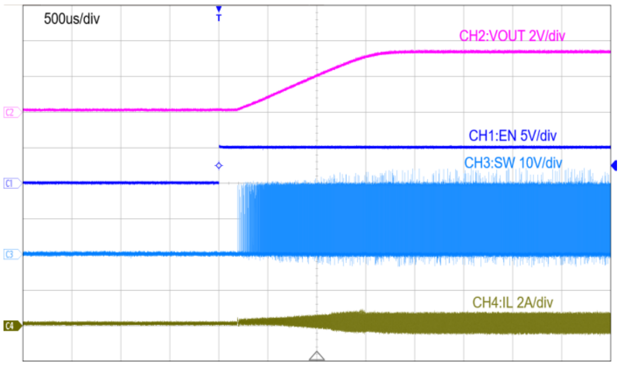


500us/div

Application Curves(Continued)

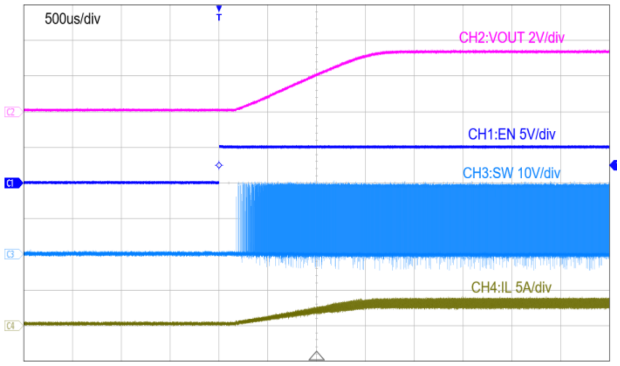
V_{IN} = 19V, F_{SW} = 650kHz, T_A = +25°C (unless otherwise noted).

Start-Up through Enable vs. I_{OUT} = 0A



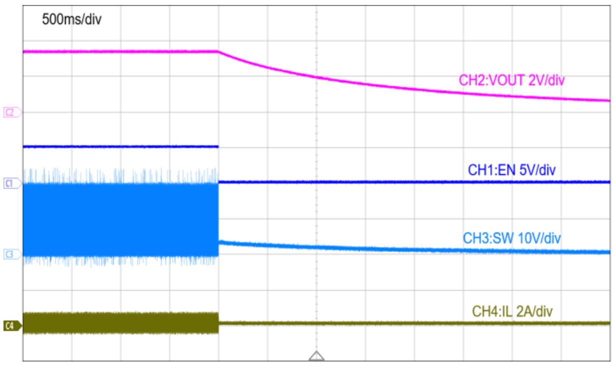
500us/div

Start-Up through Enable vs. I_{OUT} = 3A



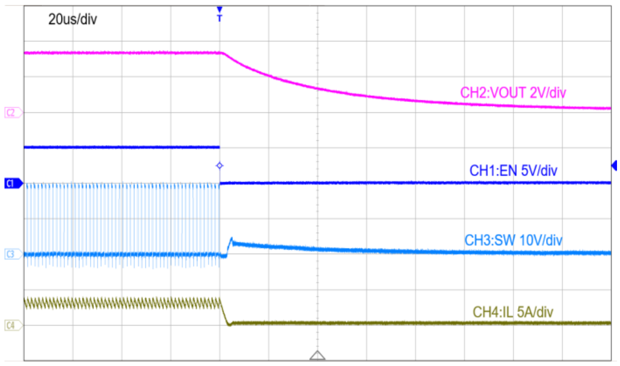
500us/div

Shutdown through Enable vs. I_{OUT} = 0A



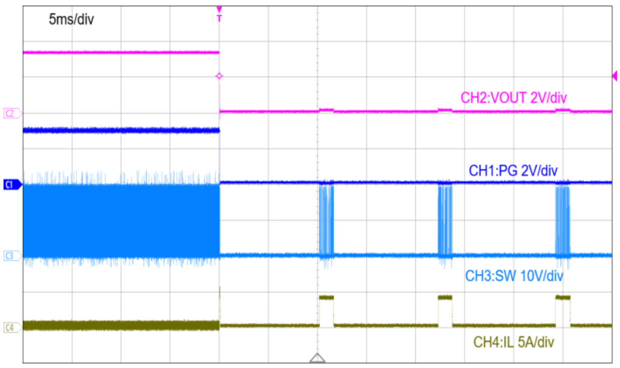
500ms/div

Shutdown through Enable vs. I_{OUT} = 0A



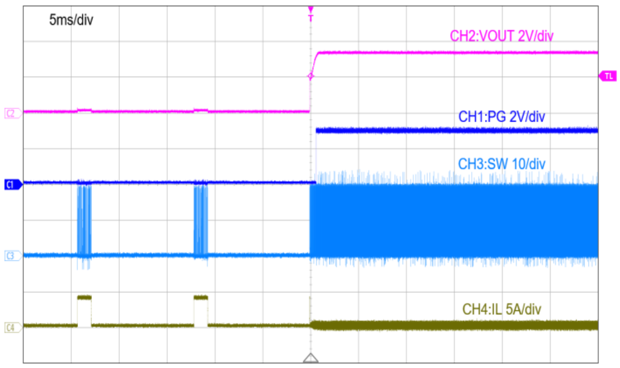
500us/div

Short-Circuit Entry vs. I_{OUT} = 0A



5ms/div

Short-Circuit Recovery vs. I_{OUT} = 0A

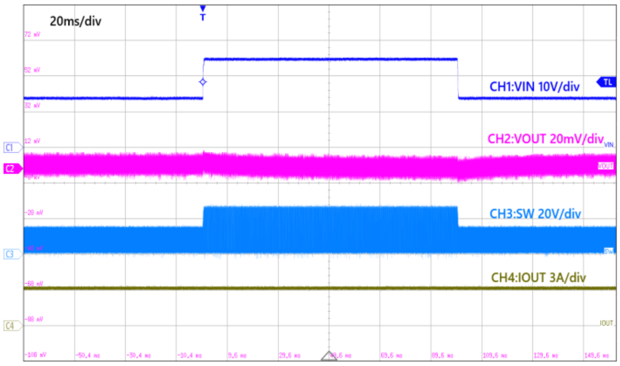


5ms/div

Application Curves(Continued)

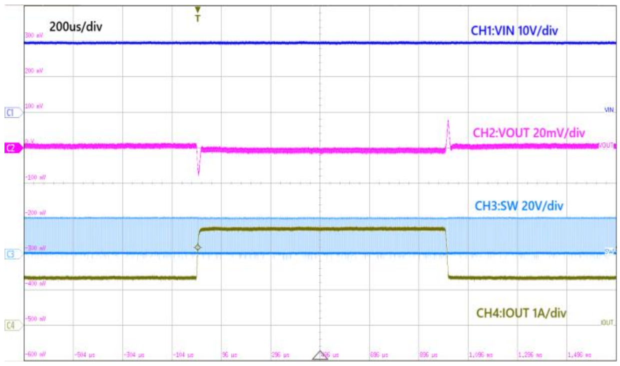
V_{IN} = 19V, F_{SW} = 650kHz, T_A = +25°C (unless otherwise noted).

VOUT=3.3V Line Transient Test



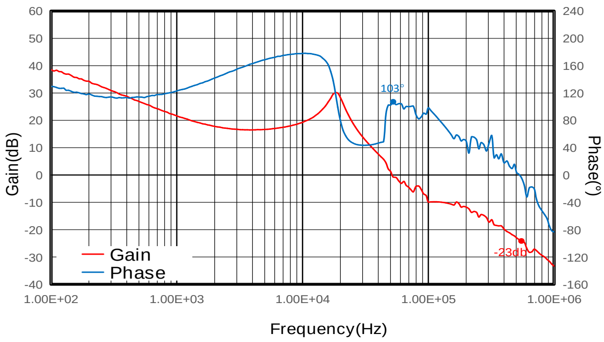
VIN from 13V to 24V

VOUT=3.3V Load Transient Test



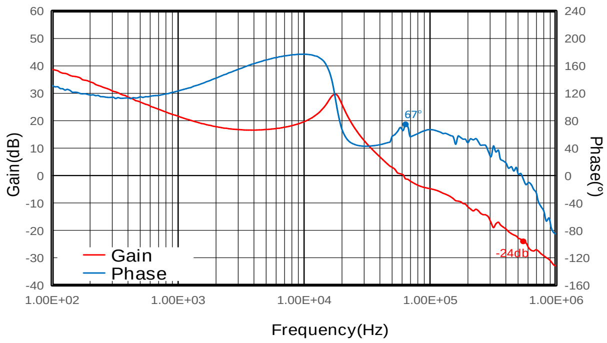
Load Current from 1.5A to 3.0A(2.5A/μs E-load)

Bode Plot



VIN=13V, VOUT=3.3V, IOUT=10mA

Bode Plot



VIN=13V, VOUT=3.3V, IOUT=3A

Typical Application

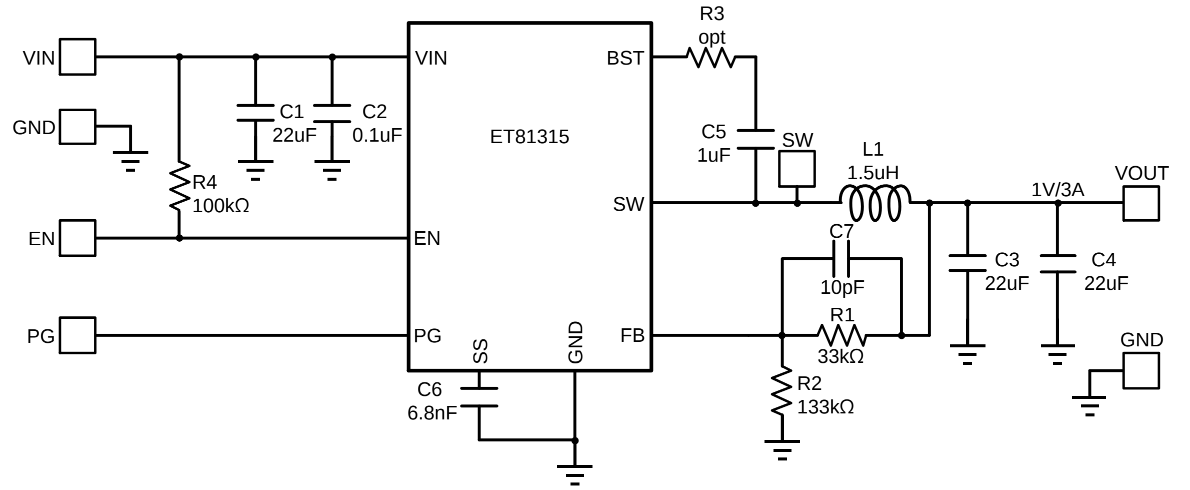


Figure 4: V_{IN} = 19V, V_{OUT} = 1V/3A

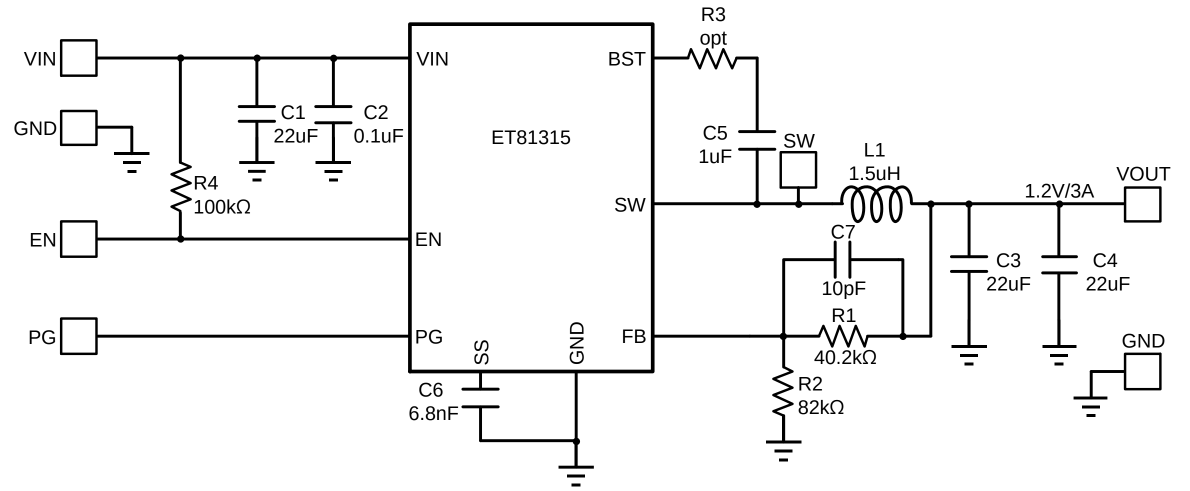


Figure 5: V_{IN} = 19V, V_{OUT} = 1.2V/3A

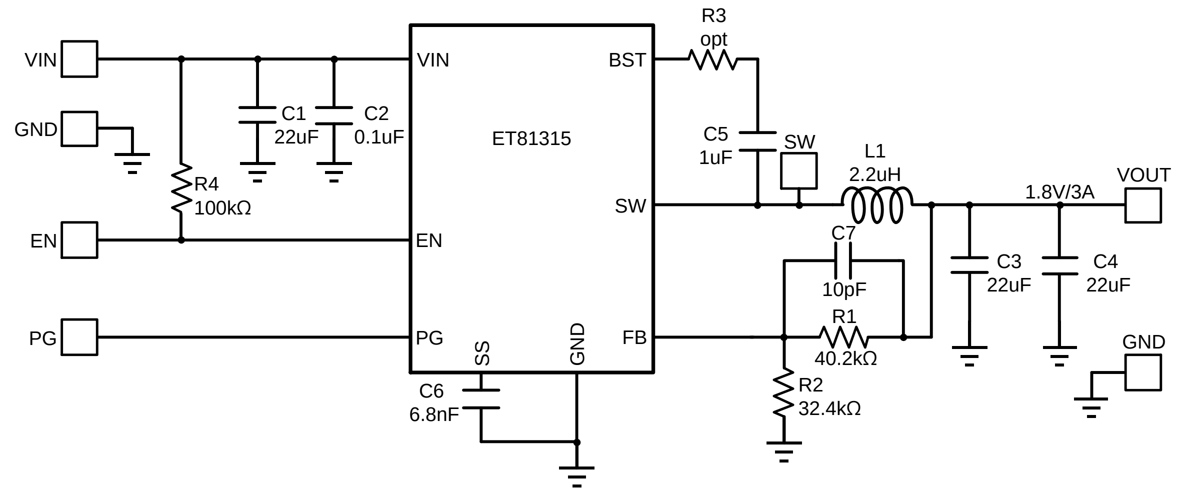


Figure 6: V_{IN} = 19V, V_{OUT} = 1.8V/3A

Typical Application(Continued)

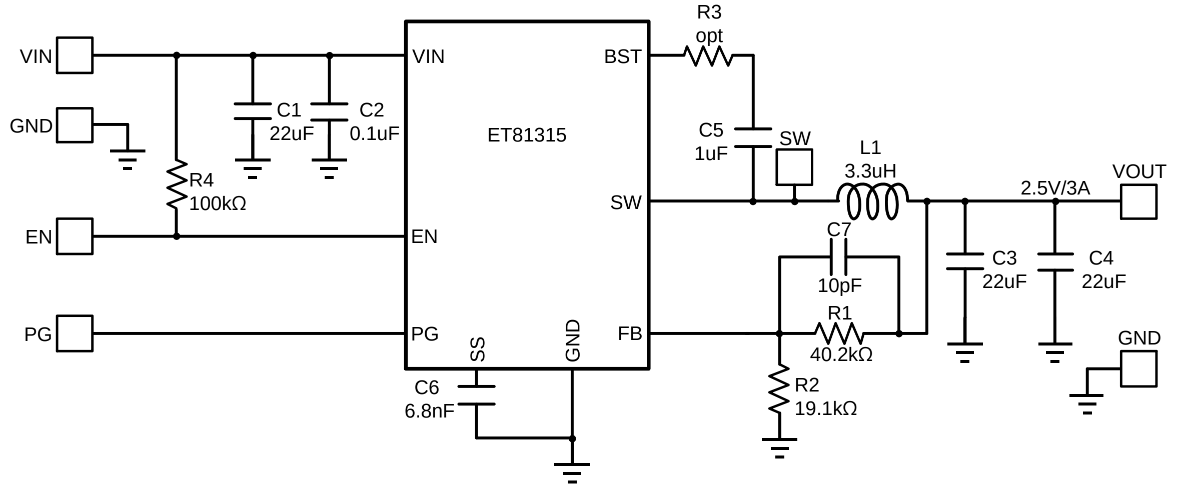


Figure 7: V_{IN} = 19V, V_{OUT} = 2.5V/3A

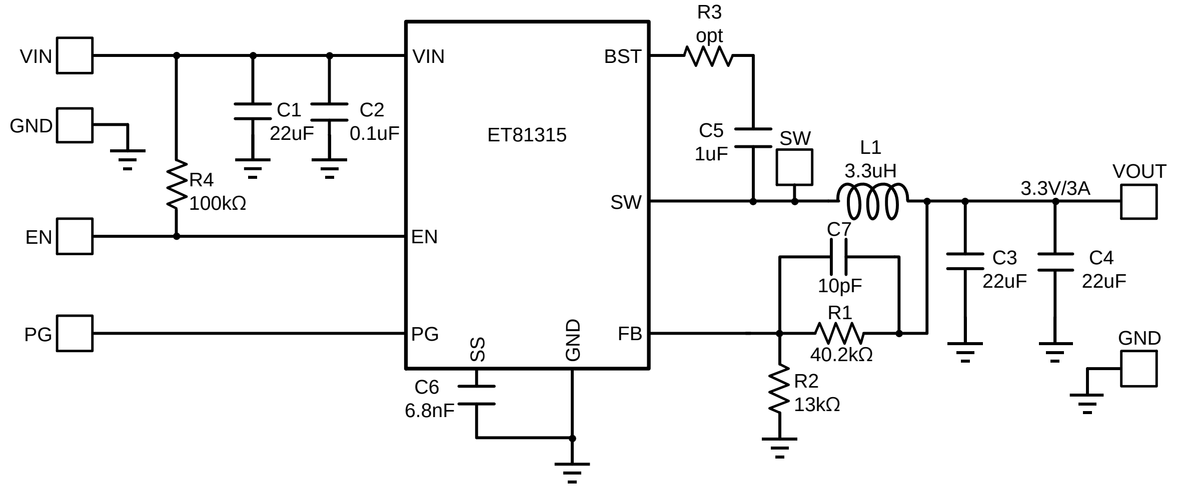


Figure 8: V_{IN} = 19V, V_{OUT} = 3.3V/3A

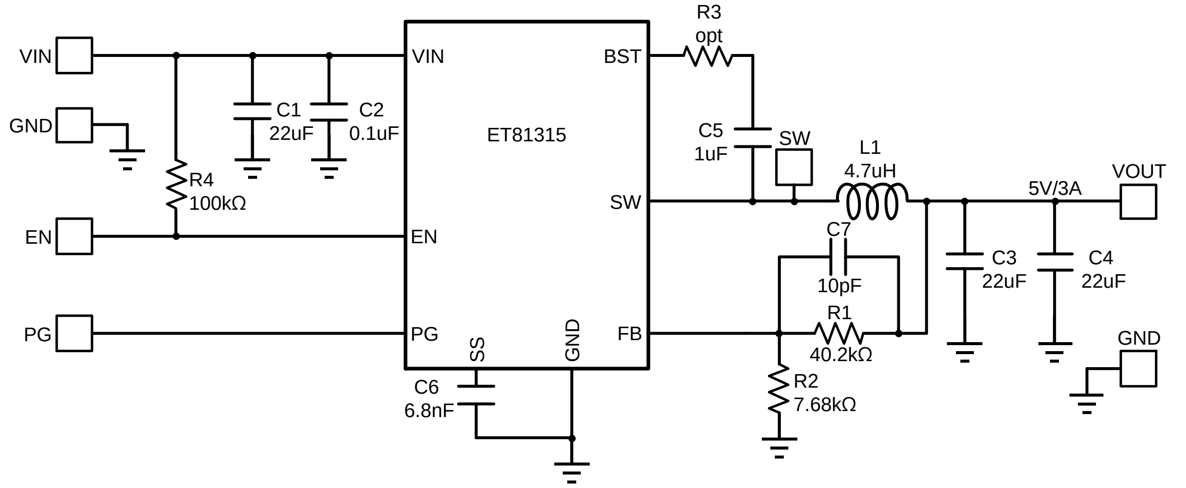
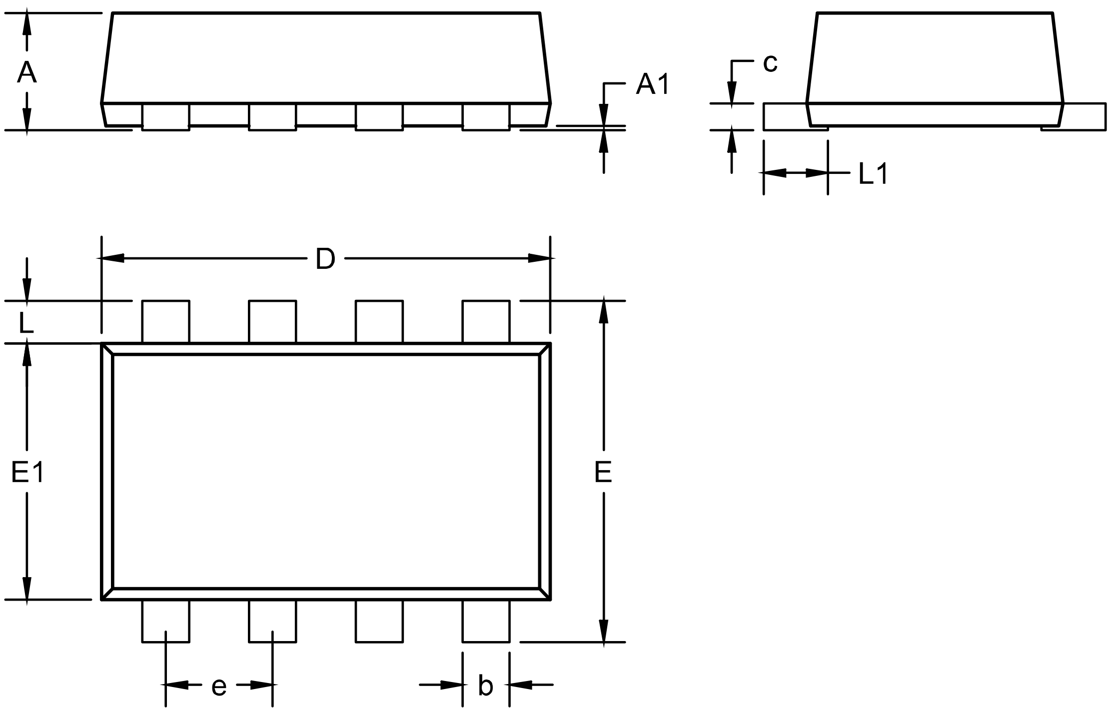


Figure 9: V_{IN} = 19V, V_{OUT} = 5V/3A

Package Dimension

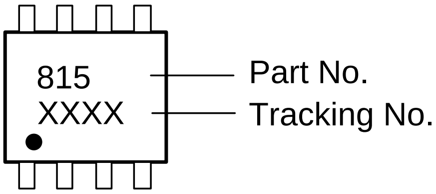


COMMON DIMENSIONS

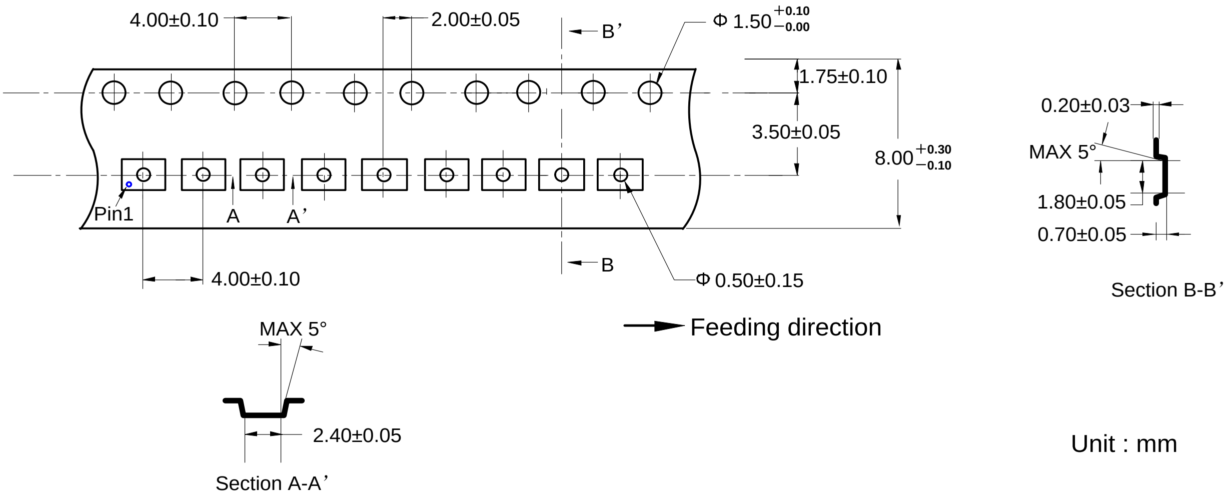
(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	0.525	—	0.6
A1	0.00	—	0.05
b	0.17	0.22	0.27
c	0.09	—	0.18
D	2.00	2.10	2.20
E	1.50	1.60	1.70
E1	1.10	1.20	1.30
e	0.45	0.50	0.55
L	0.10	0.20	0.30
L1	0.20	0.30	0.40

Marking



Tape Information



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-08-09	Preliminary Version	Liuj	Liuj	Liujy
1.0	2025-10-20	Officially Version	Wuhs	Liuj	Liujy