6 ~36V Input, 2A, high efficiency under light load Synchronous Step-down Converter

General Description

The ET8124S0 is a high-efficiency synchronous DC step-down converter with a rated load current capability of up to 2A. It operates within an input voltage range of 6V to 36V and features integrated high-side and low-side MOSFETs with typical on-resistance values of 90mΩ and 65mΩ. The device supports light-load skip-mode operation to enhance efficiency under light-load conditions, with a quiescent current of only 6μA in shutdown mode. Across the full temperature range, its reference voltage accuracy is 1.5%, ensuring precise output voltage regulation.

ET8124S0 is equipped with various high-sensitivity protection functions, including enable control, under-voltage latch, soft start, over temperature shutdown, cycle by cycle current detection, over-current, short-circuit protection, etc., further enhancing its reliability in applications.

The ET8124S0 is available in an ESOP8 package.

Features

- 6V to 36V Input Voltage Range
- 1V to 24V Adjustable Output Voltage Range
- Reference Voltage and Accuracy: 0.6V, 1%
- 2A Continuous Output Current
- 6μA Shutdown Current (Typ)
- 500 kHz Fixed Frequency
- Light Load Control Mode: PFM
- Low On Resistance：90mΩ/65mΩ（High/Low-Side）
- Current Mode Control
- Multiple Protection Function
  - -- Over Current Protection Function
  - -- Short Circuit Protection Function
  - -- Cycle By Cycle Current Detection Function
  - -- Under Voltage Latch Function
  - -- Over Temperature Protection Function
- Compatible with Both Internal and External Soft Start Functions
- Enable Control

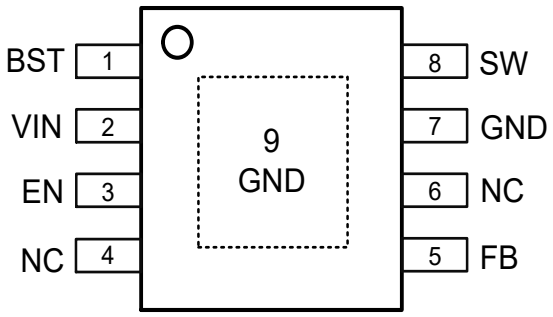
- Integrated Bootstrap Capacitor FET
- Soft Start: 1.5ms (Typ)
- Package:

Part No.	Package
ET8124S0	ESOP8

Applications

- Industrial automation and motor control
- Monitoring system
- Printer system
- Automotive battery voltage stabilization
- Industrial power supply
- Telecommunications and data communication systems

Pin Configuration



Top View

Pin Function

Pin No.	Pin Name	Pin Function
BST	1	High side gate pole drive input. When applied, connect a 10nF capacitor in series between this pin and the SW pin.
VIN	2	Voltage input pin. The power supply voltage range of ET8124S0 is 6V to 38V, and a decoupling capacitor needs to be added to this pin, and a wider PCB routing method is used to provide sufficient current path.
EN	3	Enable pins: High Activity. When soft disconnect is not needed, it can be directly connected to VIN Pin. In application, it is recommended to connect a resistor of not less than 2k in series between EN and VIN Pins. This pin cannot be used floating.
NC	4,6	No Connection.
FB	5	Output feedback pin. Connect this pin to the center point of the output resistor voltage divider to regulate the output voltage.
GND	7	Ground. When designing the PCB, attention should be paid to the reference ground of the output voltage. The GND of the output capacitor and the GND of the input capacitor should be as close as possible to the GND of the device system to ensure that the parasitic inductance is as small as possible, thereby achieving better EMC performance.
SW	8	Switch output pin. During PCB design, thicker wires are used to connect with inductors in order to optimize EMI.
GND	9	Thermal Pad , connected to GND, can improve the thermal performance of the device by maintaining sufficient soldering with the PCB.

Block Diagram

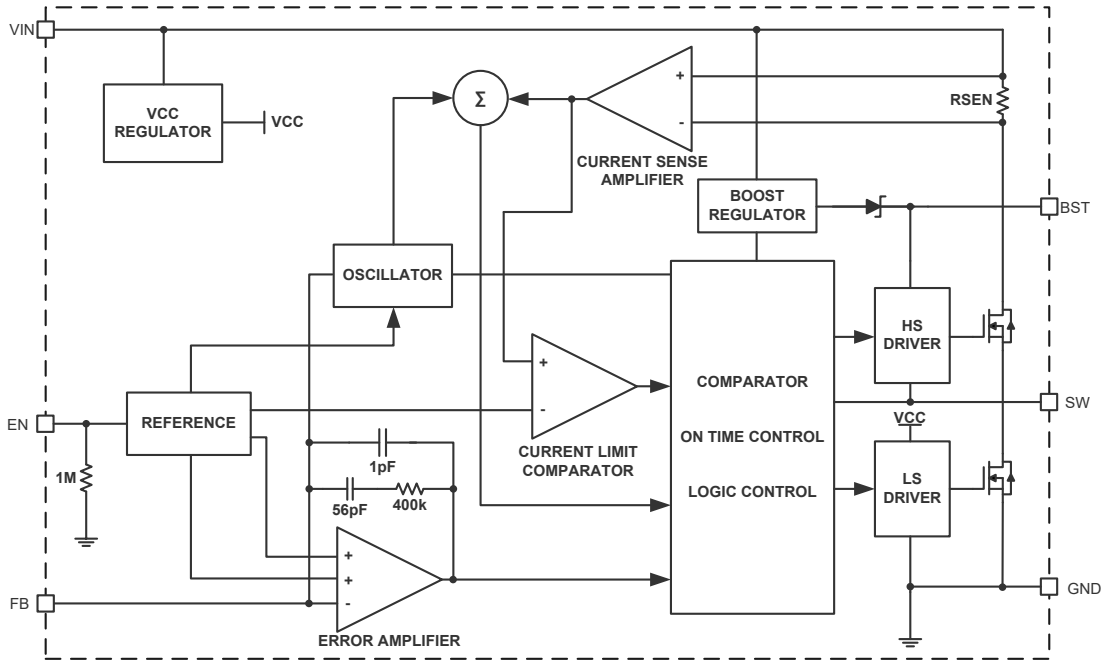


Figure 1. Internal functional block diagram

Functional Description

The ET8124S0 is high efficient, 500kHz synchronous buck DC/DC regulator that can provide up to 2A load current. It can operate within a wide input voltage range of 6V to 36V and integrates the main switch and synchronous switch together, with very low on resistance to minimize conduction losses. ET8124S0 provides protection functions such as weekly flow restriction and hot shutdown protection.

Soft Start

The ET8124S0 has an internal soft start circuit that limits inrush current during the start-up process, allowing the converter to gradually reach the steady-state operating point and reduce the impact of start-up surges. During the start-up process, the switch current limit gradually increases, and the typical soft start time for this device is 1.5ms.

Over Current Protection and Short Circuit Protection

If the current of the high side power field-effect transistor is higher than the peak current limit threshold, the high side power field-effect transistor will be turned off and the low side power field-effect transistor will be turned on. If the current of the low side field-effect transistor is higher than the valley current threshold, the low side field-effect transistor will continue to turn on until the current of the low side field-effect transistor drops below the valley current threshold, so the peak valley current is finite. If the load current continues to increase under these conditions, the output voltage will decrease. When the output voltage drops below 33% of the regulated level, an output short circuit is detected, and the IC will turn off the main switch, stop working for a

period of time (about 9ms), and then restart working (2.5ms). If the output short circuit is eliminated, the system will enter normal operation.

Under Voltage Protection

The EN pin has precise rise and fall thresholds and provides programmable ON/OFF control by connecting an external resistive voltage divider. Once the EN pin voltage exceeds the rising threshold, the device will start working. If the EN pin voltage is pulled below the falling threshold, the device will enter a shutdown state.

Absolute Maximum Ratings

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Symbol	Parameters	Min	Max	Unit
V_{CC}	VIN to GND Voltage Range	-0.3	38	V
	SW、EN to GND Voltage Range	-0.3	V_{IN}+0.3	V
	FB to GND Voltage Range	-0.3	4	V
	BST to SW Voltage Range	-0.3	4	V
V_{ESD}	Human Body Model (HBM)	-	2000	V
	Machine Model (MM)	-	200	V
T_J	c	-	+150	°C
T_A	Recommended Working Temperature Range	-40	+125	°C
T_{STG}	Storage Junction Temperature	-50	+150	°C
θ_{JA}	Thermal Resistance θ_{JA}	-	42.1	°C/W
θ_{JC}	Thermal Resistance θ_{JC}	-	50.9	°C/W

Recommended Operating Conditions

Symbol	Parameters	Min	Max	Unit
V_{IN}	Supply Input Voltage Range	6	36	V
C_{OUT}	Output Capacitor		22*3	uF
L	Inductor Selection Range	4.7	15	uH
T_A	Recommended Working Temperature Range	-40	125	° C

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 5V, L = 10uH, C_{OUT} = 44uF, T_A = 25℃, I_{OUT} = 1A, Unless Otherwise Noted)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage Range		6		36	V
V_{UVP}	Input UVLO Threshold	V_{IN} Rising			5.3	V
V_{HYS}	Input UVLO Hysteresis			0.6		V
I_Q	Quiescent Current	I_{OUT}=0, V_{FB}=V_{REF}×105%		150		uA
I_{SHDN}	Shutdown Current	V_{EN} = 0		6		uA
V_{EN_R}	EN Rising Threshold			1.2		V
V_{EN_F}	EN Falling Threshold			1		V
V_{REF}	FB Reference Threshold			0.6		V
I_{FB}	FB Pin Input Current	V_{FB}=3.3V	-50		50	nA
R_{DSON}	High-Side FET On-Resistance			90		mΩ
R_{DSON}	Low-Side FET On-Resistance			65		mΩ
T_{ON_MIN}	Minimum Conduction Time			50		ns
T_{OFF_MIN}	Minimum Shutdown Time			100		ns
T_{ON_DLY}	Enable Delay Time	from EN high to SW start switching		180		us
T_{SS}	Soft Start Time	V_{OUT} from 0 to 100%		1.5		ms
F_{SW}	Switching Frequency	V_{OUT}=3.3V, CCM		500		kHz
I_{LIM_TOP}	High-Side FET Current Limit Threshold			3		A
I_{LIM_BOT}	Low-Side FET Current Limit Threshold			3		A
T_{SD}	Thermal Shutdown Temp			150		°C
T_{HYS}	Thermal Shutdown Temp Hysteresis	Duty = 30%		15		°C

Application Circuits

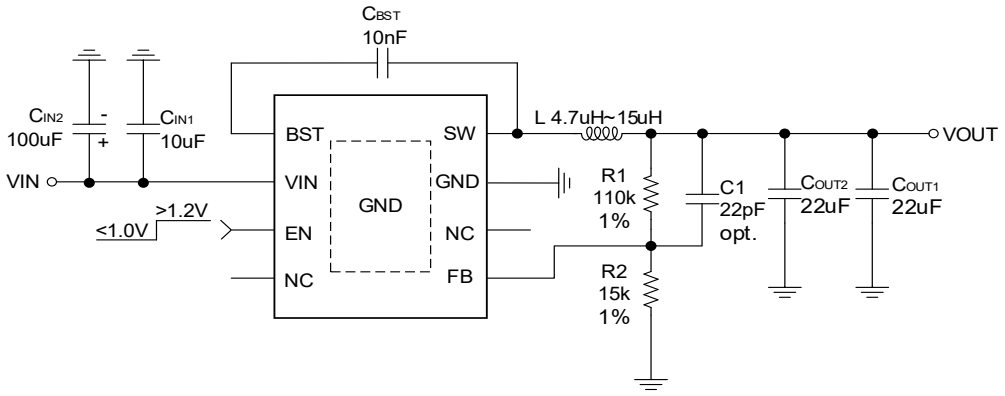


Figure 2. Typical application circuit diagram

*：The circuit is for reference only.

Applications Information

Output Voltage

ET8124S0 uses a resistive voltage divider from the output node to the feedback pin to set the output voltage. It is recommended to use 1% or better accuracy for the voltage divider resistor. The calculation of the output voltage is shown in Equation 1:

$$V_{OUT} = \frac{V_{Feedback} \times (R1 + R2)}{R2} \quad (1)$$

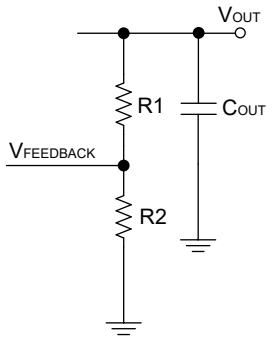


Figure 3. Application of output voltage regulation

To improve efficiency under light loads, high-value resistors can be considered, but excessively high values can increase system noise.

Inductors Selection

In applications, it is recommended to use inductors with a DC rated current at least 25% higher than the maximum load current. To achieve the highest efficiency, please choose inductors with a DC resistance less than 15mΩ. For most designs, derive the inductance value from the following Equation 2:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{(V_{IN} \times \Delta I_L \times F_S)} \quad (2)$$

In Equation 2, ΔIL is the ripple current flowing through the inductor, and the selected inductor has a rated current close to 30% of the maximum load current. The calculation method for the peak current in the inductor is shown in Equation 3:

$$I_{L(MAX)} = I_{Load} + \frac{\Delta I_L}{2} \quad (3)$$

In light load mode (less than 100mA), using a larger inductance can improve device efficiency.

Input Capacitor Selection

The input current of a buck converter is discontinuous, therefore a capacitor is required to provide AC current to the buck converter and maintain DC input voltage. For optimal performance, please use low ESR capacitors, such as ceramic capacitors with X5R or X7R dielectric and low temperature coefficient. For most applications, a 10uF capacitor is sufficient. The input capacitor requires sufficient ripple current rating as it absorbs input switch noise. Equation 4 estimates the RMS current in the input capacitor:

$$I_{CIN} = I_{Load} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad (4)$$

The worst-case scenario occurs when VIN=2VOUT, at which point:

$$I_{CIN} = \frac{I_{Load}}{2} \quad (5)$$

For simplicity, please choose an input capacitor with a rated current greater than half of the maximum load current. The input capacitor can be an electrolytic capacitor, tantalum capacitor, or ceramic capacitor. When using electrolytic capacitors or tantalum capacitors, a small, high-quality ceramic capacitor (0.1uF) should be placed as close to the IC as possible. When using ceramic capacitors, please ensure that they have sufficient capacitance to provide sufficient charge to prevent excessive input voltage ripple. Estimate the input voltage ripple caused by capacitance using Equation 6:

$$\Delta V_{IN} = \frac{I_{Load}}{F_S \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Output Capacitor Selection

The output capacitor stabilizes the DC output voltage and can use ceramic, tantalum, or low ESR electrolytic capacitors. If a low ESR electrolytic capacitor is used, Equation 7 estimates the output voltage ripple:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_S \times C_{OUT}}\right) \quad (7)$$

In Equation 7, L is the value of inductance, and RESR is the equivalent series resistance of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplicity, estimate the output voltage ripple using Equation 8:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F^2_S \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

For tantalum capacitors or electrolytic capacitors, ESR is dominant at the switching frequency, and the approximate estimation method for their output ripple is shown in Equation 9:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor will affect the stability of the regulator system. It is recommended to use X5R or capacitors with better performance materials for the output terminal, and the output capacitor value should preferably be greater than 44uF.

Bootstrap Capacitor Selection

A 0.1F ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. Capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 6.3V or higher voltage rating.

PCB Layout

PCB layout is an important component of DC-DC converter design. Poor circuit board layout can damage the performance of DC-DC converters and surrounding circuits, leading to electromagnetic interference, ground bounce, and loss of voltage accuracy. These will provide feedback error signals to the DC-DC converter, leading to poor or unstable regulation. A good layout can be achieved by following some simple design rules.

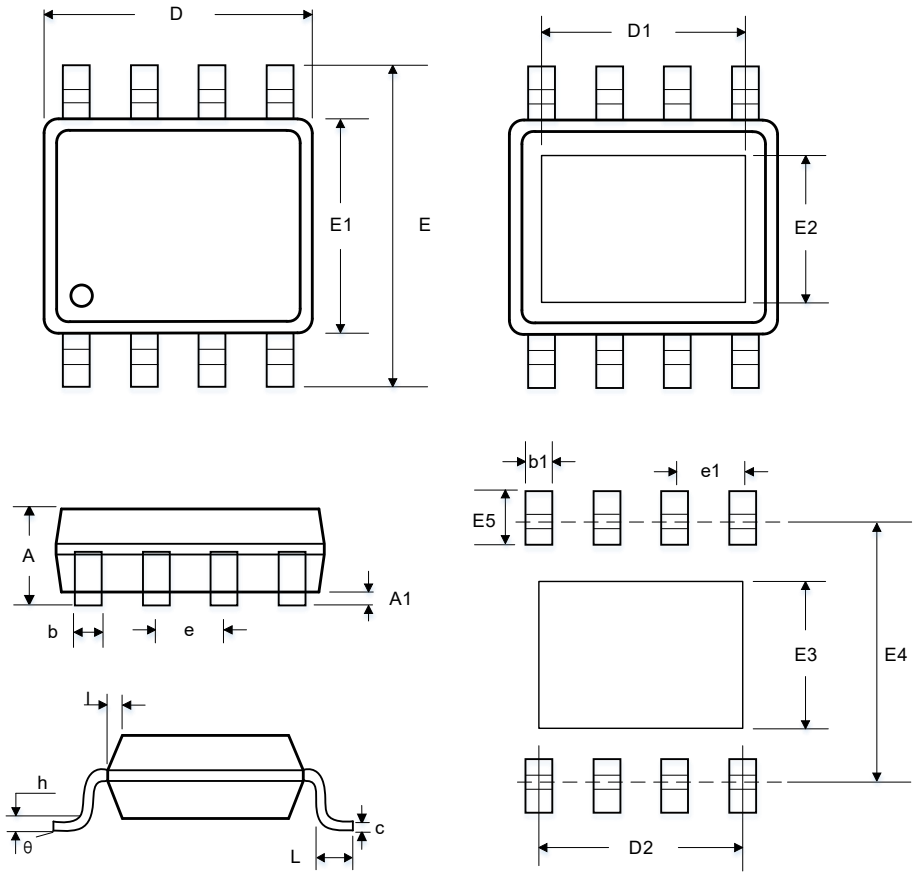
Minimize the area of the switch current circuit as much as possible. In a voltage regulator, there are two circuits for fast switching of current. The first circuit starts from the CIN input capacitor, to the VIN terminal of the regulator, to the SW terminal of the regulator, to the inductor, and then to the output capacitor COUP and load. The second circuit starts from the output capacitor ground, goes to the regulator GND terminal, goes to the inductor, and then goes to the COUP and load. In order to minimize the two circuit areas, the input capacitor should be placed as close as possible to the VIN terminal. The grounding of both input and output capacitors should be connected to GND through a small localized plane. Inductors should be placed as close as possible to the SW pin and output capacitor.

Line width principle:

1. The line width is determined by the magnitude of the current flowing through it. For high current wiring, sufficient line width should be provided to optimize efficiency and reduce heat generation; Especially for SW nodes, copper plating can be used if conditions permit. The line width of the control circuit should be at least 20mil, such as V_{CC}, GND (SGND);
2. Make the input and output bus connections as wide as possible. To reduce any voltage drop on the input or output of the converter and improve efficiency. If the voltage accuracy at the load is important, please ensure that the feedback point is as close to the load as possible, so as to avoid the impact of voltage drop on the feedback acquisition accuracy on the line.
3. Bypass/decoupling capacitor: The capacitor is arranged near the IC power pin. When there are multiple capacitors, the small capacitance value is close to the IC;
4. Minimize the trace length to the FB terminal. The feedback trace should be wired from the SW pin and inductor to avoid switch noise interference on the feedback signal.

Package Dimension

ESOP8



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	1.30	-	1.70	E2	2.26	-	2.55
A1	0.00	-	0.15	E3	-	2.62	-
b	0.33	-	0.51	E4	-	5.40	-
b1	-	0.61	-	E5	-	1.60	-
c	0.19	-	0.25	e	1.27BSC		
D	4.80	-	5.00	e1	1.27BSC		
D1	3.15	-	3.45	L	0.41	-	1.27
D2	-	3.51	-	I	0.25	-	0.50
E	5.20	-	5.80	h	0.25BSC		
E1	3.80	-	4.00	θ	0°	-	8°

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-01-28	Initial version	Caojc	Wuhs	Liujy