USB PD and Other Fast Charging Protocol Sink Controller

General Description

ET73224 integrates multiple fast charging protocols such as USB PD3.0/2.0, BC1.2, automatically detects VCONN and simulates E-Mark chips, and supports up to 100W power. ET73224 has a built-in PD communication module, with features of high integration and streamlined peripherals. It integrates output voltage detection function, and provides over-temperature and over-voltage protection functions, etc. It can be widely used in various electronic equipment to expand high-power input, such as wireless charger, electric toothbrush, rechargeable shaver, lithium battery power tools and other application scenarios. ET73224Q is a USB PD fast charging protocol receiver chip that supports USB PD3.2, up to PD3.2 EPR 140W power, and supports single resistor configuration, I/O level configuration and I^2C configuration. Through the I^2C interface can read the protocol handshake status and read the current PD gear rated current.

Features

- Supports 4V to 22V input voltage
- Supports fast charging protocols such as PD3.0/2.0 and BC1.2.
- Support PD3.2 EPR, AVS, PPS, SPR protocols and BC1.2.(Only ET73224Q)
- Support 400kHz rate I^2C communication. (Only ET73224Q)
- Supports USB Type-C PD. Supports forward and reverse plug detection and automatic switching
- Supports E-Mark simulation and automatic detection of VCONN, and supports 100W power PD request Very Low IQ: 12μA
- The requested voltage can be dynamically adjusted by a variety of methods
- The single chip has features of high integration, simplified peripherals and low costs
- Built-in over-voltage protection module and over-temperature protection module Excellent Load/Line Transient Response
- Package Information:

Part No.	Package	MSL
ET73224	ESSOP-10	Level 1
ET73224D	QFN20	Level 1
ET73224Q	DFN10	Level 1

Applications

- Wireless charger or Laptop charging cable
- Lithium battery minor electric appliances
- Lithium battery electric tool
- Power bank

Pin Configuration(ET73224)

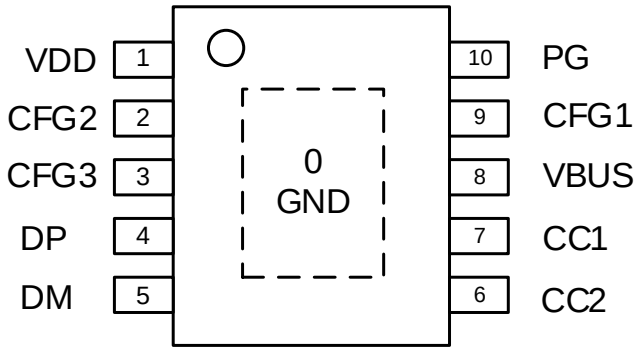


Figure 1. Pin Assignments (Top View)

Pin Function(ET73224)

Pin No.	Pin Name	Pin type	Pin Function
0	GND	Power	Ground. Heat dissipation EPAD.
1	OUT	Power	Operating power input. An external 1uF decoupling capacitor is required. Connected in series with a resistor to VBUS.
4,5	DP, DM	Input/Output	USB data line
6,7	CC1, CC2	Input/Output	Type-C CC data line
2	CFG1	Analog input	Power configuration input
3	CFG2	Analog input	Power configuration input
9	CFG3	Analog input	Power configuration input
8	VBUS	Analog input	Voltage detection input. It is required to be connected in series with a resistor to external input VBUS.
10	PG	Open-drain output	Indicate Power Good by default. Active low. Customized functions.

Pin Configuration(ET73224D)

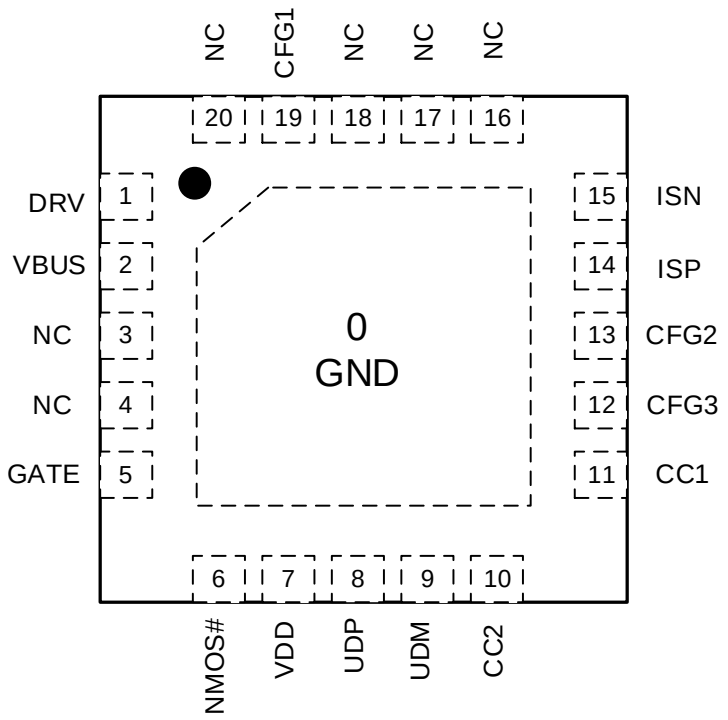


Figure 2. Pin Assignments (Top View)

Pin Function(ET73224D)

Pin No.	Pin Name	Pin type	Pin Function
0	GND	Power	Ground. Heat dissipation EPAD.
1	DRV	Output	Weak driving output. Used to drive configuration resistor.
2	VBUS	Power	Operating power input
5	GATE	HV output	Used to drive high-side power channel NMOS. Customized functions.
6	NMOS	Digital input	GATE pin drive NMOS enable. Active low.
7	VDD	Power	Internal voltage regulator output. An external 1uF decoupling capacitor is required.
8, 9	DP, DM	Input/Output	USB data line
10, 11	CC1, CC2	Input/Output	Type-C CC data line
19,13,12	CFG1~3	Input	CFG1 is analog input. CFG2 and CFG3 are digital inputs, with built-in pull-down resistors.

Pin Configuration(ET73224Q)

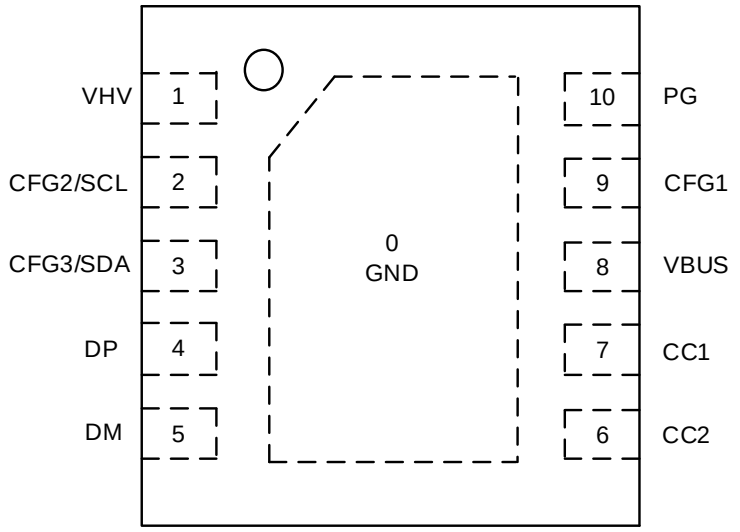


Figure 3. Pin Assignments (Top View)

Pin Function(ET73224Q)

Pin No.	Pin Name	Pin type	Pin Function
0	GND	P	Common ground terminal, heat dissipation EPAD.
1	VHV	P	Operating power supply input, externally connected with 1uF capacitance to ground (pay attention to tolerant voltage).
4	DP	I/O	USB bus.
5	DM	HV output	Used to drive high-side power channel NMOS. Customized functions.
7	CC1	I/O	Type-C CC signal line.
6	CC2	Power	Internal voltage regulator output. An external 1uF decoupling capacitor is required.
9	CFG1	I	Power gear configuration input pin 1.
2	CFG2/SCL	I,PU	Power gear configuration input pin 2 or I^2C clock input pin.
3	CFG3/SDA	I/O,PU	Power gear configuration input pin 3 or I^2C data bidirectional pin.

Notes: Pin type abbreviation explanation:

I = Signal input;

O=Signal output;

P = Power supply or ground;

OD = Open-drain output;

HV = High voltage pin;

PD = Built-in pull-down resistor;

PU = Built-in pull-up resistor.

Block Diagram

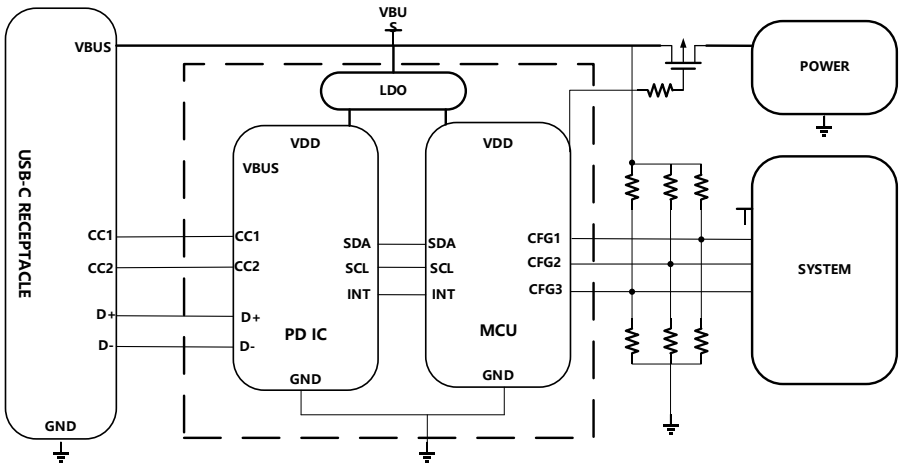


Figure 4. Block Diagram

Absolute Maximum Ratings

Operating in critical ratings or exceeding the absolute maximum ratings may cause the chip to work abnormally or even be damaged.

Symbol	Parameters (Items)	Min	Max	Unit
TA	Operating ambient temperature	-40	90	°C
TS	Storage ambient temperature	-55	105	°C
VDD	Operating supply voltage (VDD is connected to power, GND to ground)	3.0	3.6	V
VODHV	Voltage on CFG and VBUS which support high voltage	-0.5	13.5	V
VIOCC	Voltage on CC1, CC2 and CFG1	-0.5	8	V
VIOUX	Voltage on DP, DM, CFG, CFG2 and CFG3	-0.5	VDD+0.5	V
PD	Maximum power consumption of the entire chip (VDD voltage * current)		400	mW

Note: Rating at mounting on a board (PCB board dimension: 40mm x 40mm (4layer), copper: 1OZ).

Electrical characteristics

Test condition: TA=25°C

Symbol	Parameters	Min	Typ	Max	Unit
VLDOK	ET73224 internal power regulator VDD parallel voltage	3.24	3.3	3.36	V
ILDO	Draw current on VDD pin	0		30	mA
TOTA	Reference threshold of the over-temperature module (OTA	90	105	120	°C
VR	Power-on reset threshold	2.2	2.4	2.6	V

Functional specification

Overview

ET73224 is a USB PD sink controller, supports fast charge protocols such as PD3.0/2.0 and BC1.2, supports 4V to 22V, and can dynamically configure the request-voltage through multiple methods.

ET73224 supports resistance configuration mode and level configuration mode.

Request-voltage configuration

It is suitable for applications to achieve different request-voltages by modifying the value of the resistor in a single PCB.

CFG1 is connected with a resistor to GND. Different request-voltages are available by configuring different resistance values. In resistor configuration mode, the CFG2 and CFG3 pins cannot be connected. The resistances and the corresponding request-voltages are shown in the table below.

Table 1. ET73224/ET73224D

Resistance on CFG1	Request-voltage
6.8KΩ	9V
24KΩ	12V
56KΩ	15V
NC	20V

Table 2. ET73224Q

Resistance on CFG1	Request-voltage
6.8KΩ	9V
24KΩ	12V
56KΩ	15V
120KΩ	20V
210KΩ	28V

Level configuration mode

It is suited when an MCU is used to dynamically adjust the request-voltage, or when the PCB circuit is not changed.

CFG1, CFG2 and CFG3 can be directly connected to the external MCU IO ports, or directly connected to the VDD/GND pin on ET73224.Different request-voltages are available by configuring the level on the 3 pins, as shown in the table below.

CFG1	CFG2	CFG3	Request-voltage
1	-	-	5V
0	0	0	9V
0	0	1	12V
0	1	1	15V
0	1	0	20V

In level configuration mode, the voltage on IO ports and default states should be noted.

For ET73224, the input voltage on CFG2/CFG3 cannot be higher than 3.7V.

If the back-end circuits such as MCU start slowly, or if the MCU pins have a specific default state, CFG1 may be in floating state or in IO configuration mode before MCU starts working. In this case, 20V may be requested. If the system cannot withstand 20V input, a configuration resistor should be added to the CFG1 pin to ensure that ET73224 can request a suitable voltage by configuring the resistor before MCU starts working.

I²C Configuration

When the chip is configured as a single resistor, the I²C configuration function is automatically enabled. At this time, the voltage request can be controlled or related information can be read through I²C communication.

ET73224Q 7-bit I²C address is 0x22 or 0x23 (excluding read and write bits).

Address	Name	Function
0x09	I²C status register	Get the current protocol status
0x0A	Voltage control register	Switching request voltage
0x50	Current data register	Get the maximum available current in the current gear
0x51	AVS voltage configuration register (high eight bits)	Configure the AVS request voltage high eight bits
0x52	AVS voltage configuration register (low eight bits)	Configure the AVS request voltage low eight bits
0x53	PPS voltage configuration register	Configure PPS request voltage
0x60~0x8F	PD power data register	Get complete power information of the adapter

Register detailed description, see below

0x09: I²C status register

Bit	7	6	5	4	3	2	1	0
Name	Reserved	AVS exist	EPR exist	EPR activation	PD activation	QC3 activation	QC2 activation	BC activation
Defaulted Value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Notes:

1. When BIT0, 1, 2, 3, 4 is 1, it indicates that the corresponding protocol handshake is successful.

2. When BIT5 is 1, it indicates that the power supply exists in EPR mode (i.e., adapter maximum power > 100W mode).

3. When BIT6 is 1, it indicates that the power supply exists in AVS mode. 0x0A: Voltage control register

0x0A: Voltage control register

Bit	7	6	5	4	3	2	1	0
Name	Request voltage value, refer to the detailed explanation							
Defaulted Value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Note: Request voltage details:

0: 5V ; 1: 9V; 2: 12V; 3: 15V; 4: 20V; 5: 28V; 6: PPS mode; 7: AVS mode

0x50: Current data register

Bit	7	6	5	4	3	2	1	0
Name	Maximum current reference value (unit: 50mA)							
Defaulted Value	0xXX							
Read/Write	Read-only							

Note: Indicates the maximum current value available under the current PD gear. This register is only valid during the handshake PD protocol.

0x51, 0x52: AVS voltage configuration register high eight bits, AVS voltage configuration register low eight bits

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AVS request voltage value (unit: 25mV)															
Defaulted Value	0x0000															
Read/Write	Write-only															

Note: When configuring, write the upper eight bits first and then the lower eight bits. When applying for AVS for the first time, configure the voltage first, and then configure the voltage control register to AVS mode. Subsequent voltage adjustments can be made by directly modifying the AVS voltage configuration register.

0x53: PPS voltage configuration register

Bit	7	6	5	4	3	2	1	0
Name	PPS setting voltage (unit: 100mV）							
Defaulted Value	0x00							
Read/Write	Write-only							

Note: When applying for PPS for the first time, configure the voltage first, then configure the voltage control register to PPS mode. For subsequent voltage adjustments, simply modify the PPS voltage configuration register.

0x60~0x8F: PD power data register

Defaulted Value	0x00
Read/Write	Read-only

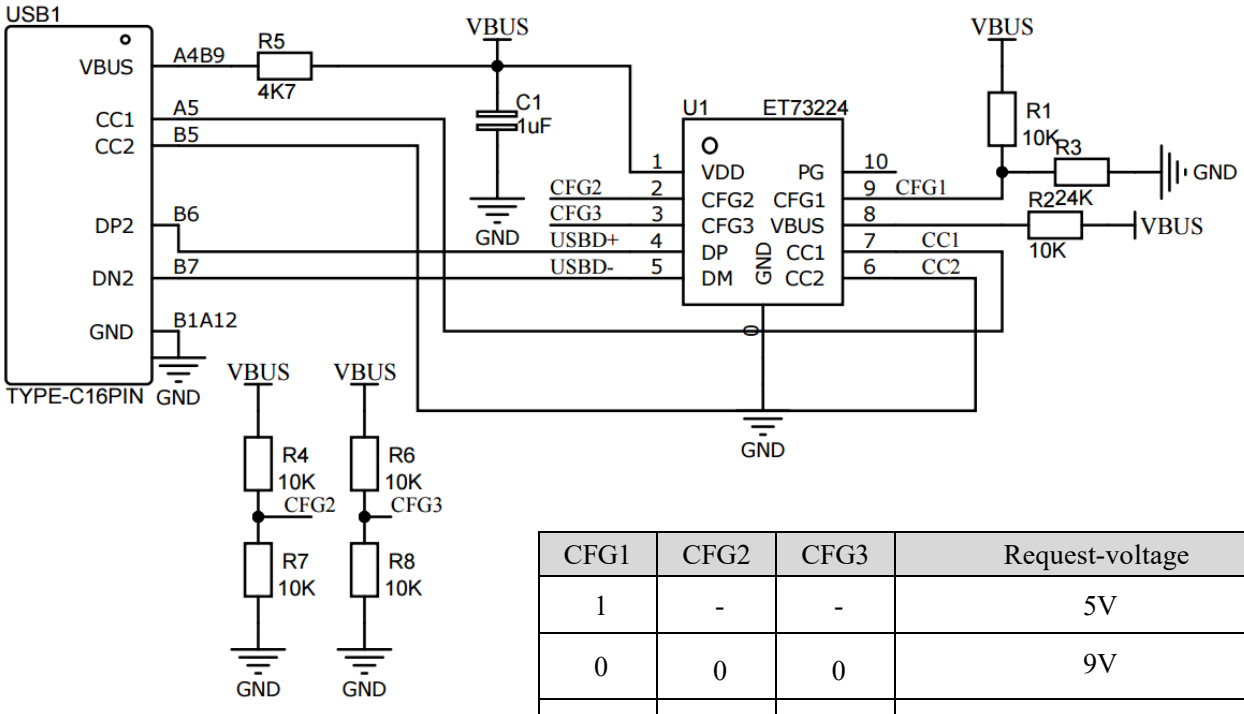
Note: When the adapter's power supply capacity is less than 100W, reading this area can obtain complete power SRCCAP data.
When the chip is in EPR mode (28V), reading this area can obtain the complete EPR_SRCCAP data.

E-Mark simulation function

If you need to simulate E-Mark function to request voltage higher than 20V or power higher than 60W, you must use a Type-C male plug, and connect the CC2 pin with a 1 KΩ resistor to GND. (Please contact us for technical support)

Typical Application

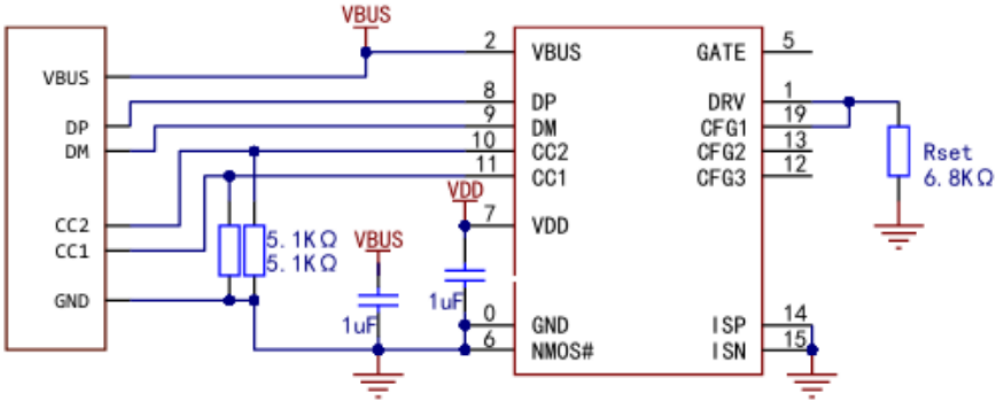
ET73224



CFG1	CFG2	CFG3	Request-voltage
1	-	-	5V
0	0	0	9V
0	0	1	12V
0	1	1	15V
0	1	0	20V

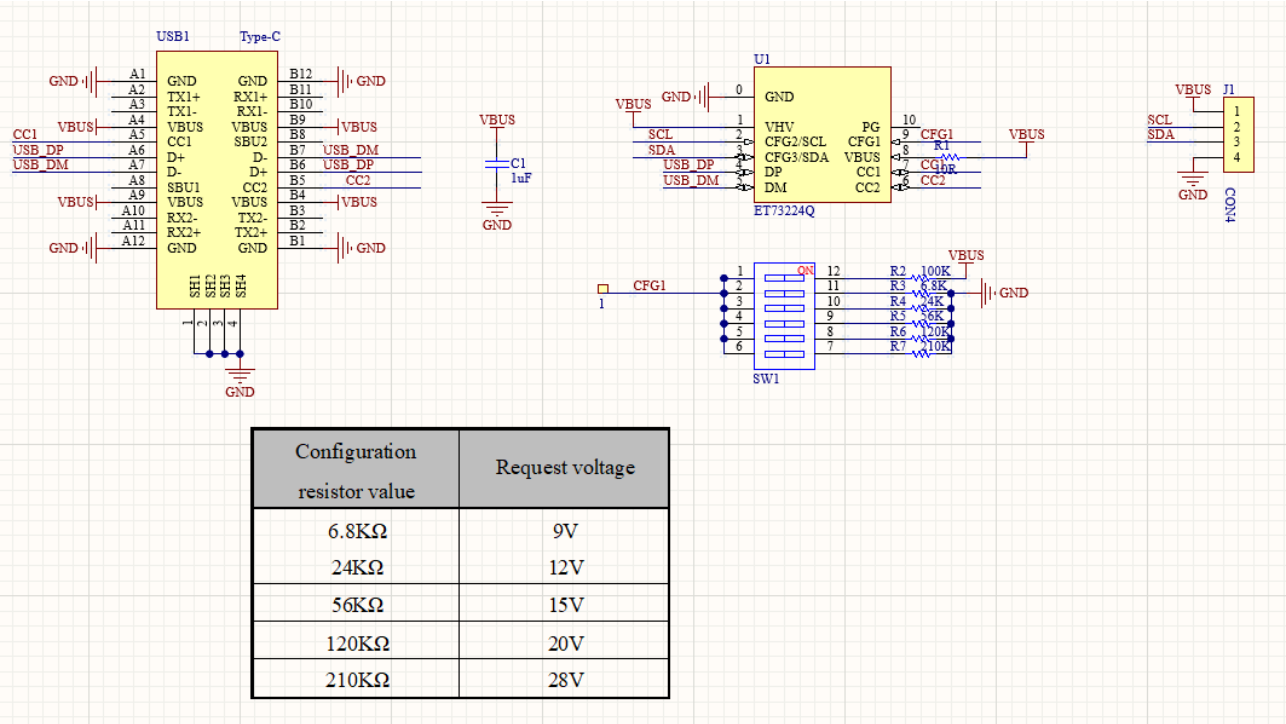
Note: 9/12/15/20V request-voltage configuration by resistance (In the figures below, a 6.8 KΩ resistor is used to configure 9V request voltage)

ET73224



CFG1	Request-voltage
0R	5V
6.8K	9V
24K	12V
56K	15V
NC	20V

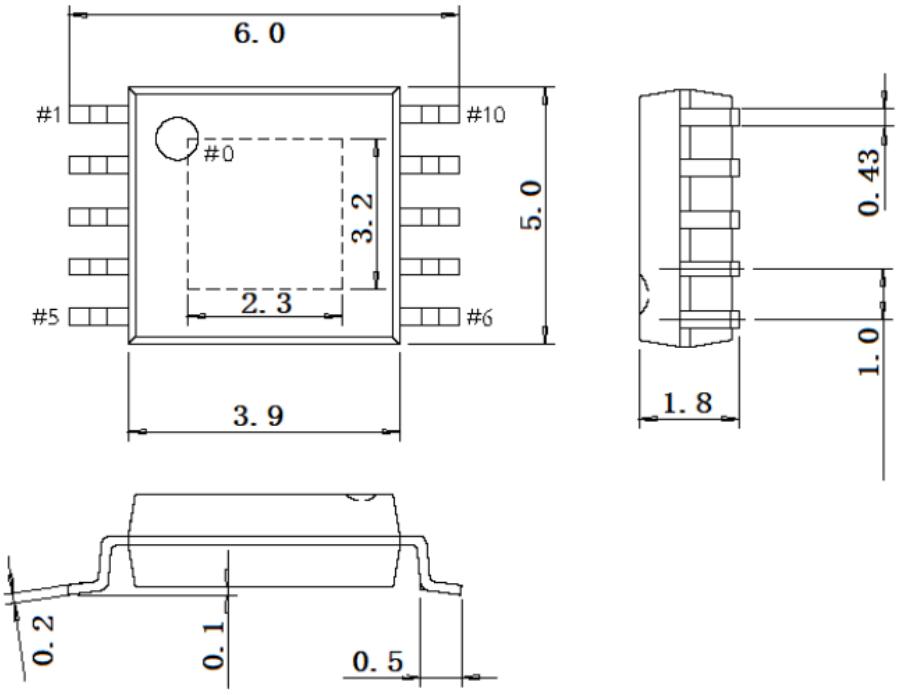
ET73224Q



Configuration resistor value	Request voltage
6.8KΩ	9V
24KΩ	12V
56KΩ	15V
120KΩ	20V
210KΩ	28V

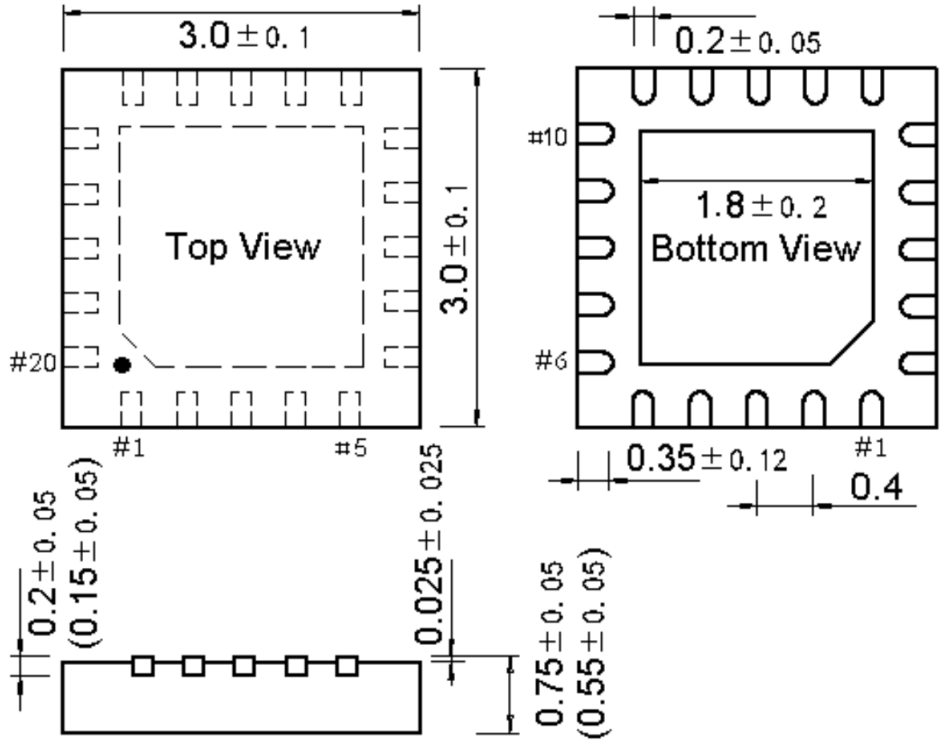
Package Dimension

ET73224



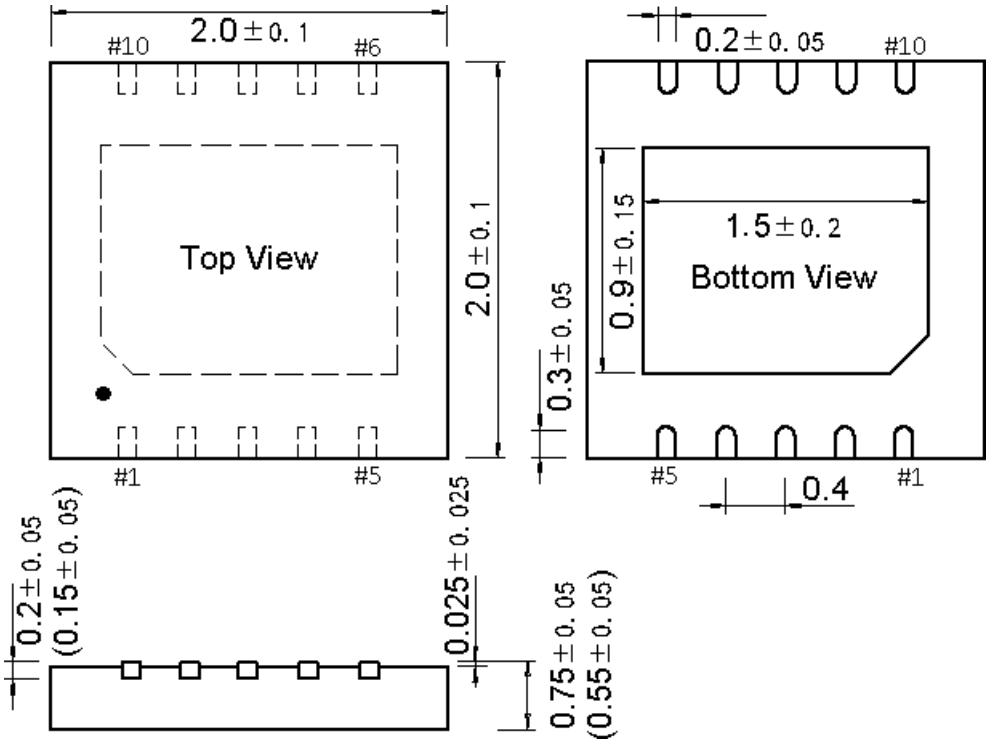
Unit: mm

ET73224D



Unit: mm

ET73224Q



Unit: mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2024-09-24	Original Version	Jiang Sheng	Jiang Sheng	Jiang Sheng
1.1	2024-11-11	Add ET73224D	Jiang Sheng	Jiang Sheng	Jiang Sheng
1.2	2024-12-27	Add ET73224D CIRCUIT	Jiang Sheng	Jiang Sheng	Jiang Sheng
1.3	2024-03-24	Add ET73224Q	Jiang Sheng	Jiang Sheng	Jiang Sheng