ET61934-Constant Current LED Matrix Driving Circuit

General Description

ET61934 is a dedicated circuit for matrix constant current LED driving control. It has strong driving capability and can support up to 128 LEDs. It adopts the I²C communication interface and has strong anti-interference ability. It is mainly applied in the driving of small-sized LED displays.

Features

- I²C communication interface with 4 selectable chip addresses
- Maximum application dot matrix 16 × 8
- Adjustable dot matrix scan rows (1~8 bits)
- Output constant current drive with a maximum driving current of 50mA
- 32-level adjustable constant current output
- Single-channel constant current output with 4-level adjustment
- Built-in RC oscillator with high refresh rate
- Built-in power-on reset and power-off reset functions
- Built-in fade-out feature
- Product name and packaging form:

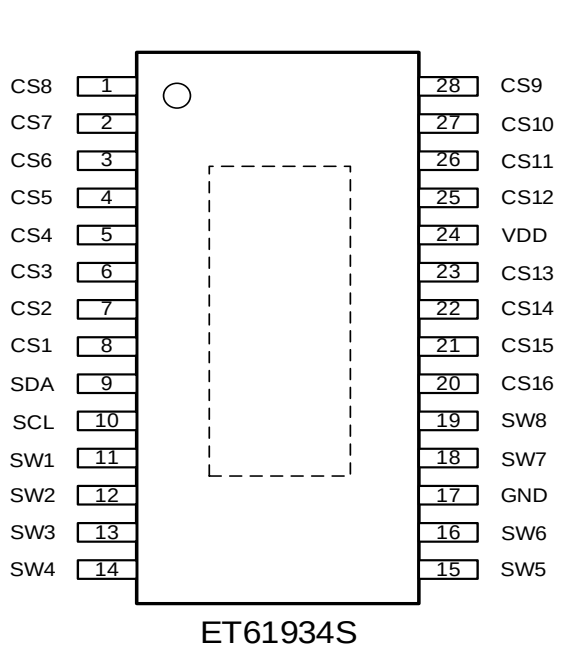
Part No.	Package
ET61934S	EQSOP28
ET61934M32	SOP32

Product Name Description

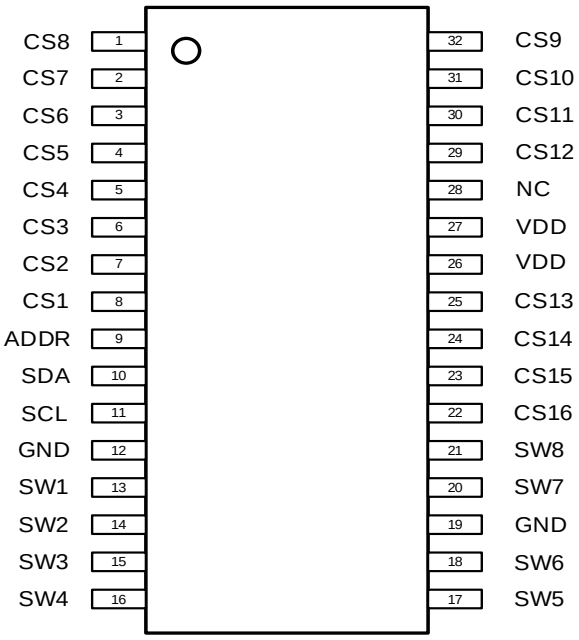
ET 61934 X

61934	X Package	
Product model name	S	EQSOP28
	M32	SOP32

Pin Configurations



ET61934S



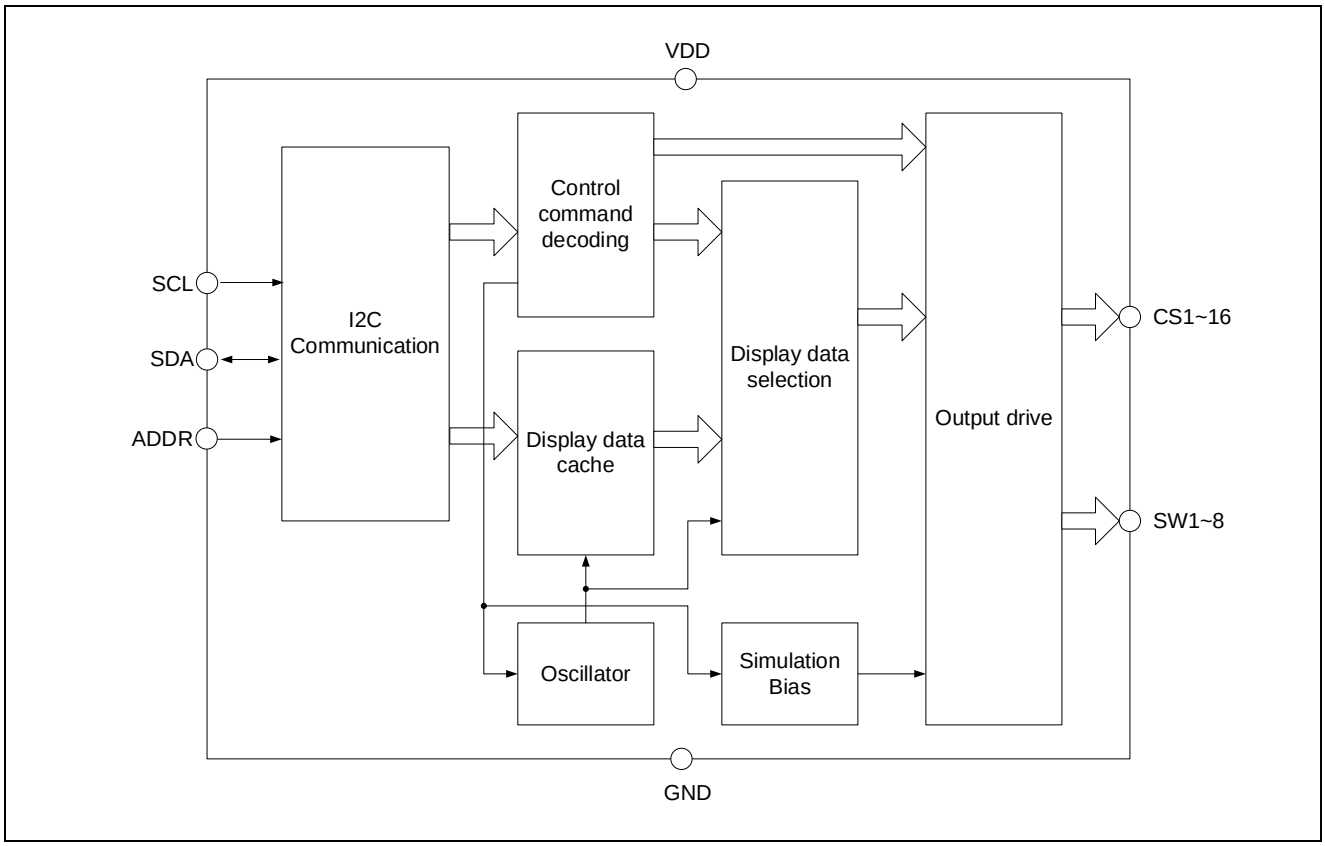
ET61934M32

Top View

Pin Description

Pin number		Symbol	Name	Description
S	M32			
8~1,28~25,23~20	8~1,32~29,25~22	CS1~CS16	Constant current output	Constant current output, connect to the LED anode
11~16,18,19	13~18,20,21	SW1~SW8	Matrix scanning switch	Matrix scanning connected to LED cathode
9	10	SDA	Serial data input	I^2C Serial data input
10	11	SCL	clock input	I^2C Serial clock input
17	12,19	GND	GND	GND
-	9	ADDR	Chip address input	Select different I^2C addresses via external VDD/GND/SCL/SDA inputs, with a built-in 3MΩ pull-down resistor.
24	26,27	VDD	Power supply	Power supply

Block Diagram



Functional Description

ET61934 is a constant current driver chip based on I²C communication protocol for LED display panel. It supports up to 8 ×16 bits of output, and can adjust the number of scanning bits(GRID port) through register configuration, so as to obtain larger single-point driving current.

Compared with the traditional LED display panel driver chip, when the number of LED lights changes, the current of a single LED will change, which will affect the brightness of the display; while the constant current design of ET61934 is adopted, when the display mode is configured, the current of each LED will remain constant, and will not fluctuate due to the number of LED lights.

Communication Protocol

Bus Interface

MCU can transmit data with ET61934 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while

the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET61934 will send a low level response signal with one period width to the SDA port. During the reading mode, ET61934 will not send response signal and the host will send a high response signal one period width to the SDA.

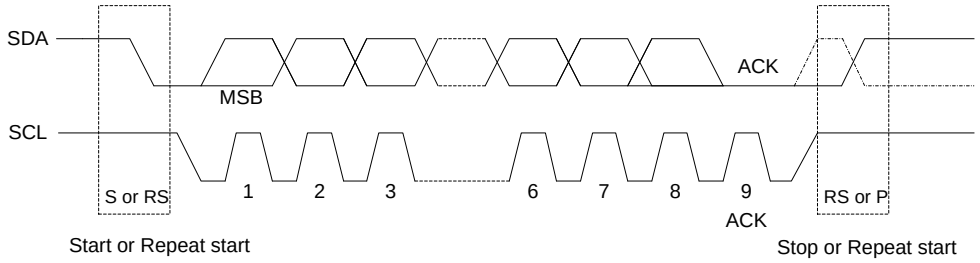


Figure 1. I²C Write Mode

- ACK=Acknowledge
- MSB=most significant bit of a byte
- S=Start signal RS=Restart signal P=Stop signal
- Maximum clock speed = 400KBITS/S
- Restart: SDA-level turnover as expressed by the dashed line waveform.

Chip-Address

The ET61934M32 supports four types of chip addresses, as shown in the table below:

ADDR pin connect signal	7bit chip address	8-bit plus read/write bit
VDD	0111011b(3BH)	76H/77H(W/R)
GND	0111010b(3AH)	74H/75H(W/R)
SCL	0111000b(38H)	70H/71H(W/R)
SDA	0111001b(39H)	72H/73H(W/R)

Note: The default chip address for ET61934S is 74H, the ADDR pin of EQSOP28 package is not exposed.

I²C Writing Command Register Interface Protocol (Single Write):

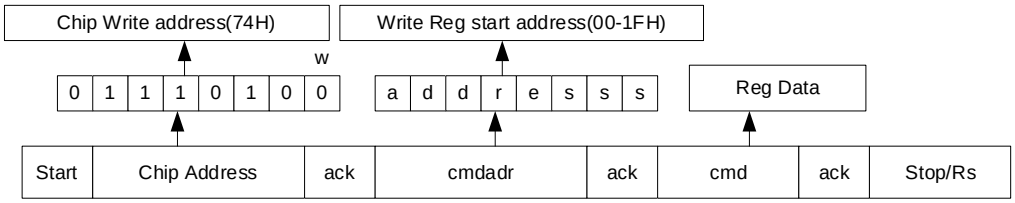


Figure 2. Register Write Mode (Single Write)

- Start =Start Conditions
- Chip Address = Write register address = 0110010+0(w)b
- ack = Acknowledge from ET61934
- Write Reg start address byte = cmdadr(REG’s 8bit address)
- ack = Acknowledge from ET61934
- Command Reg data =cmd(Command data)
- ack = Acknowledge from ET61934
- Stop/Rs=Stop Condition/Restart Condition

I²C Writing Command Register Interface Protocol (Continuous Write):

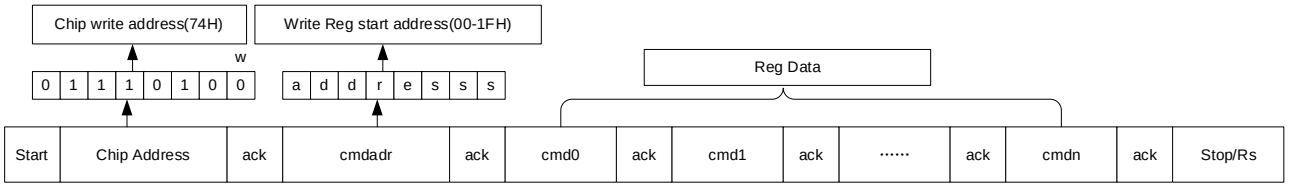


Figure 3. Register Write Mode (Continuous Write)

- Start = Start Conditions
- Chip Address = Write register address = 10000100
- ack = Acknowledge from ET61934
- Write Reg start address byte = cmdadr (REG’s 8bit address)
- ack = Acknowledge from ET61934
- Command Reg data 0=cmd0(Command data)
- ack = Acknowledge from ET61934
- ……
- Command Reg data n=cmdn(Command data)
- ack = Acknowledge from ET61934
- Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol (Single Read):

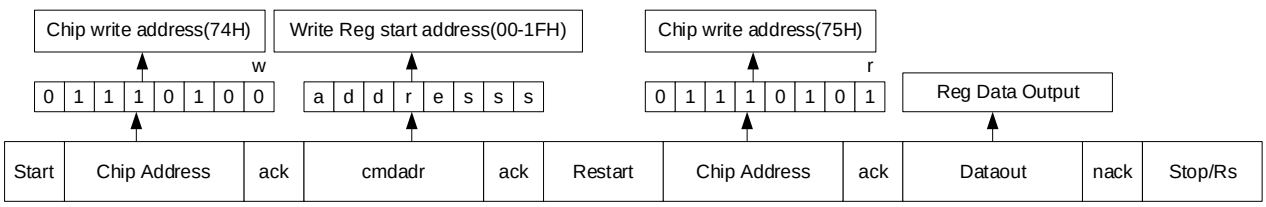


Figure 4. Register Read Mode (Single Read)

- Start = Start Conditions
- Chip Address = Write register address =0111010 + 0(w) b
- ack = Acknowledge from ET61934

- Write Reg start address byte= cmdadr (REG's 8bit address)
- ack = Acknowledge from ET61934
- Restart =Restart condition
- Chip Address = Read register address=0111010+1(r) bits
- ack = Acknowledge from ET61934
- Dataout = Register Data Output
- No response bit=nack (return from master)
- Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol (Continuous Read):

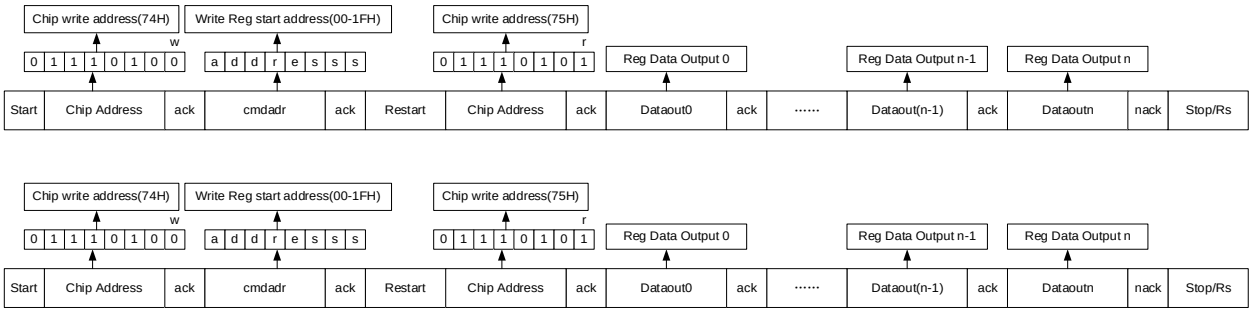


Figure 5. Register Read Mode (Continuous Read)

- Start=Start Conditions
- Chip address =Write register address=0111010+0(w) b
- ack = Acknowledge from ET61934
- Write Reg start address byte= cmdadr (REG's 8bit address)
- ack = Acknowledge from ET61934
- Restart =Restart condition
- Chip Address = Read register address=0111010+1(r) bits
- ack = Acknowledge from ET61934
- Dataout0 = Register Data Output 0
- ack = Acknowledge from Host
- ……
- Dataoutn = Register Data Output n
- nack = No Acknowledge from Host
- Stop/Rs=Stop Condition/Restart Condition

Register Definition

Table1. Registers Definition

Addr	Name	Description			
00H	CONTROL1	soft_reset=11011b effective		osc_clk_sel[1:0]	chip_en
01H	CONTROL2	000b		scan_line_sel[2:0]	chg_line_time[1:0]
02H	CONTROL3	chipid=0110		shadow_cs[1:0]	shadow_sw[1:0]
03H	CONTROL4	00b	glb_max_cur_sel[4:0]		dis_en
04H	CS_CUR_SEL1	cs4_cur[1:0]	cs3_cur[1:0]	cs2_cur[1:0]	cs1_cur[1:0]
05H	CS_CUR_SEL2	cs8_cur[1:0]	cs7_cur[1:0]	cs6_cur[1:0]	cs5_cur[1:0]
06H	CS_CUR_SEL3	cs12_cur[1:0]	cs11_cur[1:0]	cs10_cur[1:0]	cs9_cur[1:0]
07H	CS_CUR_SEL4	cs16_cur[1:0]	cs15_cur[1:0]	cs14_cur[1:0]	cs13_cur[1:0]
10H	SW1_CSH8	SW1 corresponds to the high 8 bit display data of CS16 to CS9			
11H	SW1_CSL8	SW1 corresponds to the lower 8 bits of data displayed by CS8 to CS1			
12H	SW2_CSH8	SW2 corresponds to the high 8-bit display data of CS16 to CS9			
13H	SW2_CSL8	SW2 corresponds to the lower 8 bits of CS8 to CS1 for displaying data			
14H	SW3_CSH8	SW3 corresponds to the high 8-bit display data of CS16 to CS9			
15H	SW3_CSL8	SW3 corresponds to the lower 8 bits of CS8 to CS1 for displaying data			
16H	SW4_CSH8	SW4 corresponds to the high 8-bit display data of CS16 to CS9.			
17H	SW4_CSL8	SW4 corresponds to the low 8-bit display data of CS8 to CS1.			
18H	SW5_CSH8	SW5 corresponds to the high 8-bit display data of CS16 to CS9.			
19H	SW5_CSL8	SW5 corresponds to the low 8-bit display data of CS8 to CS1.			
1AH	SW6_CSH8	SW6 corresponds to the high 8-bit display data of CS16 to CS9.			
1BH	SW6_CSL8	SW6 corresponds to the lower 8 bits of CS8 to CS1 for displaying data			
1CH	SW7_CSH8	SW7 corresponds to the high 8-bit display data of CS16 to CS9.			
1DH	SW7_CSL8	SW7 corresponds to the low 8 bits of the display data for CS8 to CS1.			
1EH	SW8_CSH8	SW8 corresponds to the high 8-bit display data of CS16 to CS9.			
1FH	SW8_CSL8	SW8 corresponds to the low 8 bits of the display data for CS8 to CS1.			

Table2. CONTROL1 Register

CONTROL Register 1						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
00H	7:3	sw_reset	00000b	R/W	Software Reset Command	
					11011b	Reset reg00H~1FH
					Other	-
	2:1	osc_clk_sel	00b	R/W	Oscillator frequency Selection	
					00	1M
					01	2M
					10	4M
					11	8M
	0	chip_en	0b	R/W	Chip Enable Signal	

					0	Disable the IC
					1	Enable the IC

Note: chip_en=0, all the analog circuit will be shutdown, the current consumption will be lowest.

Table3. CONTROL2 Register

Control Register 2						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
01H	7:5	-	000	-	Reserved	
	4:2	scan_line_sel	111	W/R	SW port scan row settings	
					111	8 scans (default)
					……	……
					100	5 scans
					……	……
					001	2 scans
					000	1 scan
	1:0	chg_line_time	00	W/R	00	4 PWM cycles
					01	8 PWM cycles
					10	12 PWM cycles
					11	16 PWM cycles

Table4. CONTROL3 Register

control Register 3						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
02H	7:4	chipid	0110	R	slug ID	
	3:2	shadow_cs	01	W/R	CS port deactivation	
					00	Hide and Close
					01	weak elimination
					10	consumptive stasis
					11	strong elimination
	1:0	shadow_sw	00	W/R	SW port blackout	
					00/01	Hide and Close
					10	weak elimination
					11	strong elimination

Table5. CONTROL4 Register

Control Register 4						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
03H	7:6	-	000	-	Reserved	
	5:1	glb_max_cur_sel	01111	W/R	The continuous output current Ics (n=1~16) from the CSn port	
					11111	50mA

					11110	48.75mA
					……	……
					01111	30mA (default)
					……	……
					00001	13.2mA
					00000	12mA
	0	dis_en	0	W/R	0	Enable display switch
					1	Enable display

Table6. CS_CUR_SEL1 Register

CS4~CS1 Channel Current Selection Registers						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
04H	7:6	cs4_cur[1:0]	11b	R/W	CS4 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	5:4	cs3_cur[1:0]	11b	R/W	CS3 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	3:2	cs2_cur[1:0]	11b	R/W	CS2 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	1:0	cs1_cur[1:0]	11b	R/W	CS1 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current

Table7. CS_CUR_SEL2 Register

CS8~CS5 Channel Current Selection Registers						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
05H	7:6	cs8_cur[1:0]	11b	R/W	CS8 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current

	5:4	cs7_cur[1:0]	11b	R/W	CS7 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	3:2	cs6_cur[1:0]	11b	R/W	CS6 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	1:0	cs5_cur[1:0]	11b	R/W	CS5 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current

Table8. CS_CUR_SEL3 Register

CS12~CS9 Channel Current Selection Registers						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
06H	7:6	cs12_cur[1:0]	11b	R/W	CS12 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	5:4	cs11_cur[1:0]	11b	R/W	CS11 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	3:2	cs10_cur[1:0]	11b	R/W	CS10 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	1:0	cs9_cur[1:0]	11b	R/W	CS9 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current

Table9. CS_CUR_SEL4 Register

CS16~CS13 Channel Current Selection Registers						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
07H	7:6	cs16_cur[1:0]	11b	R/W	CS16 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	5:4	cs15_cur[1:0]	11b	R/W	CS15 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	3:2	cs14_cur[1:0]	11b	R/W	CS14 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	1:0	cs13_cur[1:0]	11b	R/W	CS13 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current

Table10. SWn_CSH8 Register

SWn_CSH8 Registers（n=1~8）						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
10H， 12H， 14H， 16H， 18H， 1AH， 1CH， 1EH；	7	SWn_CS16	0	R/W	1:LED ON	0:LED OFF
	6	SWn_CS15	0	R/W	1:LED ON	0:LED OFF
	5	SWn_CS14	0	R/W	1:LED ON	0:LED OFF
	4	SWn_CS13	0	R/W	1:LED ON	0:LED OFF
	3	SWn_CS12	0	R/W	1:LED ON	0:LED OFF
	2	SWn_CS11	0	R/W	1:LED ON	0:LED OFF
	1	SWn_CS10	0	R/W	1:LED ON	0:LED OFF
	0	SWn_CS9	0	R/W	1:LED ON	0:LED OFF

Note: Registers 10H,12H,14H,16H,18H,1AH, 1CH, and 1EH correspond to SW1, SW2, SW3, SW4, SW5, SW6, SW7, and SW8 respectively.

Table11. SWn_CSL8 Register

SWn_CSL8 Registers (n=1~8)						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
11H,	7	SWn_CS8	0	R/W	1:LED ON	0:LED OFF
13H,	6	SWn_CS7	0	R/W	1:LED ON	0:LED OFF
15H,	5	SWn_CS6	0	R/W	1:LED ON	0:LED OFF
17H,	4	SWn_CS5	0	R/W	1:LED ON	0:LED OFF
19H,	3	SWn_CS4	0	R/W	1:LED ON	0:LED OFF
1BH,	2	SWn_CS3	0	R/W	1:LED ON	0:LED OFF
1DH,	1	SWn_CS2	0	R/W	1:LED ON	0:LED OFF
1FH,	0	SWn_CS1	0	R/W	1:LED ON	0:LED OFF

Note: Registers 11H,13H,15H,17H,19H,1BH, 1DH, and 1FH correspond to SW1, SW2, SW3, SW4, SW5, SW6, SW7, and SW8 respectively.

LED Dot Matrix Diagram

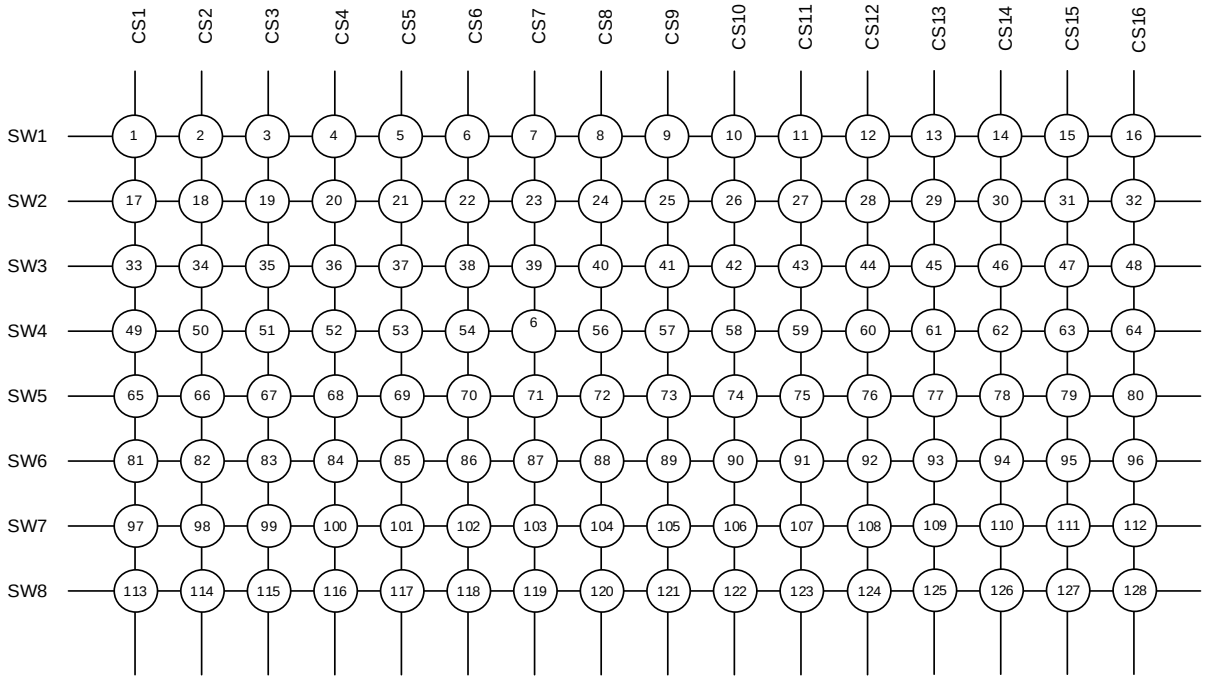


Figure 6. LED Dot Matrix Diagram

Notes:

1. The LED matrix mapping and display data correspondence are as follows:

2. In the diagram, LED 1 (SW1_CS1) displays data 11H[0], while LED 16 (SW1_CS16) shows data 10H[7].

3. In the diagram, LED 128 (SW8_CS16) displays data 1EH[7].

4. After powering on, configure the 00 register first to enable other registers. When the chip is in power-off state, no writes are allowed to other registers. The soft reset instruction should be executed after disabling the chip's enable. This will reset all control registers and PWM data registers to their default values.

Display Period Waveform

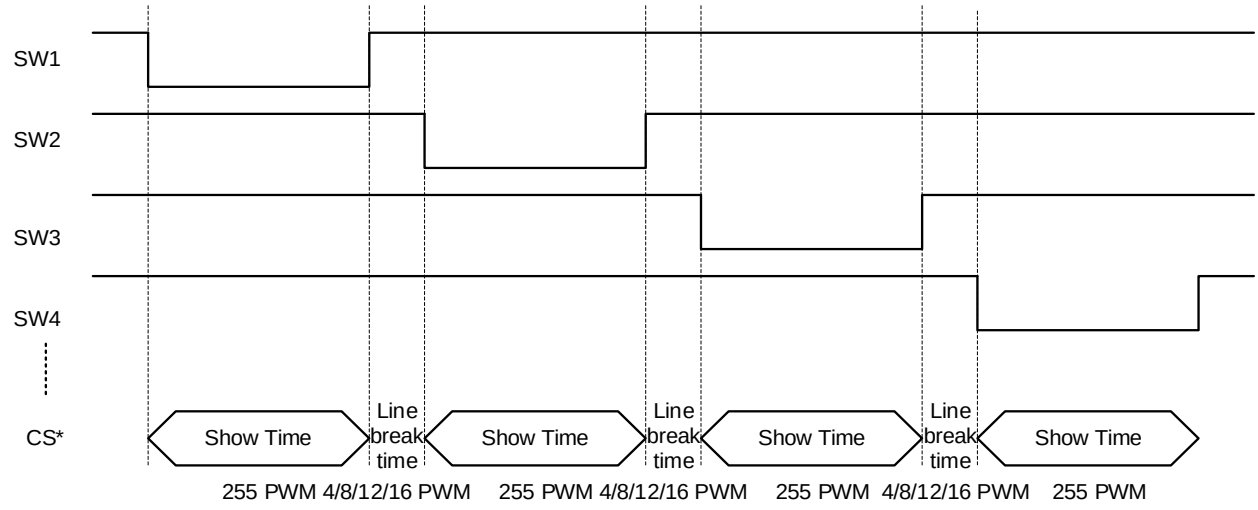


Figure 7. Data Display Period Waveform

Note: Display period: scan lines × (line change time (4/8/12/16 PWM cycles) + display time (255-level PWM cycles)) ; 1 PWM cycle = Tosc_clk.

Absolute Maximum Ratings

symbol	Characteristic	Rating	unit
V_{DD}	logic power supply voltage	-0.5 ~ 6.0	V
P_D	power consumption	1200	mW
T_J	maximum-junction temperature	-40 ~ 150	°C
T_{STG}	storage temperature	-65 ~ 150	°C

Recommended Operating Conditions

(TA = -40 to +85°C, GND = 0V)

symbol	Characteristic	Min	Typ	Max	unit
V_{DD}	logic power supply voltage	4.5	5.0	5.5	V
T_A	working temperature	-40		85	°C
V_{IH}	high level input voltage	2.4	-	V_{DD}	V
V_{IL}	low level input voltage	0	-	0.6	V

Electrical Characteristics

(unless otherwise specified: TA = 25°C, VDD = 5V, GND = 0V)

symbol	Characteristic	Test Condition	Min	Typ	Max	Unit
I_{CS_max}	Maximum constant current output	CSn；VCSn=4V(n=1~16) csn_cur [1:0]=11b(n=1~16) glb_max_cur_sel [4:0]=11111b SWn_CS1~16=1b(n=1~8)		50		mA
$I_{CS\_default}$	Default constant current output	CSn；VCSn=4V(n=1~16) csn_cur [1:0]=11b(n=1~16) glb_max_cur_sel [4:0]=01111b SWn_CS1~16=1b(n=1~8)		30		mA
I_{SW}	SW port output current	VSWn=0.5V(n=1~8)		800		mA
I_{IN}	input current	VI=VDD， SDA，SCL			±1	uA
V_{IH}	High level input voltage	SDA，SCL	2.4			V
V_{IL}	Low level input voltage	SDA，SCL			0.6	V
V_{OL_SDA}	SDA output low level	IOUT=3mA			0.4	V
I_{DD}	Quiescent current	Display off when no load		2	5	mA
I_{SLEEP}	Sleep current	SCL=SDA=VDD or GND REG00[0]=chip_en=0			5	uA

AC Characteristics

(unless otherwise specified: TA=25°C, VDD=5V, GND=0V)

symbol	Characteristic	condition	Min	Typ	Max	Unit
$t_{DISPLAY}$	display time	Display open, osc_clk_sel=00		255		us
t_{CHG_LINE}	Line break time	Display open, scan_chg_line=00, osc_clk_sel=00		4		us

I²C Timing Specifications

(unless otherwise specified, TA = 25°C, VDD = 5V, GND = 0V)

symbol	Parameter name	minimum	typical case	maximum	unit
F_{SCL}	SCL Clock Frequency	0	-	400	KHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	1.3	-	-	μs
$t_{HD:STA}$	Hold Time(Repeated) START Condition	0.6	-	-	μs
t_{LOW}	Low Period of SCL Clock	1.3	-	-	μs
t_{HIGH}	HIGH Period of SCL Clock	0.6	-	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	0.6	-	-	μs
$t_{HD:DAT}$	Data Hold Time	0.1	-	-	μs
$t_{SU:DAT}$	Data Setup Time	100	-	-	ns
t_R	Data Hold Time2		20+0.1Cb(1)	300	ns
t_F	Data Hold Time2		20+0.1Cb	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	0.6	-	-	μs

Note1: Cb=total capacitance of one bus line in PF unit.

I²C Timing Waveform

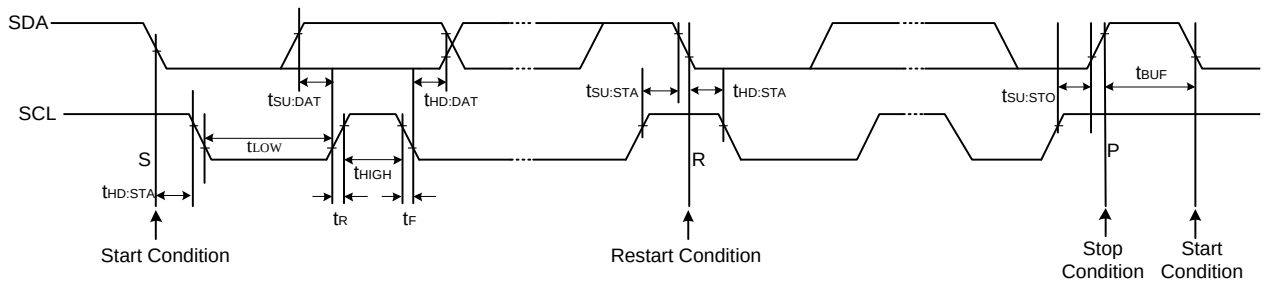


Figure 8. I²C Timing Waveform

Application Circuit

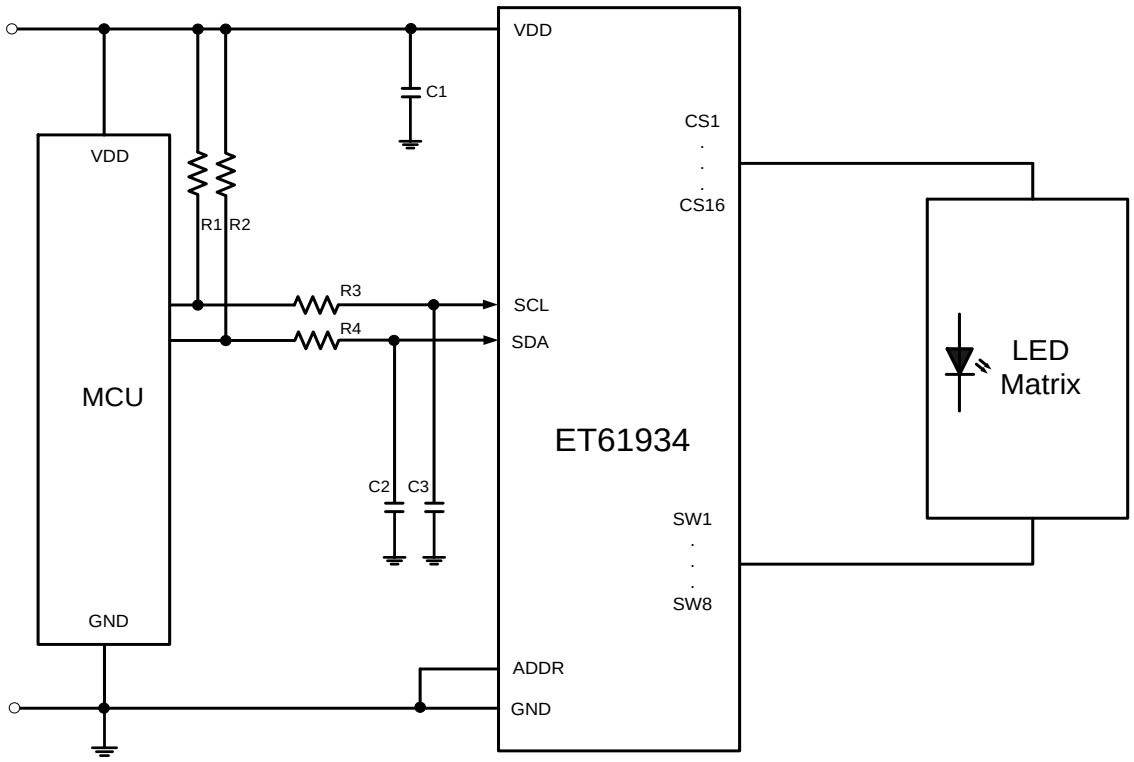


Figure 9. Application Circuit

Note: The application diagram is for reference only.

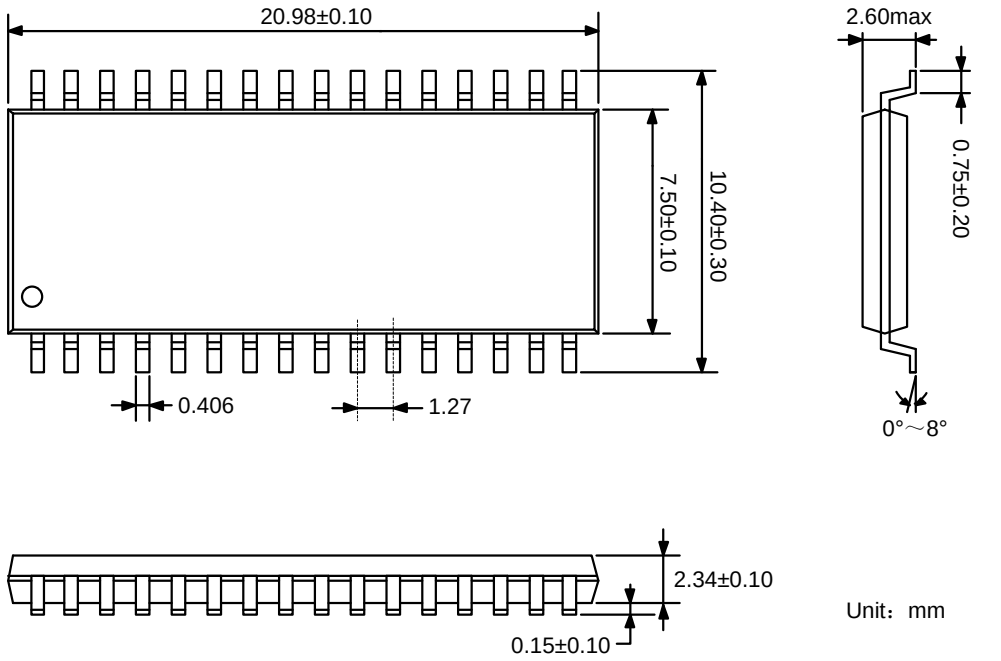
1. C1 should have a capacitance of at least 1μF, and the filter capacitor C1 should be placed as close as possible to VDD.

2. R1~R2 = 4.7kΩ, R3~R4 = 100Ω, C2~C3 = 100pF;

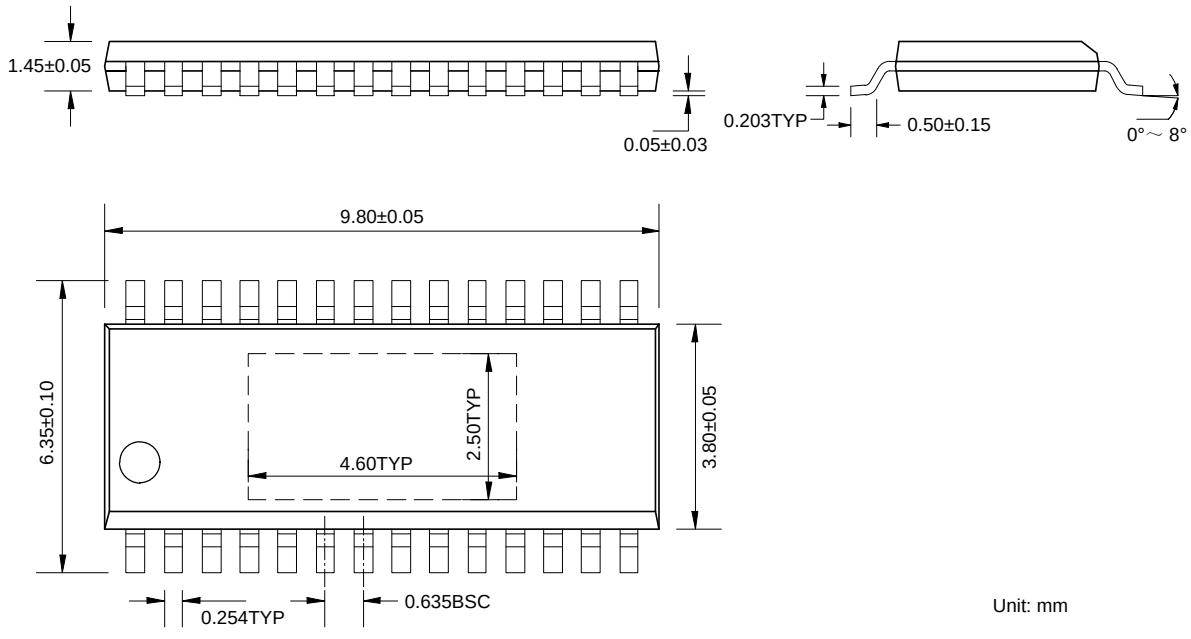
3. Place the series resistor and GND capacitor as close as possible to the ET61934 on the communication port. The resistance and capacitance values can be adjusted based on actual anti-interference requirements and test results.

Package Dimension

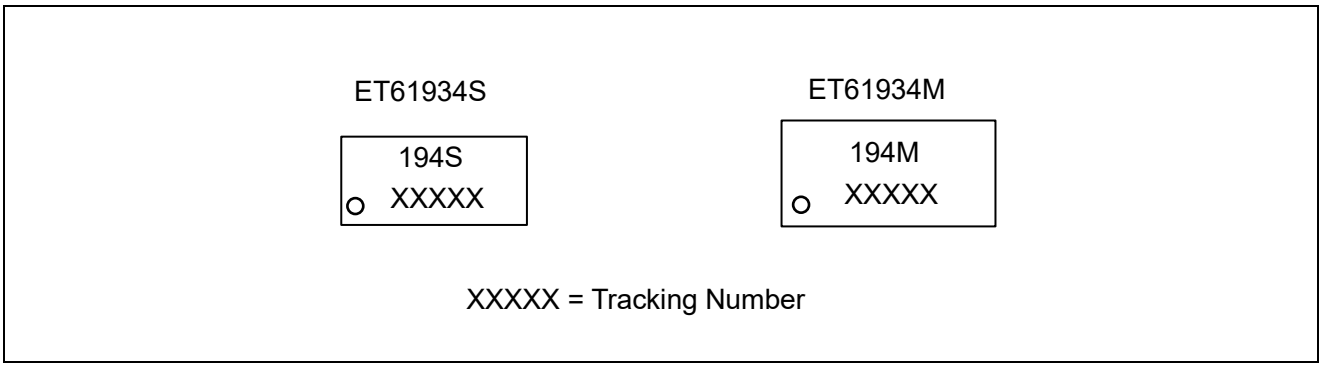
SOP32



EQSOP28



Marking



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-01-21	Official Version	Wangli	Licx	Liujy