



1A Ultra-Low Noise, High PSRR LDO for RF and Analog Circuits

General Description

The ET5A8XXYB series of low-dropout, low-power linear regulators offer up to 1000mA with PMOS pass transistor. The device offers low noise, high PSRR, low quiescent current and very good line/load transients, suitable for RF applications and analog circuits.

The ET5A8XXYB is stable with a 1 μ F input and 1 μ F ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve accuracy of 1.5%.

It is in small DFN6 (2.0mm \times 2.0mm) package, which is ideal for small form factor portable equipment such as wireless handsets and PDAs.

Features

- Wide Input Voltage Range from 1.9V~5.5V
- Output Voltage: 1.8V, 2.5V, 2.8V, 3.0V, 3.3V and etc.
- Output Current up to 1A
- Very Low I_Q of 25 μ A Typical
- Shutdown Current of 0.1 μ A Typical
- Low Dropout Are Typical 280mV at 1A, 3.0V output
- Ultra-low Noise Are Typical 10 μ Vrms ($I_{OUT} = 200mA$) @ $V_{OUT} = 3V$
- Very High PSRR Are 90dB at 1kHz, 42dB at 1MHz @ $V_{OUT} = 3V$
- Excellent Line/Load Transient Response
- Built-in ILIMIT Protection and Thermal Shutdown Circuit
- Built-in Auto Discharge Function
- Part No. and Package Information

| Part No. | Package | Packing Option | MSL |
|-----------|-----------------------------|------------------------|-----|
| ET5A8XXYB | DFN6 (2.0mm \times 2.0mm) | Tape and Reel, 3K/Reel | 1 |

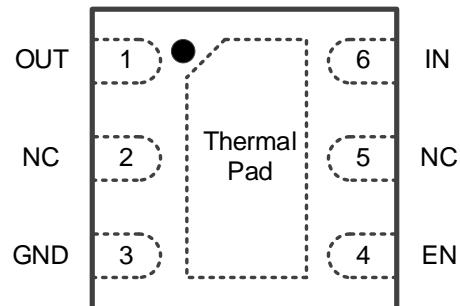
* XX=X.XV, For example, ET5A830YB is 3.0V VOUT Version.

Applications

- Smart Phones and Cellular Phones
- PDAs
- Digital Still Cameras
- Portable Instrument

ET5A8XXYB

Pin Configuration



DFN6 Top View

Figure1. Pin Configuration

Pin Function

| Pin No. | Pin Name | Pin Description |
|---------|-------------|---|
| 1 | OUT | Output pin. A 1 μ F low-ESR capacitor should be connected to this pin to ground. |
| 2, 5 | NC | No connect |
| 3 | GND | Ground |
| 4 | EN | Enable control input, active high. Do not leave EN floating |
| 6 | IN | Supply input pin. Must be closely decoupled to GND with a 1 μ F ceramic capacitor |
| - | Thermal Pad | Thermal Pad, connect to GND plane for better power dissipation |

ET5A8XXYB

Block Diagram

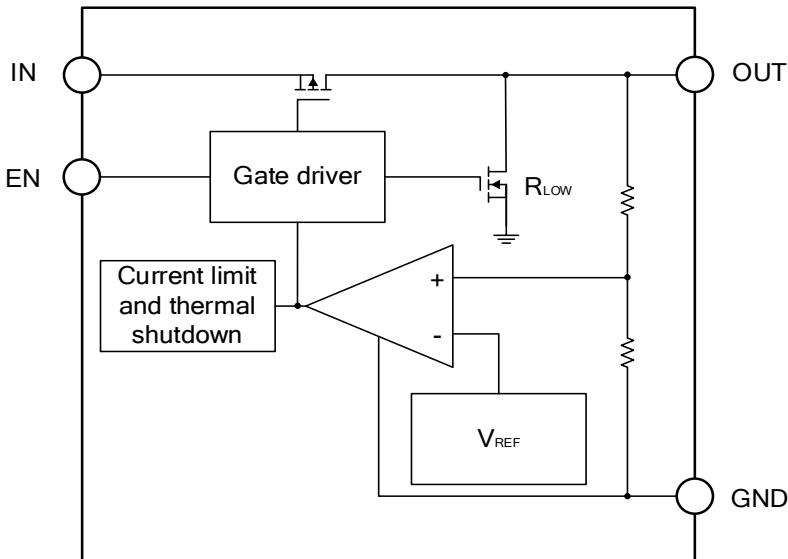


Figure2. Block Diagram

Functional Description

Input Capacitor

A 1 μ F ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 μ F to 10 μ F, Equivalent Series Resistance (ESR) is from 5m Ω to 100m Ω , and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins. With a reasonable PCB layout, the single 1 μ F ceramic output capacitor can be placed up to 10cm away from the ET5A8XXYB device.

Remote Output Capacitor Placement

The ET5A8XXYB requires at least a 1 μ F capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10cm away from the LDO.

Low Quiescent Current

The ET5A8XXYB, consuming only 25 μ A quiescent current, provides great power saving in portable and low power applications.

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On/Off Input Operation

The ET5A8XXYB is turned on by setting the EN pin higher than V_{IH} threshold, and is turned off by pulling it lower than V_{IL} threshold. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time.

During soft-start time, in order to achieve a rapid increase in output voltage to reach the set value, the ET5A8XXYB will short-circuit the filter resistor for approximately 0.5ms. Therefore, it is required that V_{IN} be greater than V_{OUT} set value within 0.5ms upon enable or be established completely before the enable signal is issued.

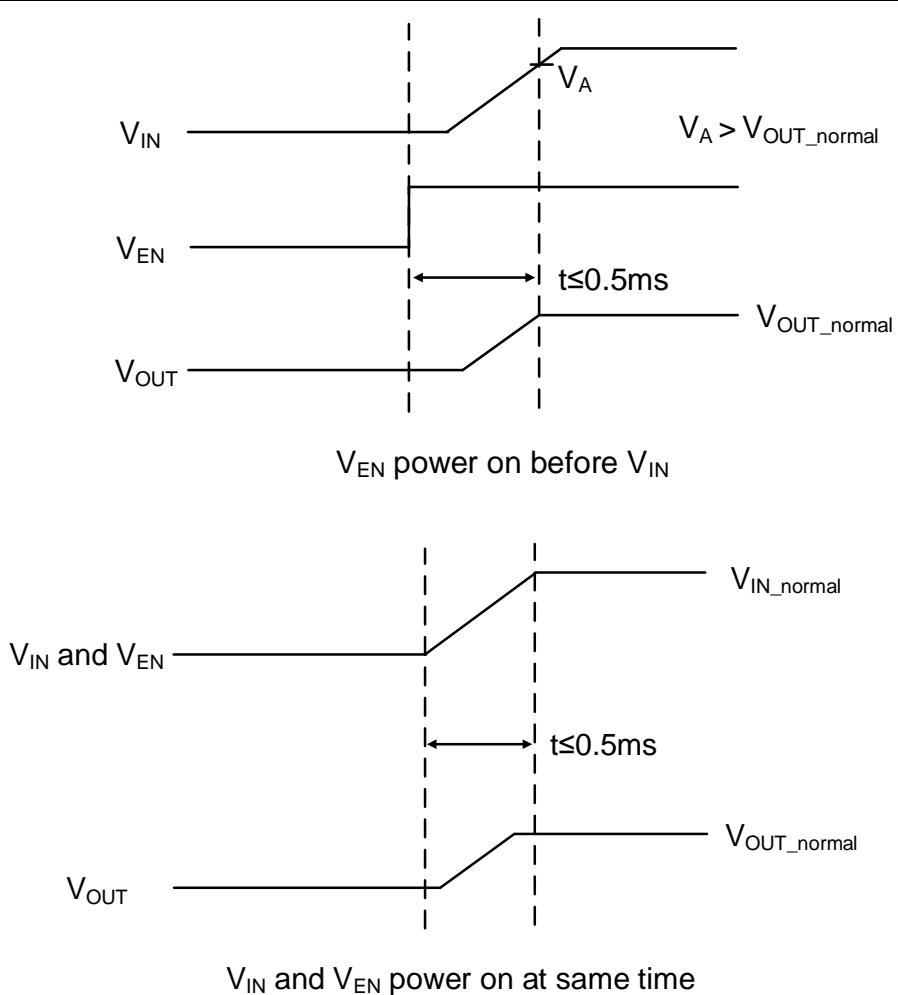


Figure3. On/Off Input Operation

High PSRR and Low Noise

The ET5A8XXYB, with PSRR of 90dB at 1KHz. It is suitable for most of these applications that require high PSRR and low noise.

Fast Transient Response

The ET5A8XXYBs fast transient response from 0 to 1A provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

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Dropout Voltage

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage. The ET5A8XXYB internal circuitry is not fully functional until V_{IN} is at least 1.9V. The output voltage is not regulated until V_{IN} has reached at least the greater of ($V_{OUT} + V_{DROP}$).

Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuiting to GND, the current limit protection will be triggered and clamp the output current to approximately 1.5A to prevent over-current and to protect the regulator from damage due to overheating.

Output Automatic Discharge

The ET5A8XXYB output employs an internal 90 Ω (typical) pull-down resistance to discharge the output when the EN pin is low, and the device is disabled.

Thermal Overload Protection

Thermal shutdown disables the output when the junction temperature rises to approximately 155°C which allows the device to cool. When the junction temperature cools to approximately 130°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the ET5A8XXYB has been designed to protect against temporary thermal overload conditions. The TSD circuitry was not intended to replace proper heat-sinking. Continuously running the ET5A8XXYB device into thermal shutdown may degrade device reliability.

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Absolute Maximum Ratings

| Symbol | Item | | Rating | Unit |
|------------|--|------|------------------------|------|
| V_{IN} | IN Voltage | | -0.3 to 6.0 | V |
| V_{EN} | Input Voltage (EN Pin) | | -0.3 to 6.0 | V |
| V_{OUT} | Output Voltage | | -0.3 to $V_{IN} + 0.3$ | V |
| P_D | Maximum Power Consumption ⁽¹⁾ | DFN6 | 1200 | mW |
| I_{MAX} | Maximum Load Current | | 1000 | mA |
| T_J | Operating Junction Temperature | | -40 to 150 | °C |
| T_{STG} | Storage Temperature | | -65 to 150 | °C |
| T_{SLOD} | Lead Temperature (Soldering, 10 sec) | | 260 | °C |
| V_{ESD} | HBM (JEDEC JS-001) | | ± 2000 | V |
| | CDM (JEDEC JS-002) | | ± 500 | V |

Note1: Rating at mounting on a board (PCB board dimension: 40mm × 40mm (4layer), copper: 1OZ).

Recommended Operating Conditions

| Symbol | Item | Rating | Unit |
|-----------|---|------------|------|
| V_{IN} | Input Voltage ⁽²⁾ | 1.9 to 5.5 | V |
| I_{OUT} | Output Current | 1 to 1000 | mA |
| T_A | Operating Ambient Temperature | -40 to 85 | °C |
| C_{IN} | Effective Input Ceramic Capacitor Value | 0.68 to 10 | µF |
| C_{OUT} | Effective Output Ceramic Capacitor Value | 0.68 to 10 | µF |
| ESR | Input and Output Capacitor Equivalent Series Resistance (ESR) | 5 to 100 | mΩ |

Note2: In order to achieve high performance of PSRR, it is recommended that the V_{IN} needs to be no smaller than $(V_{OUT} + 0.5V)$.

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Electrical Characteristics

($V_{EN} = V_{IN} = V_{OUT} + 1V$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$. Typical values are at $T_A = 25^\circ C$, unless otherwise stated)

| Symbol | Parameters | Test Conditions | Min | Typ | Max | Unit |
|---------------------|--|---|------------------|------|-----|---------------|
| $V_{IN}^{(2)}$ | Input Voltage Range | | 1.9 | | 5.5 | V |
| V_{OUT} | Output Voltage Accuracy | $V_{IN} = V_{OUT(NOM)} + 1V$, $I_{OUT} = 1mA$, $-40^\circ C < T_A < 85^\circ C$ | -1.5 | | 1.5 | % |
| I_{LOAD} | Load Current | | 1000 | | | mA |
| V_{DROP} | Dropout Voltage | $I_{OUT} = 500mA$ | $V_{OUT} = 3.0V$ | 130 | 190 | mV |
| | | | $V_{OUT} = 3.3V$ | 110 | 170 | |
| | | $I_{OUT} = 1000mA$ | $V_{OUT} = 3.0V$ | 280 | 390 | |
| | | | $V_{OUT} = 3.3V$ | 260 | 370 | |
| Reg_{LINE} | Line Regulation | $V_{IN} = V_{OUT} + 1V$ to $5.5V$, $I_{OUT} = 1mA$ | | 0.01 | 0.1 | %/V |
| Reg_{LOAD} | Load Regulation | $V_{IN} = V_{OUT} + 0.5V$, $I_{OUT} = 1mA$ to $1000mA$ | | 50 | 70 | mV |
| I_{Q_ON} | Input Quiescent Current | $I_{OUT} = 0mA$ | | 25 | 35 | μA |
| I_{Q_OFF} | Input Shutdown Quiescent Current | $V_{EN} = 0V$ | | 0.1 | 1 | μA |
| I_{LIMIT} | Current Limit | $T_A = 25^\circ C$ | 1.05 | 1.5 | 2.0 | A |
| I_{SHORT} | Short Current Limit | $V_{OUT} = 0V$, $T_A = 25^\circ C$ | 450 | 650 | 850 | mA |
| $PSRR^{(3)}$ | Power Supply Rejection Ratio $V_{OUT} = 3.0V$ | $f = 100Hz$, $I_{OUT} = 20mA$ | | 90 | | dB |
| | | $f = 1kHz$, $I_{OUT} = 20mA$ | | 90 | | dB |
| | | $f = 100kHz$, $I_{OUT} = 20mA$ | | 60 | | dB |
| | | $f = 1MHz$, $I_{OUT} = 20mA$ | | 42 | | dB |
| $e_N^{(3)}$ | Output Noise Voltage $V_{OUT} = 3.0V$ | BW=10 Hz to 100kHz, $I_{OUT} = 1mA$ | | 13 | | μV_{RMS} |
| | | BW=10 Hz to 100kHz, $I_{OUT} = 200mA$ | | 10 | | μV_{RMS} |
| V_{IH} | EN Input Logic High Voltage | $V_{IN} = 5.5V$, $I_{OUT} = 1mA$, V_{EN} Rising until the Output is Enabled | 0.84 | | | V |
| V_{IL} | EN Input Logic Low Voltage | $V_{IN} = 5.5V$, V_{EN} Falling until the Output is Disabled | | | 0.4 | V |
| I_{EN} | EN Input current | $V_{EN} = 0V$ to $5.5V$ | | 10 | | nA |
| R_{LOW} | Output Discharge FET Rdson | $V_{EN} < 0.4V$, $V_{OUT} = 3.0V$ | 70 | 90 | 120 | Ω |
| $V_{TRLN}^{(3)}$ | Line transient | $V_{IN} = V_{OUT} + 1V$ to $5.5V$ in $10\mu s$, $I_{OUT} = 1mA$, $T_A = 25^\circ C$ | | | +25 | mV |
| | | $V_{IN} = 5.5V$ to $V_{OUT} + 1V$ in $10\mu s$, $I_{OUT} = 1mA$ | -25 | | | mV |
| $V_{TRLD}^{(3)(4)}$ | Load transient | $I_{OUT} = 1mA$ to $1000mA$ in $10\mu s$ | | 50 | 70 | mV |
| | | $I_{OUT} = 1000mA$ to $1mA$ in $10\mu s$ | | 70 | 90 | mV |

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Electrical Characteristics (Continued)

($V_{EN} = V_{IN} = V_{OUT} + 1V$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$. Typical values are at $T_A = 25^\circ C$, unless otherwise stated)

| Symbol | Parameters | Test Conditions | Min | Typ | Max | Unit |
|------------|--|--|-----|-----|-----|------------|
| t_{ON} | Output Turn-on Time | From $V_{EN} > V_{IH}$ $V_{OUT} = 95\%$ of $V_{OUT(NOM)}$ | 300 | 500 | 700 | μs |
| T_{SHDN} | Thermal Shutdown threshold ⁽³⁾ | T_J rising | | 155 | | $^\circ C$ |
| T_{HYS} | Thermal Shutdown Hysteresis ⁽³⁾ | T_J Falling from Shutdown | | 25 | | $^\circ C$ |

Note3: Guaranteed by design and characterization. not a FT item.

Note4: Due to PD limitations, during the test of the SOT package circuit, $V_{IN} = V_{OUT} + 0.5V$.

Application Circuit

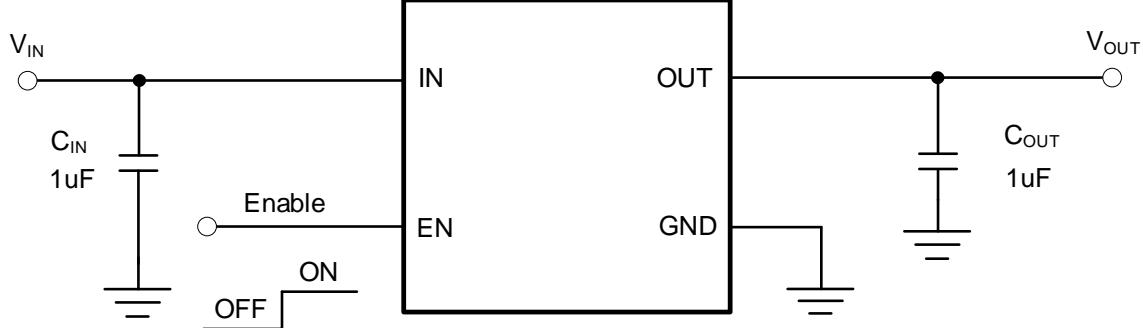
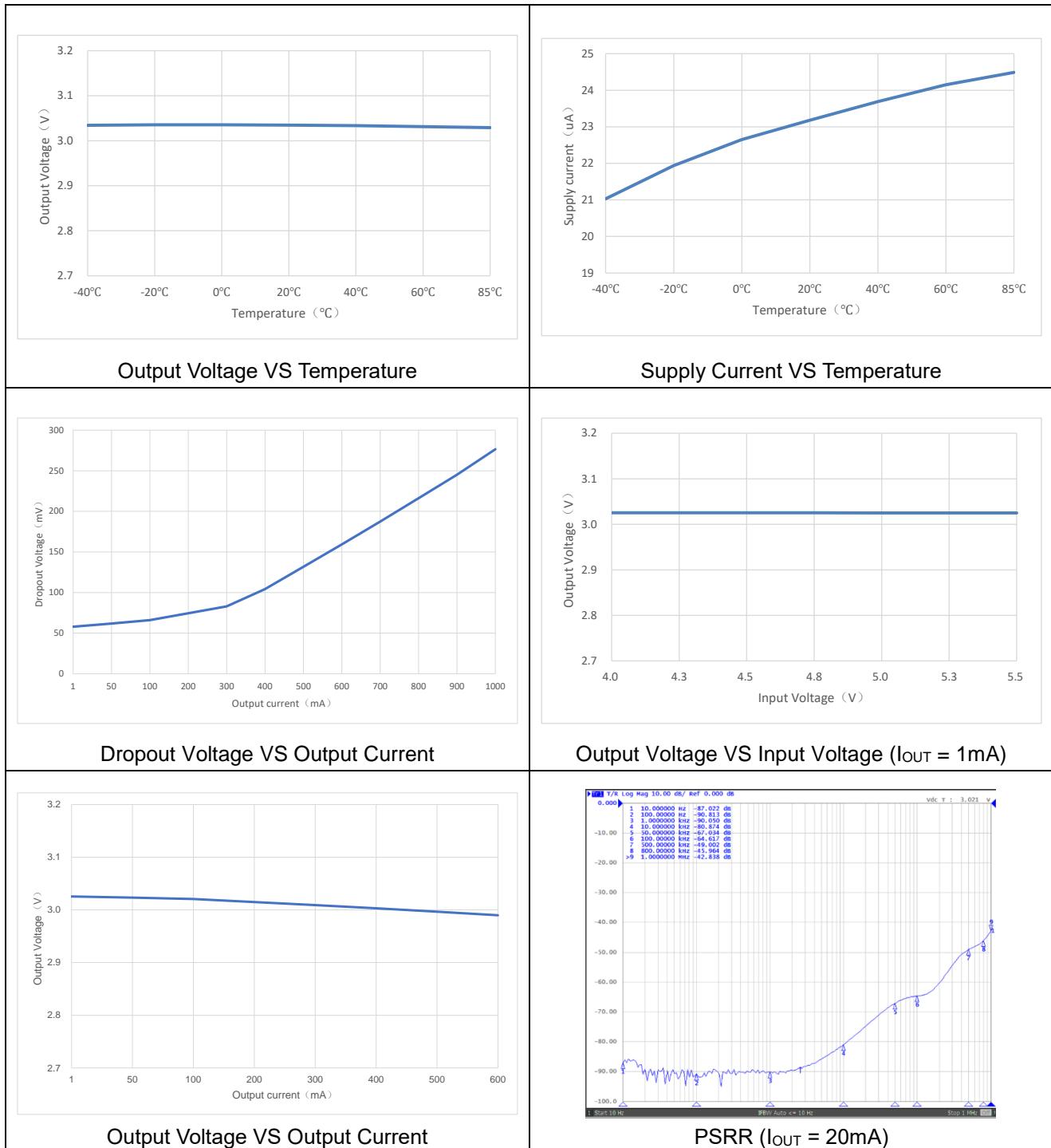


Figure4. Application Circuit

ET5A8XXYB

Typical Characteristics

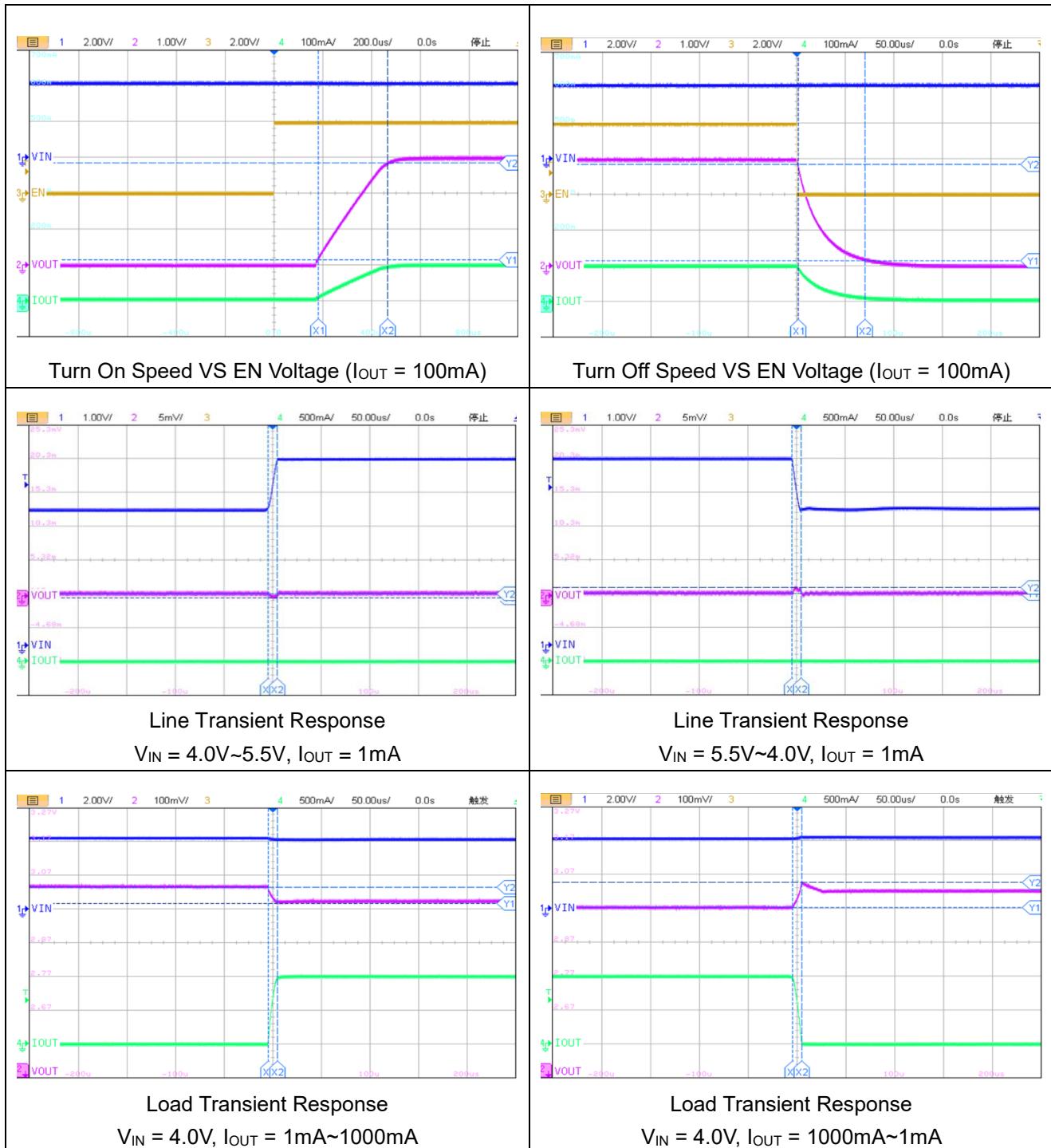
($V_{OUT} = 3.0V$, $V_{EN} = V_{IN} = V_{OUT} + 1V$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$. Typical values are at $T_A = 25^\circ C$, unless otherwise stated.)



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Typical Characteristics (Continued)

($V_{OUT} = 3.0V$, $V_{EN} = V_{IN} = V_{OUT} + 1V$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$. Typical values are at $T_A = 25^{\circ}C$, unless otherwise stated.)



ET5A8XXYB

Recommend PCB Layout

DFN6 (2mm x 2mm)

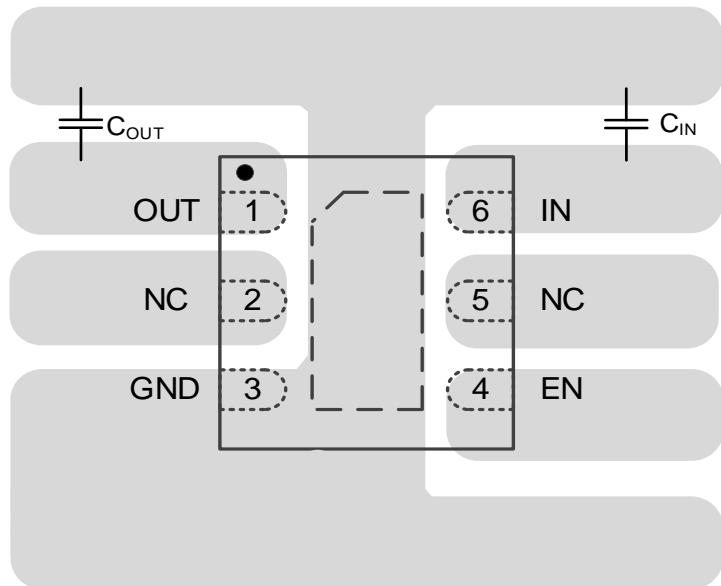
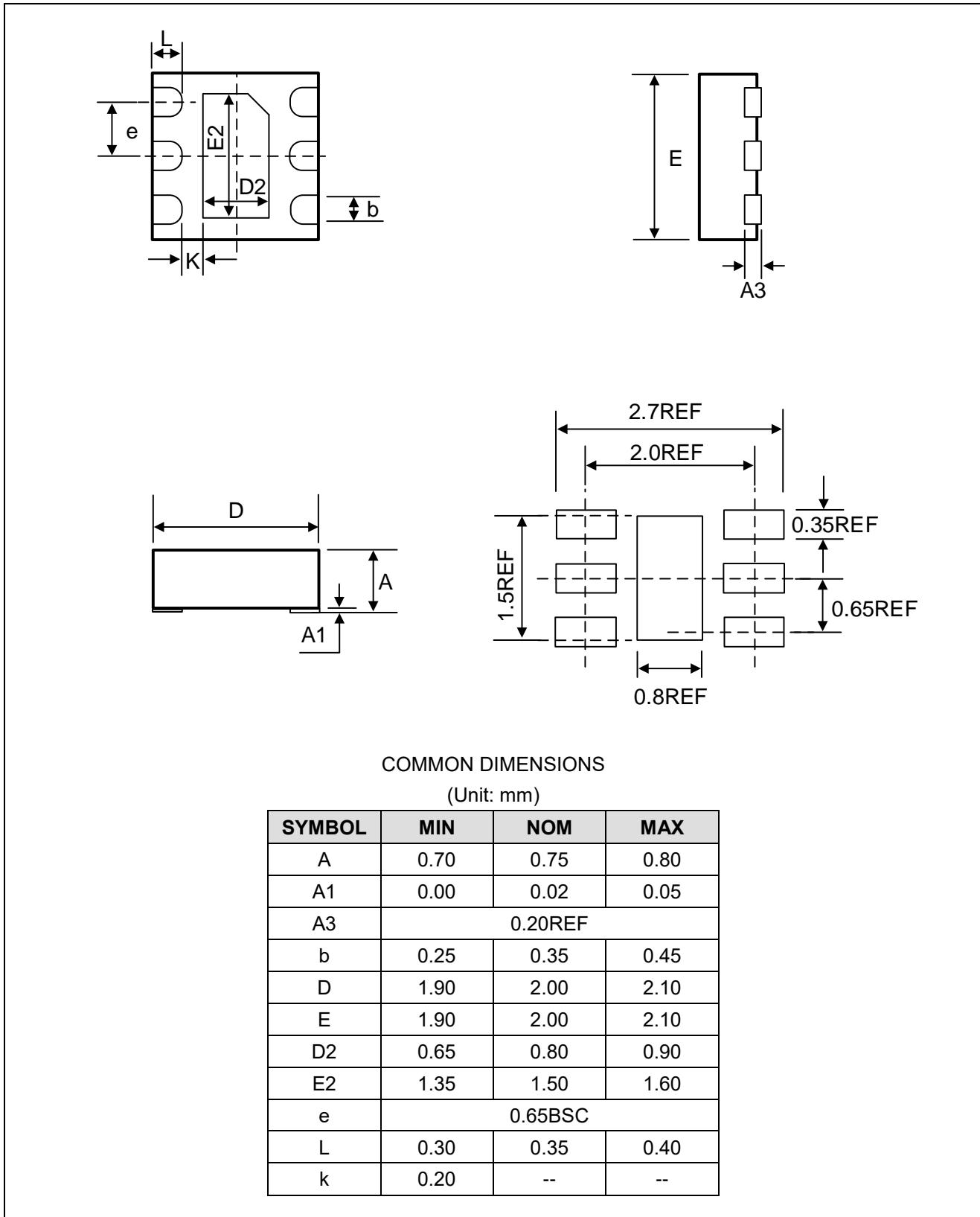


Figure5. Recommend PCB Layout

ET5A8XXYB

Package Dimension

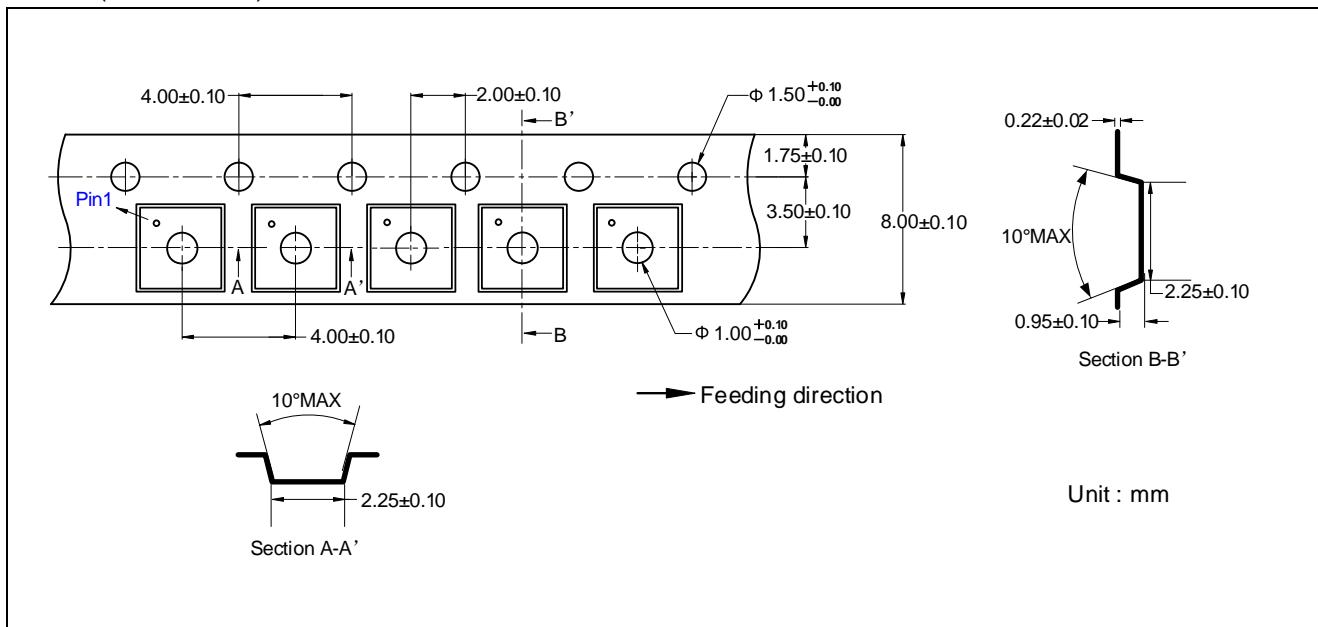
DFN6 (2mm x 2mm)



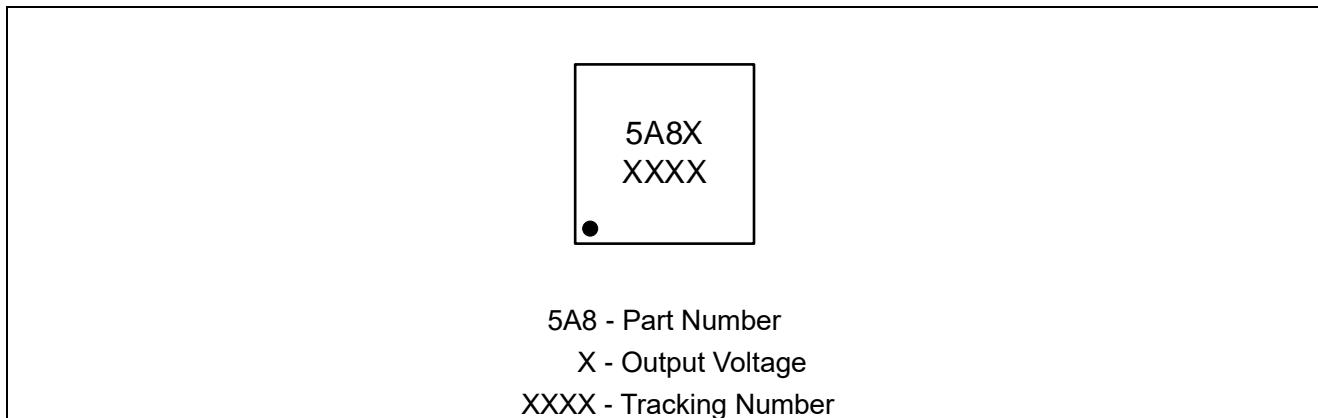
ET5A8XXYB

Tape Information

DFN6 (2mm x 2mm)



Marking Information



Revision History and Checking Table

| Version | Date | Revision Item | Modifier | Function & Spec Checking | Package & Tape Checking |
|---------|------------|---------------------|-------------|--------------------------|-------------------------|
| 0.1 | 2024-04-02 | Preliminary Version | Li huan | Liu yiguo | Liu jiaying |
| 0.2 | 2024-04-11 | Update Format | Wu junyan | Liu yiguo | Liu jiaying |
| 1.0 | 2025-08-07 | Official Version | Yang xiaoxu | Liu yiguo | Liu jiaying |
| 1.1 | 2025-10-09 | Update EC table | Yang xiaoxu | Liu yiguo | Liu jiaying |
| | | | | | |