High Input Voltage Ultra High PSRR 200mA LDO

General Description

ET52HS27ADJ is a high-performance, low dropout voltage linear regulator with adjustable voltage output from 0.5V to 16V. Adopting ultra-low noise and ultra-high PSRR architecture, it is very suitable for use in noise sensitive application circuits.

When providing an output current of 200mA, the dropout voltage is 350mV. The typical static operating current is 0.3mA, and it is less than 1μA in shutdown mode.

The ET52HS27ADJ has a wide output voltage range (0.5V to 16V) and provides excellent output noise while maintaining stable output PSRR, Bandwidth and load adjustment rate. In addition, the regulator also has programmable current limits, quick startup, and the ability to indicate output voltage regulation.

In practical applications, the ET52HS11 recommends using ceramic capacitors with a minimum of 4.7μF at the output pin to provide ultra-low noise performance and good circuit stability. It is equipped with various protection circuits, including over-current protection, internal foldback current limit protection, overheating limit protection, etc.

ET52HS27ADJ supports DFN10 (3mm × 3mm) and MSOP10 package, with a working junction temperature range of -40°C~125°C.

Features

- Wide Input Voltage Range from 2.4V~20V
- Output Current: 200mA
- Single Capacitor Improves Noise and PSRR
- Programmable Current Limit
- High Bandwidth: 1MHz
- Low Dropout are Typical 350mV at 200mA
- Output Voltage Regulation Range from 0.5V~16V(ADJ output)
- Quick Startup
- High-Precision Enable Control and Undervoltage-Lockout Function
- Internal Foldback Current Limit Protection
- Ultra-low noise: 1.6μVrms (Typical) @V_{OUT} = 3V, I_{OUT} = 10mA, 10Hz to 100kHz
- High power supply rejection ratio (PSRR)
  - -- 120dB @ 100Hz
  - -- 118dB @ 10kHz
  - -- 95dB @ 100kHz
  - -- 78dB @ 1MHz
  - -- 40dB @ 10MHz
- Configure Output Voltage through External Resistors

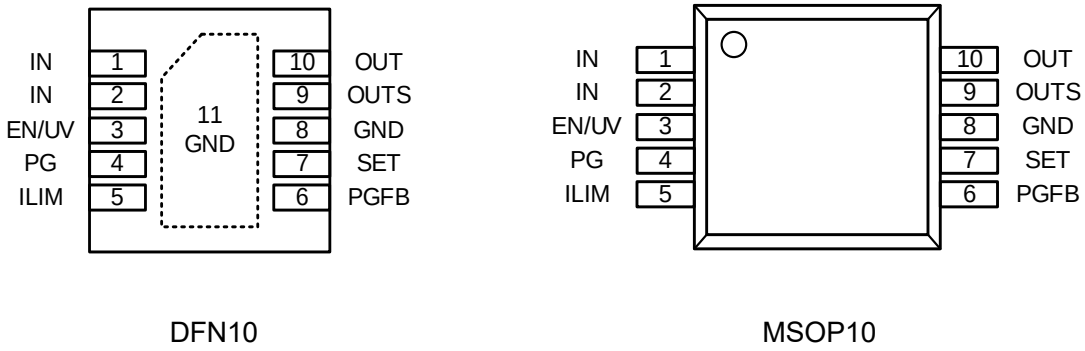
- Package Information:

Part No.	Package	MSL
ET52HS27ADJY	DFN10 (3mm × 3mm)	3
ET52HS27ADJM	MSOP10	3

Applications

- RF Power Supply: PLL, VCO, Mixer, Low-Noise Amplifier
- Ultra Low Noise Instrument
- High Speed/High-Precision Data Converter
- Medical Applications: Imaging, Diagnosis
- High Precision Power Supply

Pin Configuration



DFN10 MSOP10

Figure1. Pin Configuration

Pin Function

Pin No.	Pin Name	I/O	Function Description
1, 2	IN	I	**Input Voltage:** Voltage regulator power supply requires a bypass capacitor on the IN pin.
3	EN/UV	I	**Enable / Undervoltage Lockout:** Pulling the pin down to a low level can place the device in power down mode. The static current in power down mode decreases to below 1μA, and the output voltage is turned off. When EN/UV is connected to a high level (usually greater than 1.24V with a hysteresis of 100mV), the device is turned on. If soft shutdown is not required, EN/UV can be connected to IN. Do not float the EN/UV pin.
4	PG	O	**Power-Good Status Indicator:** It Indicates the open collector mark for output voltage regulation. If PGFB is below 300mV, PG is pulled to a low level. If the power-good status indication function is not required, hang the PG pin. There is a parasitic substrate diode between the PG and GND pins; During normal operation or in case of malfunction, do not drive PG to 0.3V lower than GND.

Pin Function (Continued)

Pin No.	Pin Name	I/O	Function Description
5	ILIM	I	**Current Limit Programming Pin:** Connecting a resistor between ILIM and GND can set the current limit. To achieve optimal accuracy, the resistor should be directly connected to the GND pin using a Kelvin connection method. It also serves as a current monitoring pin with a range of 0V to 300mV. If programmable current limiting function is not required, connect ILIM to GND. There is a parasitic substrate diode between the ILIM and GND pins; During normal operation or in case of malfunction, do not drive ILIM below GND by more than 0.3V.
6	PGFB	I	**Power-Good status feedback:** If PGFB increases to over 300mV on its rising edge and has a 10mV hysteresis on its falling edge, pull the PG pin to high level. By connecting an external resistive voltage divider between the OUT, PGFB, and GND pins, the following transfer function can be used to set the good state level of the programmable power supply: 0.3V × (1+R_{PGFB1}/R_{PGFB2}). PGFB is also responsible for activating the quick startup circuit. If good status indication and quick startup function are not required, connect PGFB to IN. If reverse input protection is required, connect the anode of 1N4148 diode to IN and its cathode to PGFB. There is a parasitic substrate diode between the PGFB and GND pins; During normal operation or in case of malfunction, do not drive OUT below GND by more than 0.3V.
7	SET	O	**SET Pin:** The inverting input of the error amplifier and the stabilizing set point of ET52HS27ADJ. Adding a capacitor between SET and GND can improve noise, PSRR, and transient response, but it will increase startup time. There is a parasitic substrate diode between the SET and GND pins; During normal operation or in case of malfunction, do not drive OUT below GND by more than 0.3V.
8	GND	-	**Ground Pin.**
9	OUTS	I	**Output Detection:** Connect to the in-phase input of the internal error amplifier. To achieve optimal transient and load adjustment performance, a Kelvin connection should be used to directly connect the OUTS to the load of the output capacitor. Moreover, connect the GND wires of the output capacitor and the SET pin capacitor directly together. In addition, during PCB design, the layout of input and output capacitors (and their GND connections) should be as close as possible. There is a parasitic substrate diode between the OUTS and GND pins; During normal operation or in case of malfunction, do not drive the OUTS below GND by more than 0.3V.
10	OUT	O	**Output:** Provide power to the load. To achieve stability, a 4.7μF (minimum value) output capacitor with ESR below 50mΩ and ESL below 1nH can be used. Large load transients require larger output capacitors to limit peak voltage transients. There is a parasitic substrate diode between the OUT and GND pins; During normal operation or in case of malfunction, do not drive OUT below GND by more than 0.3V.

Block Diagram

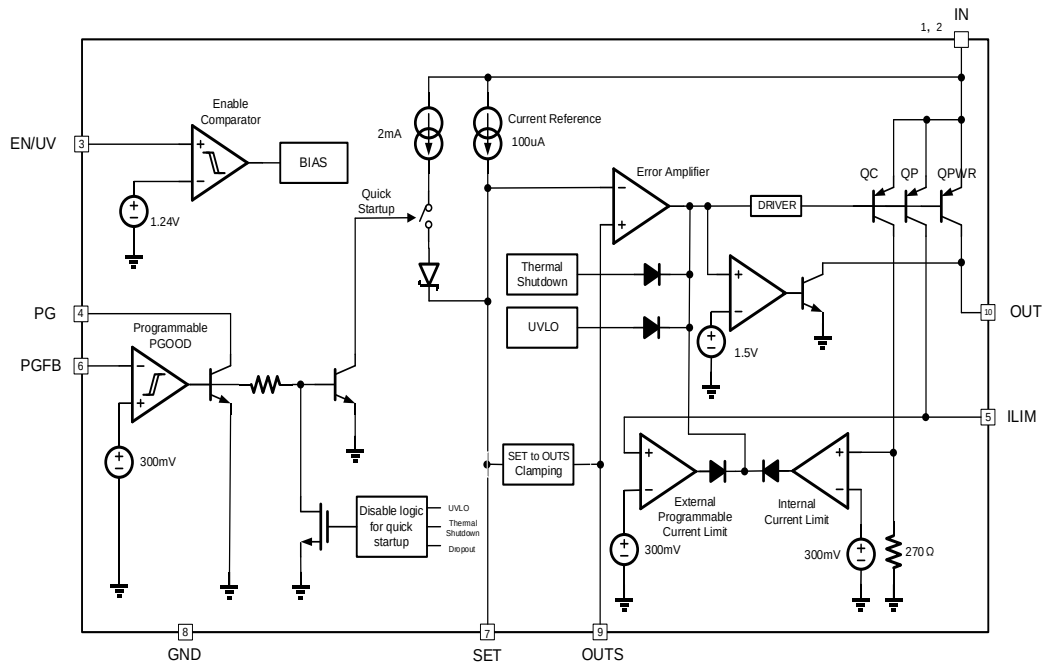


Figure2. Block Diagram

Functional Description

Input Capacitor

The input terminal of ET52HS27ADJ adopts a minimum 4.7μF capacitor for stability, and it is generally recommended to use a low ESR ceramic capacitor as the input terminal capacitor. In the scenario where a long wire is used to connect to the input terminal of ET52HS27ADJ, using a low value input capacitor can cause unstable operation of the linear regulator under high load currents. This is caused by the LC resonant circuit formed by the inductance of the wire and the input capacitor. The self-inductance of a wire is proportional to its length, while the influence of its diameter on its self-inductance is relatively small. So, it is recommended to distribute the current flowing to ET52HS27ADJ between two parallel wires during Layout, and increase the wire spacing to reduce inductance; Separate the wires connecting two identical inductors in parallel.

If the power supply end is close to ET52HS27ADJ, a 4.7μF input capacitor can meet the stability requirements. If the distance is far, a capacitor with a larger capacitance value should be used. A rough selection criterion can be followed, which is to use 1μF capacitor for every 8mil of wire length in addition to the minimum value of 4.7μF. The minimum input capacitance required to achieve stable application circuits will also vary with the output capacitance and load current.

In addition, setting up a series resistor between the power supply end and the input of ET52HS27ADJ can also help stabilize the application circuit. If necessary, a resistor as small as 0.1Ω to 0.5Ω can be connected in series. This impedance has a damping effect on the LC resonant circuit, but at the cost of sacrificing the dropout voltage. A better alternative is to connect a tantalum capacitor or electrolytic capacitor with a higher ESR in parallel with a 4.7μF ceramic capacitor at the input of ET52HS27ADJ.

Output Capacitor

The output terminal of ET52HS27ADJ also requires capacitors to achieve stable output. Given its high bandwidth (approximately 1MHz) performance, it is recommended to use low ESR and ESL ceramic capacitors. Generally, a 4.7μF(minimum) output capacitor with an ESR below 50mΩ and ESL below 2nH is chosen. In order to minimize the impact of circuit board inductance on the dynamic performance of ET52HS27ADJ, the OUTS pin should be directly connected to the output capacitor using a Kelvin connection, and the GND terminal of the SET pin capacitor (C_{SET}) should be directly connected to the GND terminal of the output capacitor using a Kelvin connection. In addition, the GND connection of the input capacitor should be connected as close as possible to the GND connection of the output capacitor. By using a single 4.7μF ceramic output capacitor, high PSRR and low noise performance can be achieved. Increasing the output capacitor can only slightly improve performance, as the bandwidth of the regulator decreases with increasing output capacitance. However, a larger output capacitance value can improve the peak-to-peak voltage during load transient response.

Output Voltage

The ET52HS27ADJ can support voltage outputs ranging from 0.5V to 16V and is equipped with a high-precision 100μA current source. It is led out from the SET pin and connected to the inverting input of the error amplifier. Connecting a resistor between the SET pin and ground can generate a voltage reference for the error amplifier. The reference voltage value is the product of the SET pin current and the SET pin resistance.

$$V_{OUT} = I_{SET} \times R_{SET} \quad (1)$$

The rail-to-rail error amplifier and current reference of ET52HS27ADJ can provide a wide output voltage range, from 0V (using a 0Ω resistor) to (V_{IN} - $V_{Dropout}$) (up to 16V). The advantage of using a current reference is that the regulator always operates at unity gain, independent of the programmed output voltage. This ensures that the loop gain, frequency response, and bandwidth are not affected by the output voltage. Therefore, noise, PSRR, and transient performance will not vary with the output voltage.

Due to the fact that amplifying the SET pin voltage to a higher output voltage does not require any error amplifier gain, the output voltage regulation can be more strictly limited within a range of a few hundred μV, rather than a fixed percentage of the output voltage. Due to the high accuracy of the reference current source, the SET pin resistor may become a limiting factor in achieving high-precision voltage output. Therefore, it is recommended to use ±1% high-precision resistors for the selection of SET resistors.

Enable/Undervoltage-Lockout (EN / UV)

The EN/UV pin is used to control the output working state of the voltage regulator. When the voltage level is high, it is in normal working state, and when the voltage level is low, it places the voltage regulator in low-power off state. As shown in Figure3, the EN/UV pin has an accurate 1.24V turn-on threshold and a 20mV hysteresis. This threshold can be used to define an accurate undervoltage lockout (UVLO) threshold for the voltage regulator with a resistive divider derived from the input power supply. When calculating the resistance divider network, it is necessary to consider the EN/UV pin current (IEN) under the threshold condition given in Electrical Characteristics:

$$V_{IN(UVLO)} = 1.24V \times (1 + R_{EN1} / R_{EN2}) \times I_{EN} \times R_{EN1} \quad (2)$$

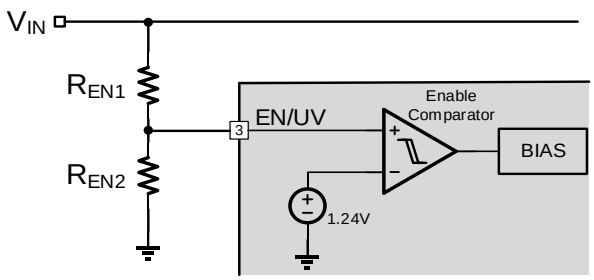


Figure3. Typical Applications of UVLO

If this function is not needed, the EN pin can be directly pulled up to VIN or a determined high and low level can be provided for control.

Output Voltage Detection

ET52HS27ADJ provides an output Kelvin detection connection OUTS pin, which is connected to the in-phase terminal of the internal amplifier. In order to achieve optimal transient performance and load regulation, the Kelvin connection method should be used in Layout, directly connecting the OUTS to the output capacitor and load. When laying out the PCB, the output capacitor and the capacitor GND of the SET pin should be placed as close as possible. In addition, the GND of the output capacitor and the input capacitor should also be placed as close as possible.

Output Noise

The ET52HS27ADJ has excellent noise performance, with a typical V_{IN} and V_{OUT} bypass capacitor of 4.7μF. Its output noise is only 1.6μV_{RMS} in the frequency band of 10Hz to 100kHz, thanks to its very clever circuit design architecture. The traditional voltage regulator noise sources include its voltage reference, error amplifier, resistor divider network noise, and the noise gain generated by the resistor divider. Many low-noise voltage regulators are equipped with voltage reference pins to achieve noise reduction through a bypass of the reference voltage.

Unlike traditional digital linear regulators, the ET52HS27ADJ does not use a voltage reference, but instead uses a 100μA current reference. This current reference operates at a typical noise current level of $20pA/\sqrt{Hz}$ (10Hz-100kHz 6nA_{RMS}). The generated voltage noise is equal to the current noise multiplied by the resistance value, and then the RMS sum is calculated with the noise of the error amplifier and the inherent noise of the $\sqrt{4kTR}$ resistor (where k = Boltzmann constant 1.38 × 10-23J/K, T is absolute temperature).

One problem faced by traditional linear regulators is that the resistor divider responsible for setting the output voltage increases the reference noise. On the contrary, the unit gain follower architecture of ET52HS27ADJ does not provide gain between the SET pin and the output. Therefore, if a capacitor bypasses the SET pin resistor, the output noise will be independent of the programming output voltage. In this way, when using a 4.7μFSET pin capacitor, the final output noise generated is only determined by the noise setting of the error amplifier, typically $2nV/\sqrt{Hz}$ (within a bandwidth of 10kHz to 1MHz) and 0.8μVRMS (10Hz-100kHz).

Programmable Power-Good Indication

Power-Good indicator, responsible for indicating the collector open circuit mark for output voltage regulation. Compared with the reference voltage of the internal voltage comparator of the device (typical value of 300mV), if it is lower than this value, PG is pulled to a low level. If the power indicator is not in good condition, it can be left hanging.

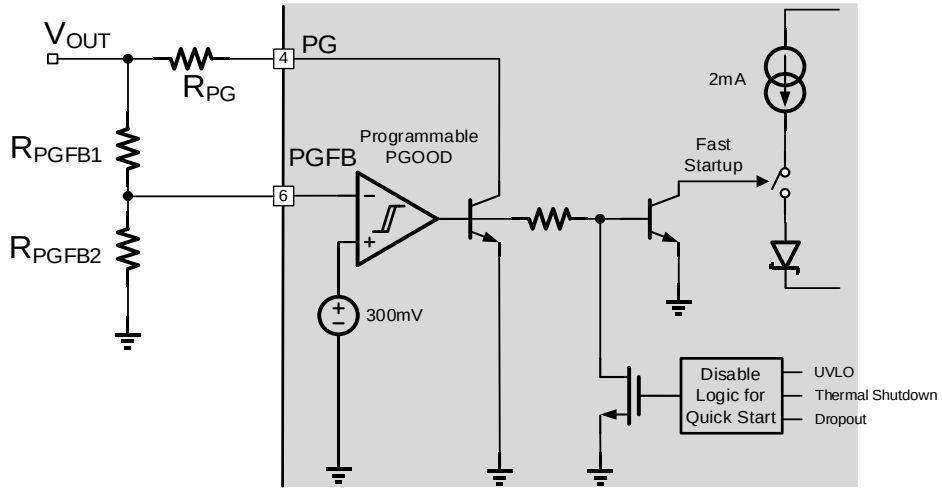


Figure4. Typical Applications of Parallel PG and PGFB Functions

As shown in the Figure4, the threshold for power-good supply can be set by the user using the ratio of the resistance values of two external resistors (R_{PGFB1} and R_{PGFB2}):

$$V_{OUT(PG\_Threshold)} = 0.3V \times (1 + R_{GFB1} / P_{GFB2}) + I_{PGFB} \times R_{PG1} \quad (3)$$

If the voltage of the PGFB pin increases above 300mV, the collector open circuit PG pin is set to invalid and becomes high impedance. The comparator with power-good supply has a 7mV hysteresis and a delay time of 5μs. When determining the resistor divider network, the PGFB pin current (I_{PGFB}) given in electrical characteristics table must be considered. If R_{PG1} is less than 30kΩ, the PGFB pin current (I_{PGFB}) can be ignored.

If the power-good indicator function is not used, float the PG pin. Please note that when the output voltage is below 300mV, the good and quick startup functions of the programmable power supply are disabled.

Quick Startup

The ET52HS27ADJ has a built-in quick startup circuit that increases the SET pin current to approximately 2mA during startup. As shown in the Figure4, the 2mA current source continues to operate when the PGFB is below 300mV (typical value), unless the regulator is in a current limiting state, differential voltage state, hot shutdown state, or the input voltage is below the minimum VIN. In practical applications, according to the design method of typical application circuit diagrams, the voltage of the PGFB pin cannot be lower than 300mV, that is, the voltage level divided by R_{PGFB1} and R_{PGFB2} to PGFB should be higher than 300mV, otherwise it will cause abnormal device operation.

If PGFB increases to over 300mV on its rising edge and has a hysteresis of 10mV on its falling edge, pull the PG pin to high level. The threshold is determined by formula3 (based on a typical application circuit diagram), and an external resistive voltage divider such as R_{PGFB1} and R_{PGFB2} is connected between the OUT, PGFB, and GND pins.

If the quick startup function is not used, the PGFB should be connected to IN or OUT (for output voltages above 300mV). Please note that this will also disable the power-good indicator function.

External Programmable Current Limit

The current limit threshold for the ILIM pin of ET52HS27ADJ is 300mV, and adding a ground resistor to the ILIM pin can set different current limits. The programming scale factor is approximately 100mA• kΩ. For example, a 1kΩ resistor sets the current limit to 100mA. When the voltage difference between IN and OUT is large, the return circuit of ET52HS27ADJ will reduce the internal current limit, which may be lower than the external programming current limit level. Therefore, in order to achieve good accuracy, detailed verification of the selection of programmable current limiting resistor values should be carried out in practical use.

The ILIM pin provides a current proportional to the output current, therefore it also has a current monitoring function in the range of 0V to 300mV. If the current limit function is not required, it can be directly connected to GND. There is a parasitic diode between the ILIM and GND pins of ET52HS27ADJ, so do not drive the ILIM below GND by more than 0.3V when using the device.

Protection Function

The ET52HS27ADJ is equipped with various protection functions for battery powered applications. High-precision current limiting and thermal shutdown can provide protection against overload and fault conditions at the output of the device. During normal use, the junction temperature is not allowed to exceed 125°C. In order to protect the low-noise error amplifier of ET52HS27ADJ, the SET to OUTS protection clamp limits the maximum voltage between SET and OUTS to ±15V (the maximum DC current flowing through this clamp is 20mA). Therefore, for applications where SET is actively driven by a voltage source, the current of the voltage source must be limited to 20mA or less. In order to cope with transient currents flowing through these clamps in the event of load transient faults, the maximum value of the SET pin capacitor (C_{SET}) should be limited to 22μF.

The ET52HS27ADJ has a built-in reverse input protection circuit, which allows the IN pin to withstand reverse voltages up to -20V without causing any input current or generating negative voltage on the OUT pin. When the polarity of the battery is reversed during insertion, the voltage regulator can provide protection for itself and the load. When the input is pulled to GND, pulled to an intermediate voltage, or placed in an open circuit state, and the output terminal still has voltage, the reverse current protection circuit will prevent current from flowing from the output to the input. Due to the clamp from OUTS to SET, unless the SET pin is floating,

current can flow through the SET pin resistor to GND and through the output overshoot recovery circuit to GND (up to 15mA). In practical applications, by placing a Schottky diode between the OUTS and SET pins (with its positive terminal on the OUTS pin), the current flowing through the output overshoot recovery circuit can be significantly reduced.

The ET52HS27ADJ also has a built-in safety work area protection circuit. When the input to output voltage difference is greater than 12V, the protection circuit will be activated. When the input to output voltage difference increases, reduce the current limit and keep the power transistor within a safe operating range for all input to output voltage values (up to the absolute maximum rated value of ET52HS27ADJ). When powered on for the first time and the input voltage rises, the output will follow the input and maintain a very low input to output voltage difference, so that the regulator can provide a large output current. Due to the current limiting protection for turn back, if the output voltage is low and the load current is high, a problem may occur under high input voltage conditions. In this case, when the short circuit is eliminated or the EN/UV pin is pulled to a high level, the load line intersects with the output current curve at two points. At this point, the voltage regulator has two stable operating points. Due to this double crossover, the input power may need to be turned off to zero and pulled up again to complete output recovery. This phenomenon is not unique to ET52HS27ADJ and is present in other linear regulators with current limit protection function.

Parallel Chip Current Expansion

The parallel use of ET52HS27ADJ can provide higher output current and reduce output noise, and is also beneficial for heat dissipation on the PCB. Connect the SET and IN pins of all parallel chips together in practical applications; Connect the OUTS pin directly to the output capacitor. Use a small section of PCB wiring (equivalent to a ballast resistor) to connect the OUT pins together to balance the output current of ET52HS27ADJ. The maximum output voltage offset of each parallel ET52HS27ADJ is very small, so it can minimize the required ballast resistance value to the maximum extent. As shown in the figure5, two ET52HS27ADJ with a 50mΩ PCB printed line ballast resistor each can provide output current sharing of better than 80% under full load conditions.

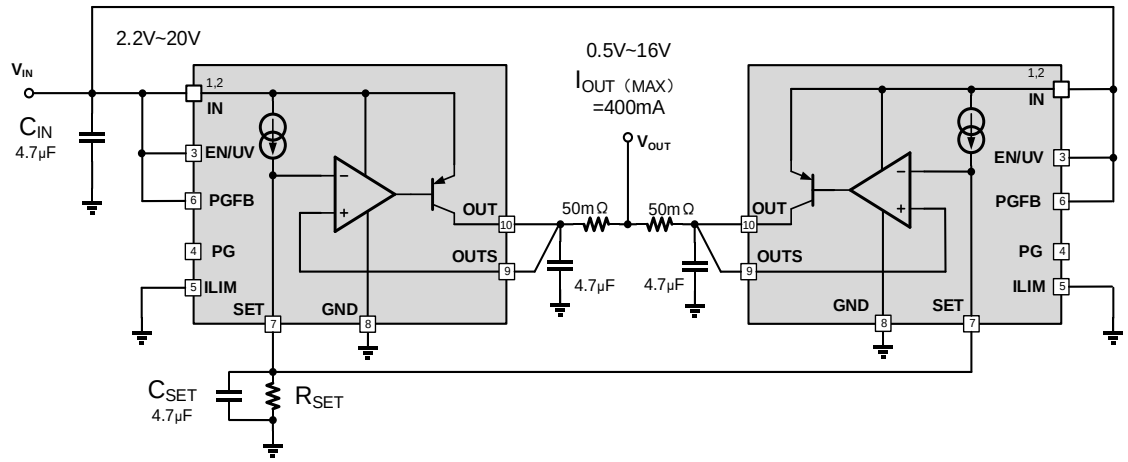


Figure5. PG Parallel application

Absolute Maximum Ratings

Symbol	Parameters	Symbol	Symbol
V_{IN}, $V_{EN/UV}$, V_{PG}, V_{PGFB}	Input Voltage (IN, EN/UV, PG, PGFB Pin)	-0.3 to 22	V
V_{OUT}, V_{OUTS}, V_{SET}	Output Voltage (OUT, OUTS, SET Pin)	-0.3 to 16	V
I_{LIM}	Current Limit	-0.3 to 1	A
T_J	Operating Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-65 to 150	°C

Thermal Characteristics

ET52HS27ADJ has overload protection and thermal protection functions. Its over temperature protection point is 150°C and has a hysteresis of approximately 12°C. For continuous stable loads, the surface temperature should not exceed 125°C. Therefore, attention should always be paid to the mutual constraint relationship between the voltage difference and the load current under its maximum heat dissipation power consumption.

Device Thermal Resistance

Table1. ET52HS27ADJ(DFN10) Reference Data for the Thermal Resistance

The Area of Copper		The Area of the Circuit Board (mm^2)	$R_{\theta JA}$ (°C/W)
TOP (mm^2)	BOTTOM (mm^2)		
3600	3600	3600	33.5
1000	3600	3600	34
400	3600	3600	36
100	3600	3600	36.2

Table2. ET52HS27ADJ(MSOP10) Reference Data for the Thermal Resistance

The Area of Copper		The Area of the Circuit Board (mm^2)	$R_{\theta JA}$ (°C/W)
TOP (mm^2)	BOTTOM (mm^2)		
3600	3600	3600	55
100	3600	3600	60

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input Voltage (IN Pin)	2.4		20	V
V_{OUT}	Output Voltage	0.6		16	V
V_{EN}	Input Voltage (EN Pin)	1.6		20	V
I_{OUT}	Output Current		200		mA
T_J	Operating Junction Temperature	-40		125	°C

Electrical Characteristics

V_{IN} = V_{OUT} + 2V; I_{LOAD} = 10mA, C_{IN} = C_{OUT} = 4.7μF, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{IN} (1)	Operating Input Voltage	I_{LOAD} = 200mA, V_{IN} UVLO Rise		2.4		20	V
V_{UVLO}	Under-Voltage Lockout	VIN UVLO Hysteresis			2.3		V
V_{IN_MIN}	Minimum Input Voltage				100		mV
Reg_{LINE}	Line Regulation	V_{IN} = 3.6V~20V, I_{LOAD} = 1mA, V_{OUT} = 3V		-0.3	0.02	0.3	mV/V
Reg_{LOAD}	Load Regulation	I_{LOAD} = 1mA~200mA, V_{IN} = 3.6V, V_{OUT} = 3V			0.03		mV/mA
V_{DROP}(4)	Dropout Voltage	I_{LOAD} = 1mA					
		I_{LOAD} = 50mA			300		mV
		I_{LOAD} = 150mA			330		mV
		I_{LOAD} = 200mA			350		mV
I_Q(5)	Quiescent Current	I_{LOAD} = 10μA			2.7		mA
		I_{LOAD} = 10mA			3	46	mA
		I_{LOAD} = 50mA			4	9	mA
		I_{LOAD} = 100mA			4.7	18	mA
		I_{LOAD} = 200mA			6.3		mA
e_N (3)(8)	Output Noise Voltage	C_{SET} = 4.7μF, V_{OUT} = 7V, BW = 10Hz~100KHz	I_{LOAD} = 10mA		1.6		μV_{RMS}
			I_{LOAD} = 200mA		1.8		μV_{RMS}
PSRR (3)(8)	Power Supply Rejection Ratio	3V ≤ V_{OUT} ≤ 16V, V_{IN} - V_{OUT} = 2V (Average), V_{RIPPLE} = 200mV_{P-P}, I_{LOAD} = 10mA, C_{IN} = 10nF, C_{SET} = 4.7μF	f = 100Hz		120		dB
			f = 10kHz		118		dB
			f = 100kHz		95		dB
			f = 1MHz		78		dB
			f = 10MHz		40		dB
V_{EN/UV_TH}	EN/UV Pin Threshold	EN/UV Rise (Turn On)			1.24	1.6	V
V_{EN/UV_HYS}	EN/UV Pin Hysteresis	EN/UV Falling Hysteresis			10		mV
$I_{EN/UV}$	EN/UV Pin Quiescent Current	$V_{EN/UV}$ = 0V, V_{IN} = 20V				±1	μA

Electrical Characteristics (Continued)

V_{IN} = V_{OUT} + 2V; I_{LOAD} = 10mA, C_{IN} = C_{OUT} = 4.7μF, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{SD}	Shutdown Quiescent Current	$V_{EN/UV}$ = 0V, V_{IN} = 4V		0.8	1	μA
I_{LIMIT} (10)	Current Limit	V_{OUT} = 0V		260		mA
V_{PGFB_R}	PGFB Rise	PGFB Rise	290	300	330	mV
V_{PGFB_HYS}	PGFB Hysteresis	PGFB Falling Hysteresis		2		mV
I_{PGFB}	PGFB Quiescent Current	V_{IN} = 2V, V_{GFB} = 300mV		25		nA
V_{PG_LOW}	PG Pin Low Level Voltage	I_{PG} = 100μA		20	60	mV
I_{PG}	PG Leakage Current	V_{PG} = 20V			1	μA
I_{REV}	Reverse Output Current	V_{IN} = -20V, $V_{EN/UV}$ = 0V, V_{OUT} = 0V, V_{SET} = 0V		9		mA
T_{TSD} (8)	Thermal Shutdown Threshold	T_J Rise		150		°C
T_{HYS} (8)	Thermal Shutdown Hysteresis	T_J Falling from Shutdown		12		°C
t_{ON} (7)	Output Turn-on Time	V_{OUT} = 3V, I_{LOAD} = 200mA, C_{SET} = 4.7μF, V_{IN} = 5V, V_{PGFB} = V_{IN}, R_{SET} = 30kΩ		600		ms
		V_{OUT} = 3V, I_{LOAD} = 200mA, C_{SET} = 4.7μF, V_{IN} = 5V, R_{PGFB1} = 102kΩ, R_{PGFB2} = 11.3kΩ, R_{SET} = 30kΩ		12		ms

Note1: Here V_{IN} means internal circuit can work normal.

Note2: The maximum junction temperature will limit the operating conditions of the device. So, the stable output specification is not applicable to all possible combinations of input voltage and output current, especially since the internal folding current limit is reduced when V_{IN} - V_{OUT} > 12V. If operating under maximum output current conditions, limit the input voltage range. If operating under maximum input voltage conditions, limit the output current range.

Note3: OUTS is directly connected to OUT.

Note4: Dropout voltage is measured when the output exceeds the adjustment range by 1% under a specified output current condition. Compared to the dropout voltage measured at V_{IN} = $V_{OUT\ (NOMINAL)}$, this definition will generate a higher dropout voltage.

Note5: The working power supply current is used to evaluate the GND pin current. Please note that the GND pin current does not include the SET pin or ILIM pin current.

Note6: The SET and OUTS pins are clamped using diodes and two 25Ω series resistors. For transients with a duration of less than 5ms, the clamp circuit can transmit a current greater than the rated current.

Note7: The capacitor on the SET pin can reduce output noise. But it will increase the startup time.

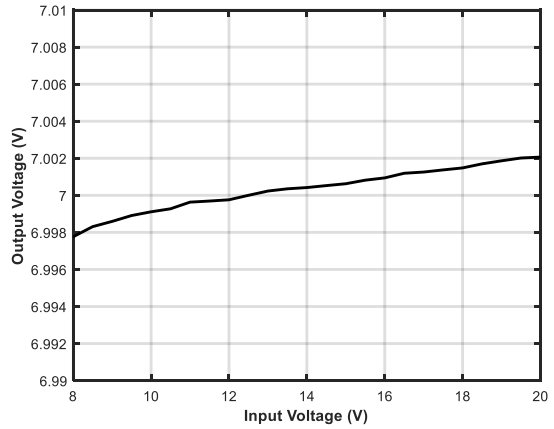
Note8: ET52HS27ADJ is tested and specified under pulse load conditions to achieve $T_J \approx T_A$.

Note9: Parasitic diodes exist internally between the ILIM, PG, PGFB, SET, OUTS, and OUT pins and the GND pin. Do not drive these pins below the GND pin level by more than 0.3V in the event of a fault. During normal operation, these pins must be at a voltage higher than GND.

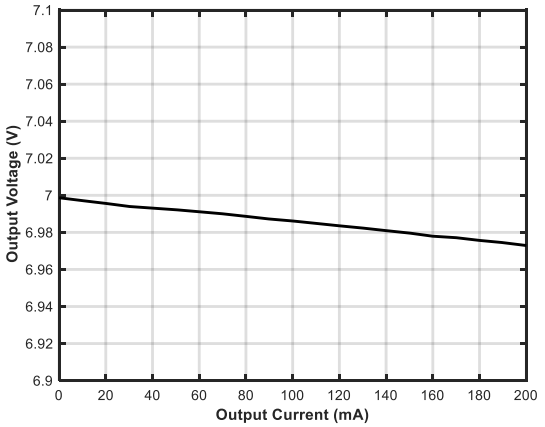
Note10: The internal current limiting function circuit provides turn back protection for V_{IN} - V_{OUT} voltage differences greater than 10V.

Typical Characteristics

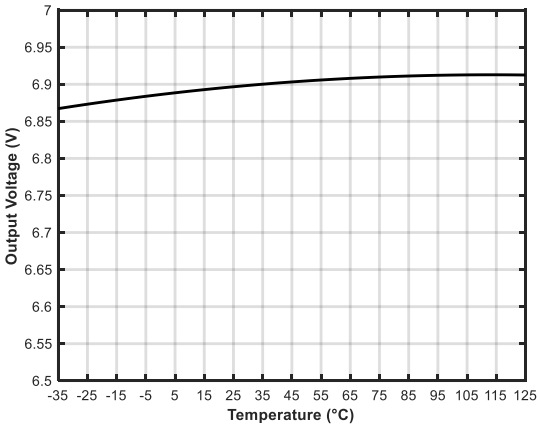
(C_{IN} = C_{OUT} = C_{SET} = 4.7μF, V_{IN} = 9V, V_{EN} = 9V, PG is Floating, ILIM = GND, PGFB = OUT, OUTS = OUT, V_{OUT} = 7V, I_{OUT} = 10mA. Typical values are at T_A = 25°C, unless otherwise noted.)



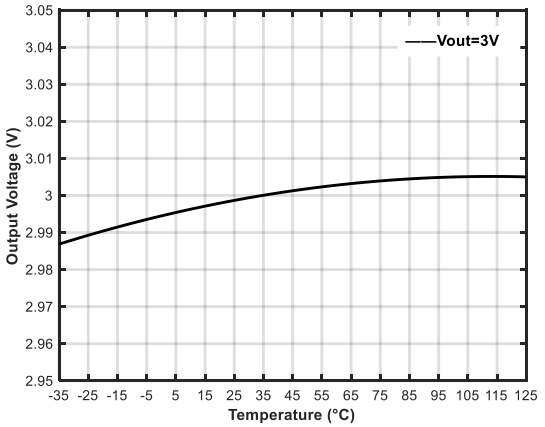
Output Voltage VS Input Voltage



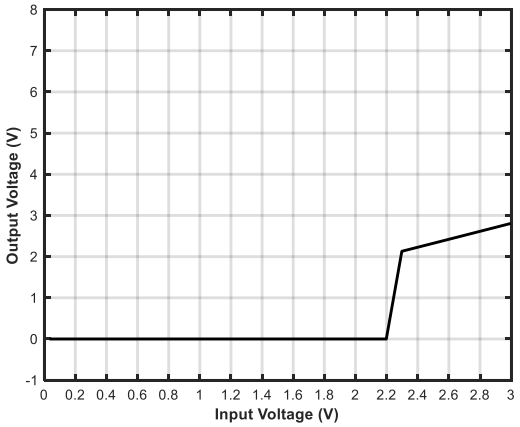
Output Voltage VS Output Current



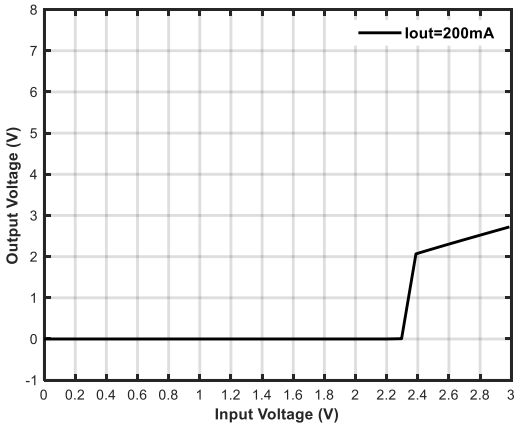
Output Voltage VS Temperature



Output Voltage VS Temperature



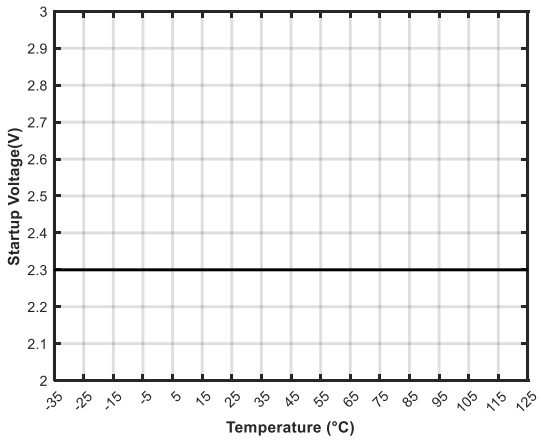
Output Voltage VS Input Voltage



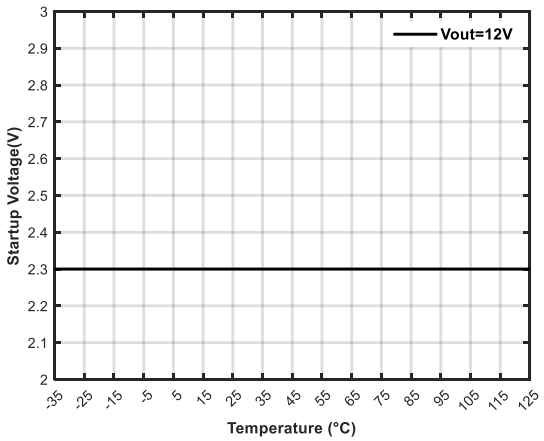
Output Voltage VS Input Voltage

Typical Characteristics (Continued)

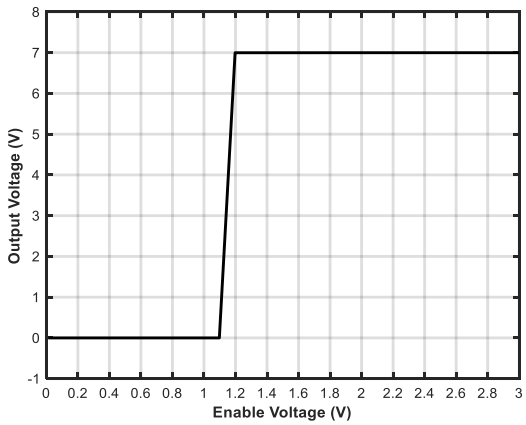
(C_{IN} = C_{OUT} = C_{SET} = 4.7μF, V_{IN} = 9V, V_{EN} = 9V, PG is Floating, ILIM = GND, PGFB = OUT, OUTS = OUT, V_{OUT} = 7V, I_{OUT} = 10mA. Typical values are at T_A = 25°C, unless otherwise noted.)



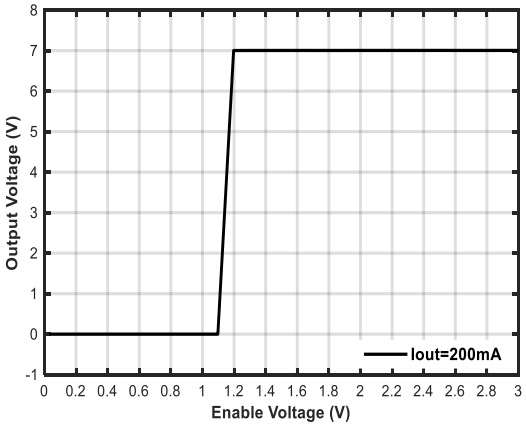
Startup Voltage VS Temperature



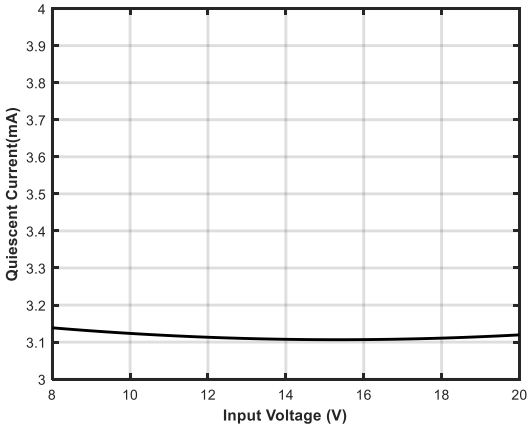
Startup Voltage VS Temperature



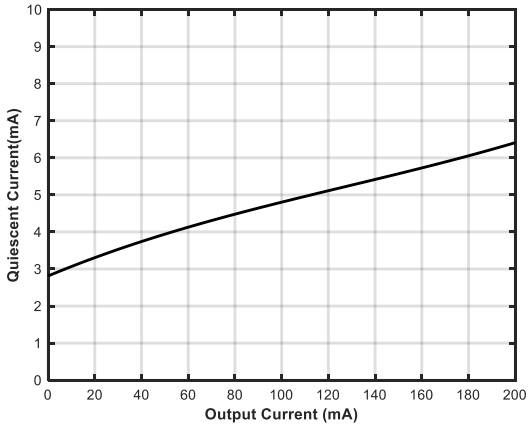
Output Voltage VS Enable Voltage



Output Voltage VS Enable Voltage



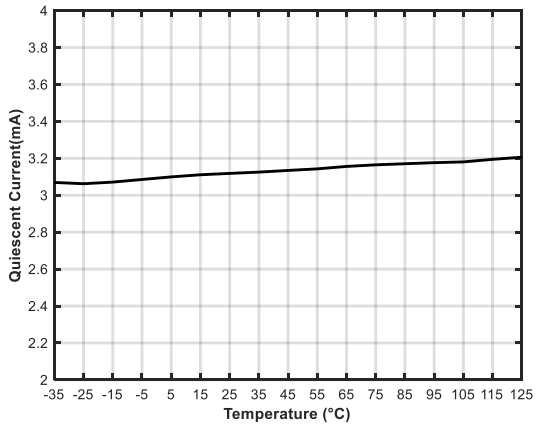
Quiescent Current VS Input Voltage



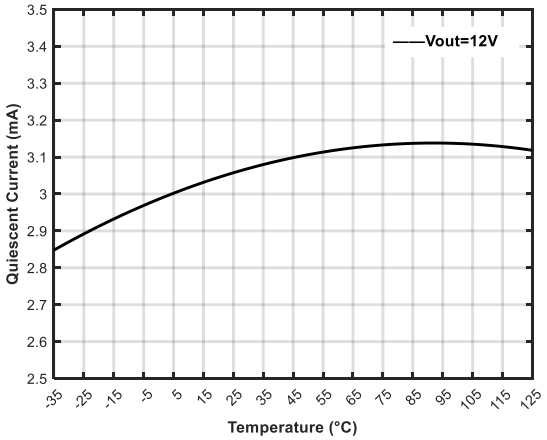
Quiescent Current VS Output Voltage

Typical Characteristics (Continued)

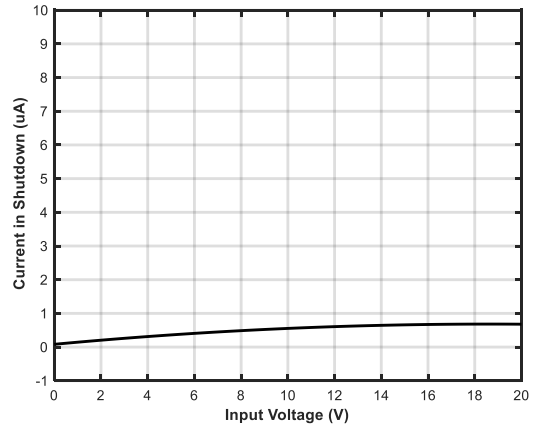
(C_{IN} = C_{OUT} = C_{SET} = 4.7μF, V_{IN} = 9V, V_{EN} = 9V, PG is Floating, ILIM = GND, PGFB = OUT, OUTS = OUT, V_{OUT} = 7V, I_{OUT} = 10mA. Typical values are at T_A = 25°C, unless otherwise noted.)



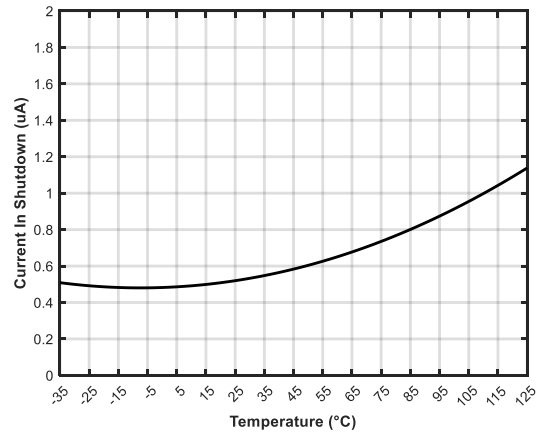
Quiescent Current VS Temperature



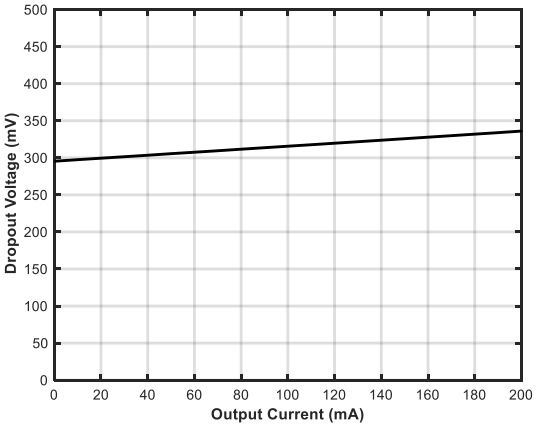
Quiescent Current VS Temperature



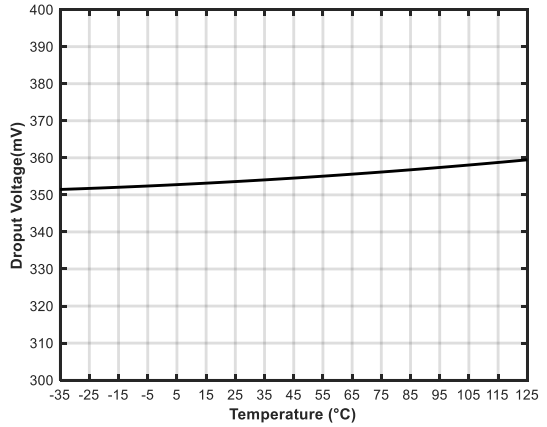
Current Shutdown VS Input Voltage



Current Shutdown VS Temperature



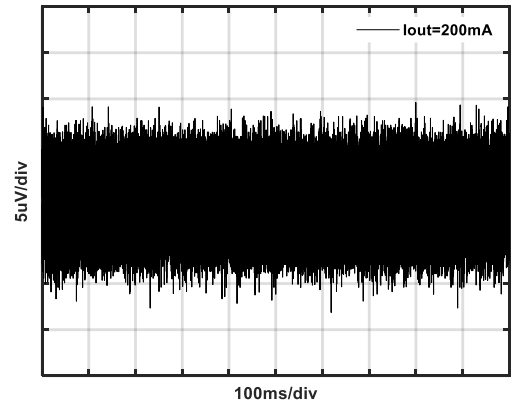
Dropout Voltage VS Output Current



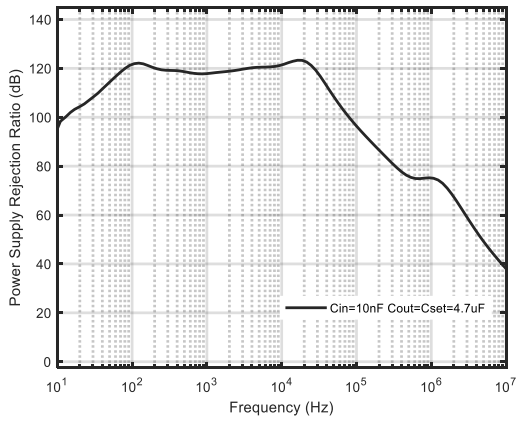
Dropout Voltage VS Temperature

Typical Characteristics (Continued)

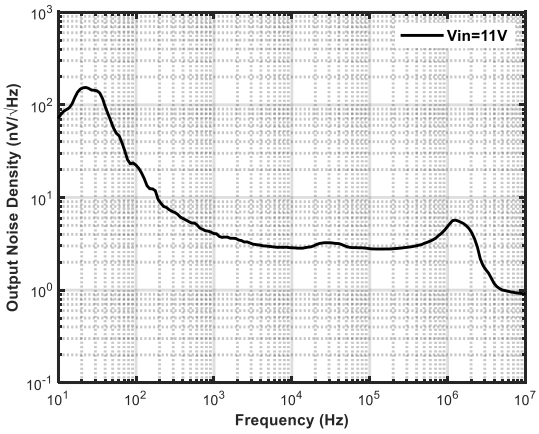
(C_{IN} = C_{OUT} = C_{SET} = 4.7μF, V_{IN} = 9V, V_{EN} = 9V, PG is Floating, ILIM = GND, PGFB = OUT, OUTS = OUT, V_{OUT} = 7V, I_{OUT} = 10mA. Typical values are at T_A = 25°C, unless otherwise noted.)



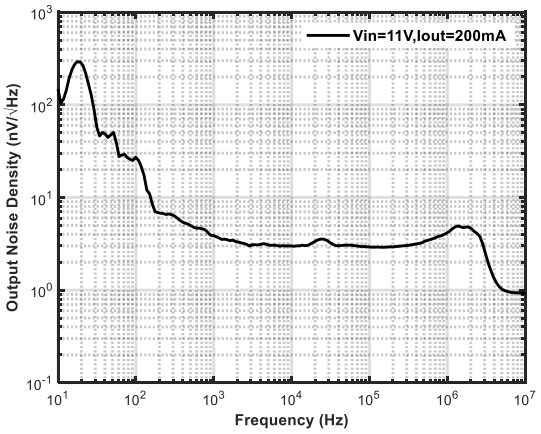
Noise



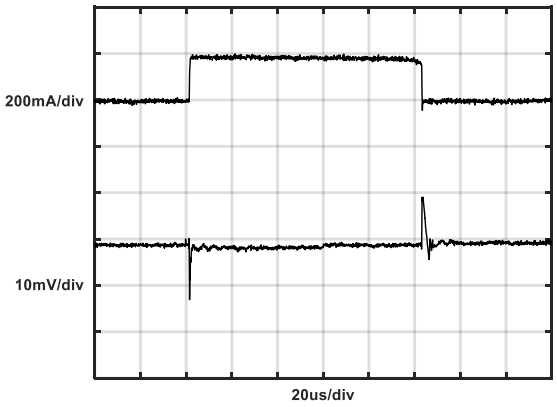
Power Supply Rejection Ratio



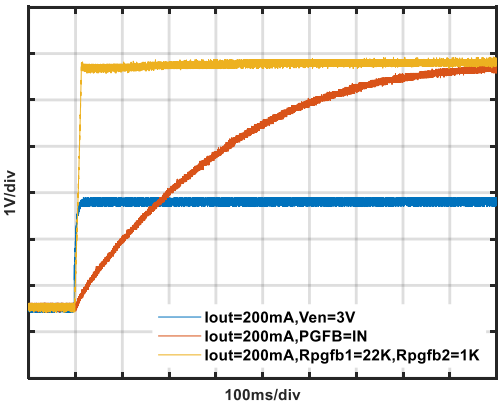
Power Supply Rejection Ratio



Power Supply Rejection Ratio



Load Transient Response



t_{on}

Application Circuits

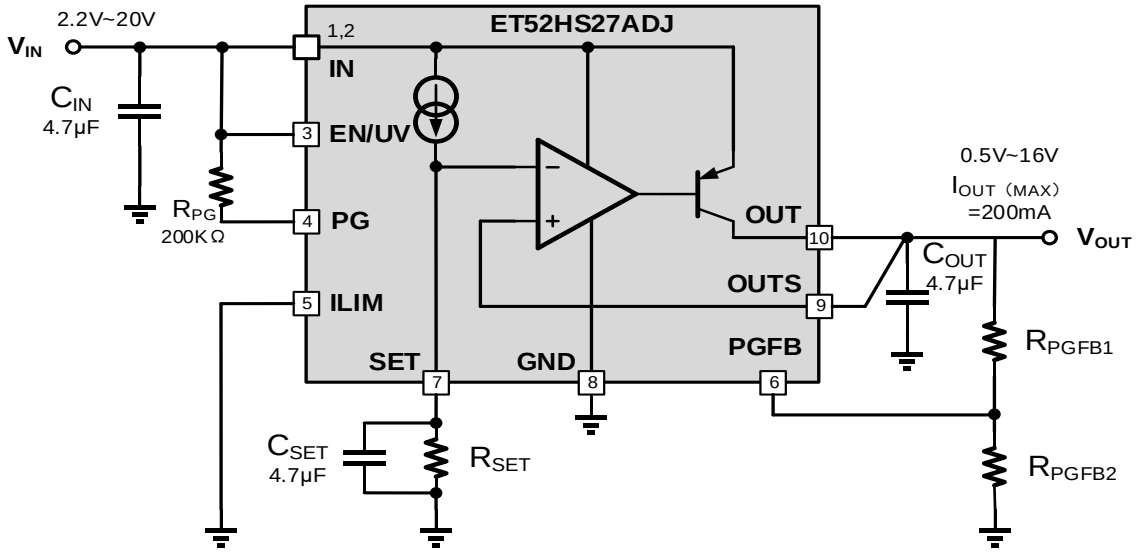
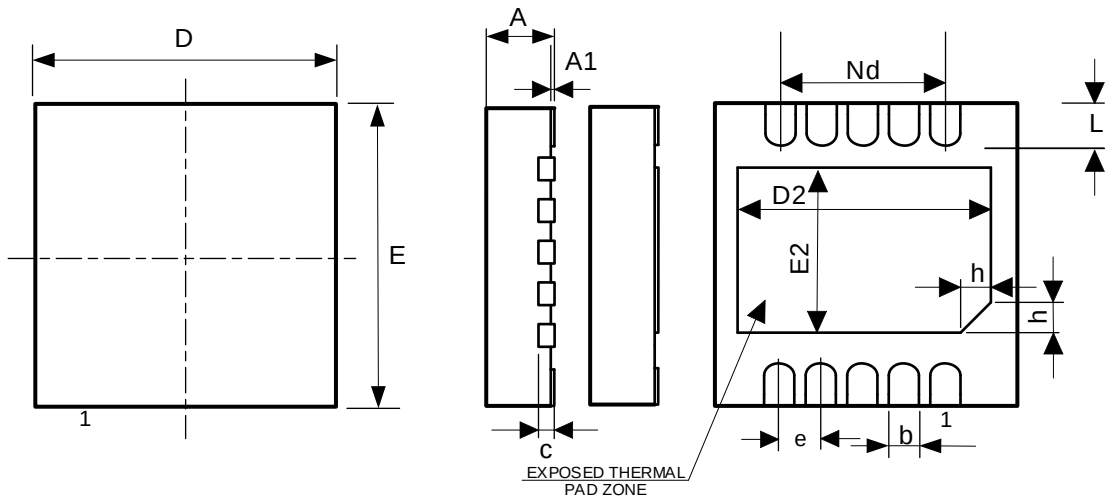


Figure6. Application Circuits

Package Dimension

DFN10 (3mm × 3mm)



Top View Side View Bottom View

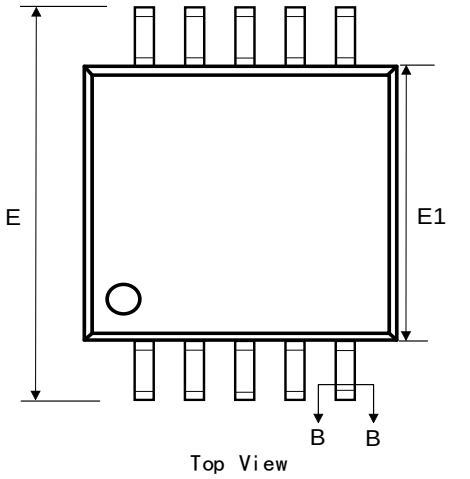
COMMON DIMENSIONS

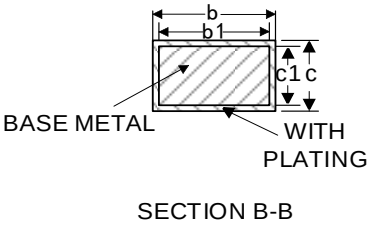
(Unit: mm)

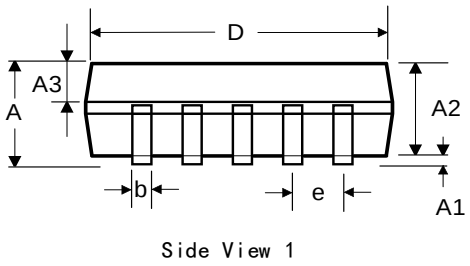
SIZE / LABEL	MIN	NOM	MAX	SIZE / LABEL	MIN	NOM	MAX
A	0.70	0.75	0.80	e	0.50BSC		
A1	-	0.02	0.05	Nd	2.00BSC		
b	0.18	0.25	0.30	E	2.90	3.00	3.10
c	0.18	0.20	0.25	E2	1.45	1.55	1.65
D	2.90	3.00	3.10	L	0.30	0.40	0.50
D2	2.40	2.50	2.60	h	0.20	0.25	0.30

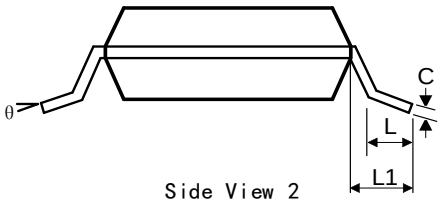
Package Dimension (Continued)

MSOP10









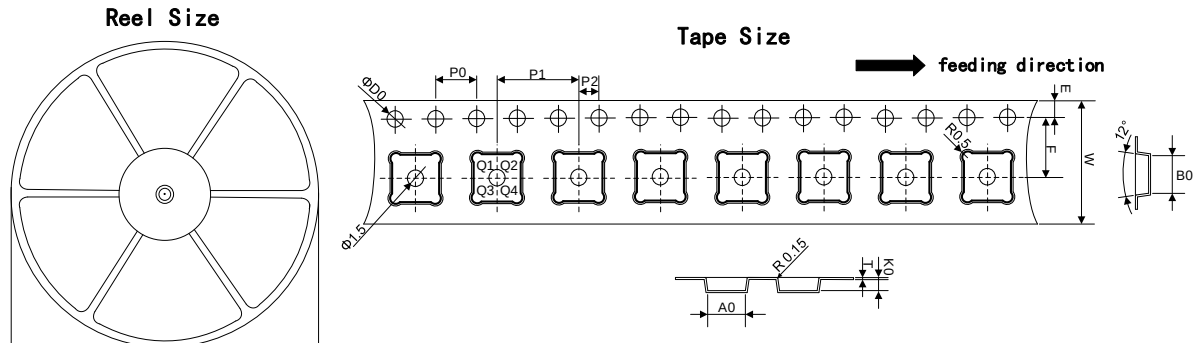
COMMON DIMENSIONS

(Unit: mm)

SIZE / LABEL	MIN	NOM	MAX	SIZE / LABEL	MIN	NOM	MAX
A	-	-	1.10	D	2.90	3.00	3.10
A1	0.05	-	0.15	E	4.70	4.90	5.10
A2	0.75	0.85	0.95	E1	2.90	3.00	3.10
A3	0.30	0.35	0.40	b	0.18	-	0.26
L	0.40	0.55	0.70	b1	0.17	0.20	0.23
L1	0.95REF			e	0.50BSC		
c	0.15	-	0.19	θ	0°	-	8°
c1	0.14	0.15	0.16				

Tape and Reel Information

DFN10 (3mm × 3mm)



Reel Size

Sign	Size
Reel Diameter	13″
Reel Width W1(mm)	12.5

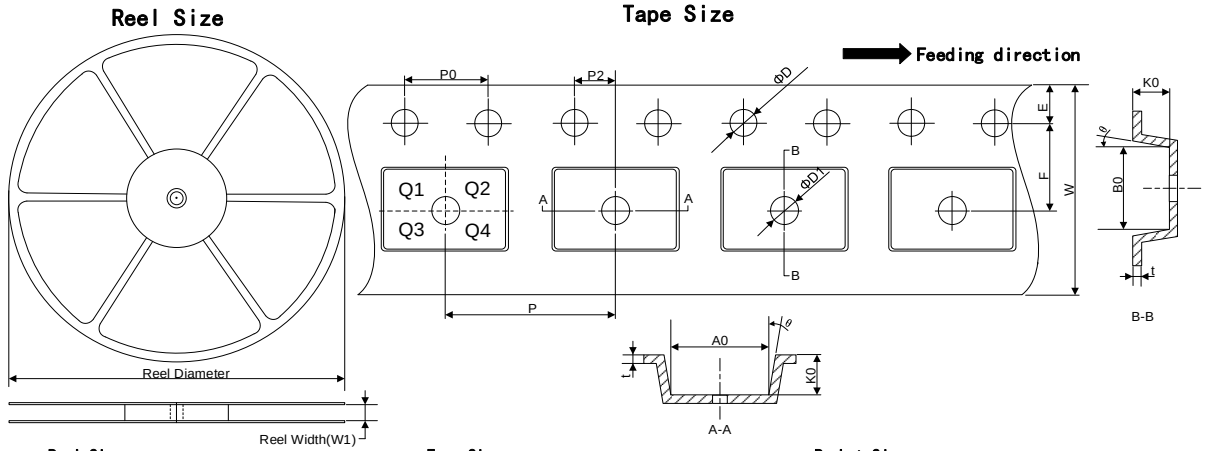
Tape Size

Sign	Size(mm)
E	1.75±0.10
F	5.50±0.10
P2	2.00±0.10
D0	$1.50^{+0.10}_{0}$
P0	4.00±0.10
P2	2.00±0.10

Pocket Size

Sign	Size(mm)
W	12.00±0.30
P1	8.00±0.10
A0	3.30±0.10
B0	3.30±0.10
K0	1.10±0.10
T	0.30±0.05
Pin1 Quadrant	Q1

MSOP10



Reel Size

Sign	Size
Reel diameter	13″
Reel width W1(mm)	12.4

Tape Size

Sign	Size(mm)
E	1.75±0.10
F	5.50±0.10
P2	2.00±0.10
D	1.55±0.05
D1	1.55±0.05
P0	4.00±0.10
10P0	40.00±0.20

Pocket Size

Sign	Size(mm)
W	12.00±0.30
P	8.00±0.10
A0	5.40±0.10
B0	3.40±0.10
K0	1.40±0.10
t	0.30±0.05
θ	3-5°TYP
Pin1 Quadrant	Q3

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-07-01	Official Version	Wang anran	Yang xiaoxu	Liu jiaying