High Input Ultra Low Noise 200mA LDO

General Description

The ET52HS11XX is linear regulator (LDO) which achieves very low noise, excellent transient response, and excellent PSRR performance.

When providing an output current of 200mA, the dropout voltage is only 230mV.It is designed for 2.2V to 12V power supplies. The adjustable output voltage range is from 1.2V to (V_{IN} - V_{drop})V.

The typical static operating current is 0.3mA, and it is less than 1μA in shutdown mode, making it highly suitable for noise-sensitive and low-power applications.

In practical applications, the ET52HS11XX's output terminal only requires a 2.2μF ceramic capacitor to provide ultra-low noise performance and good circuit stability. It is equipped with various protection circuits, including over-current and over-heating limits.

ET52HS11XX supports DFN4 (1mm × 1mm) and SOT23-5 package, with a working junction temperature range of -40°C~125°C.

Features

- Ultra-Low Noise: 3uVrms (Typical) @10mA
- High Power Supply Rejection Ratio (PSRR)
  - -- 95dB @1kHz
  - -- 40dB @1MHz
- Output Current: 200mA
- Wide Input Voltage Range from 2.2V~12V(ADJ Vout) or 3.0V,3.3V,5.0V,9.0V,12V,etc(Fixed Vout)
- Single Capacitor Improves Noise and PSRR
- Low Dropout are Typical 230mV at 200mA
- High-Precision Enable Control
- Built-in Undervoltage-Lockout Function
- Built-in Over-current Protection Function
- Configure Output Voltage through External Resistors
- Package Information:

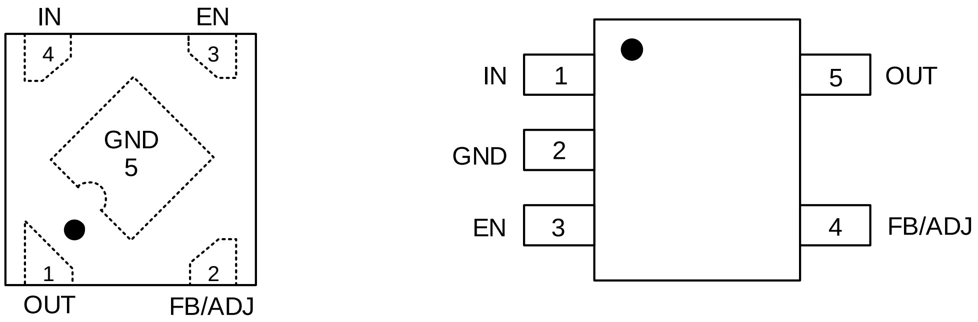
Part No.	Package	Packing Option	MSL
ET52HS11XXYB	DFN4 (1mm × 1mm)	Tape and Reel, 10K/Reel	1
ET52HS11XX	SOT23-5 (1.6mm × 2.9mm)	Tape and Reel, 3K/Reel	3
ET52HS11ADJYB	DFN4 (1mm × 1mm)	Tape and Reel, 10K/Reel	1
ET52HS11ADJ	SOT23-5 (1.6mm × 2.9mm)	Tape and Reel, 3K/Reel	3

*: XX=X.XV, For example, 50 is 5.0V output voltage.

Application

- RF Power Supply: PLL, VCO, Mixer, Low-Noise Amplifier
- Ultra Low Noise Instrument
- High Speed/High-Precision Data Converter
- Medical Applications: Imaging, Diagnosis
- High Precision Power Supply

Pin Configuration



DFN4 SOT23-5

Figure1. Pin Configuration

Pin Function

Pin No.		Pin Name	Pin Description
DFN4	SOT23-5		
1	5	OUT	Output Voltage Port Pin. Requires a bypass capacitor of 2.2μF or larger to connect OUT to GND.
2	4	FB/ADJ	Feedback Pin. Connect to the load side, and use an external resistor divider to set the output voltage higher than the fixed output voltage.
3	3	EN	Enable Control Input, Active High. Do not leave EN floating. The EN enable voltage cannot exceed 5.5V
4	1	IN	The Voltage Regulator's Input Power Pin. Should be bypassed to GND using a 2.2μF or larger capacitor.
5	2	GND	Ground Pin.

Block Diagram

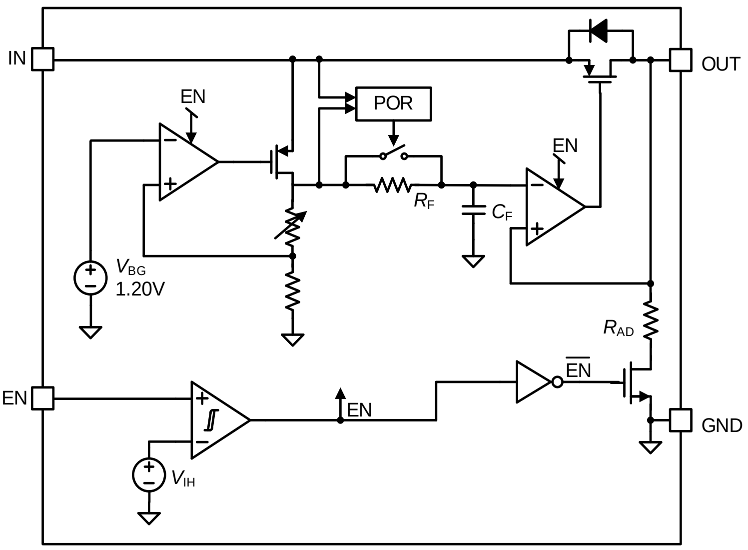


Figure2. Block Diagram

Functional Description

Input Capacitor

The input capacitor should be at least 2.2uF and placed as close to the chip as possible to minimize PCB traces' impact on the circuit. If the output capacitor exceeds 2.2uF, increase the input capacitor value accordingly.

An output capacitor is required for the stability of the LDO. The recommended output capacitance is 2.2μF, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins. This capacitor provides a low impedance path for unwanted AC signals or noise modulated onto a constant input voltage, and limits the impact of parasitic inductance and resistance at the input end on the input voltage during sudden changes in load current.

Output Capacitor

To reduce the impact of temperature on capacitance, it is recommended to use capacitors with X7R or X5R as the medium and a capacitance of 2.2μF as the output capacitor, and place them as close as possible to the OUT pin. To ensure design stability, the minimum effective capacitance is 0.7μF, and the effects of temperature, DC bias, and packaging size changes on capacitance characteristics need to be considered. Especially for capacitors with small package sizes, such as 0201, the effective capacitance value rapidly decreases as the applied DC bias increases.

There is no requirement for the minimum value of equivalent series resistance (ESR). A larger output capacitance and lower ESR can improve load transient response or high-frequency PSRR.

Enable and Disable Operations

Enable/disable the output voltage function using the EN pin. The maximum input voltage of this pin cannot exceed 6V. If the input voltage is greater than 6V, a voltage divider resistor can be used to enable EN. If the EN pin voltage is greater than 1V, the device is in the enabled state; If the EN pin voltage is less than 0.4V, the device is in a disabled state.

The EN pin has an internal pull-down current source with a typical value of 200nA, which ensures that the device is in a disabled state when the EN pin is suspended.

Output voltage Adjustment principle

The adjustable output voltage version allows voltage adjustment through external voltage divider resistors (the maximum output voltage is limited by device characteristics). The voltage adjustment principle is shown in the following formula, where R1 and R2 are the resistors in the output voltage divider, and V_{REF} = 1.2V.

$$V_{OUT} = V_{REF} \times (1 + R1 / R2) \tag{1}$$

It is recommended to choose a KΩ precision resistor as the voltage divider resistor to ensure high output voltage accuracy. At the same time, a 100nF feedforward capacitor C_{FF} should be parallel connected to the R1 resistor, as shown in typical application Figure3, to improve output voltage noise and PSRR in XX mode.

Output Current Limit

The internal output current of the ET52HS11XX is limited to 300mA (typical value), which is measured by the voltage drop across 90% of the nominal V_{OUT}. If the output voltage is directly short circuited to ground (V_{OUT} = 0V), the short-circuit protection will limit the output current to 300mA (typical value).

At the same time, it is required that there is sufficient margin between the starting current design of the front-end power supply and the output current limit to avoid the chip entering over-current protection at the moment of starting. Current limiting and short-circuit protection will function within the recommended operating temperature and input voltage range.

Thermal Shutdown

When the chip temperature exceeds the thermal shutdown threshold (typical value of T_{TSD} is 150°C), a shutdown event will be triggered and the device will be disabled. The IC will remain in this state until the chip temperature drops below the thermal shutdown reset threshold (typical value is 130°C). If the IC temperature drops below 130°C, LDO will enable again.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$\mathbf{P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}} \qquad \textbf{(2)}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

The power consumption under given application conditions can be calculated using the following formula:

$$\mathbf{P_D = V_{IN} \times I_{GND} + (V_{IN} - V_{OUT}) \times I_{OUT}} \qquad \textbf{(3)}$$

power supply rejection ratio

This device has a very high-power supply rejection ratio. If necessary, PSRR at higher frequencies in the 100kHz~10MHz range can be improved by selecting output capacitors and appropriate PCB layout.

Startup Time

This value is defined as the time from pin EN reaching the enable threshold voltage to pin OUT rising to 90% of the nominal output voltage, depending on the output voltage value, output capacitance, ambient temperature, and EN voltage rise time.

At the moment when the input voltage is powered on, the output voltage will be established with 90% accuracy in about 2ms, and 99% output accuracy is related to the load type, showing either over damping or under damping, and will be established within 10s.

PCB Layout Guide

To achieve good transient performance and regulation characteristics, C_{IN} and C_{OUT} capacitors should be placed as close as possible to the corresponding pins of the device and use wide PCB routing. The larger the copper area connected to the pin, the greater the thermal resistance of the device. The actual power consumption can be calculated by formula 3. The heat dissipation pad can be connected to a large GND plane to improve power consumption and reduce device temperature.

Absolute Maximum Ratings

Symbol	Parameters	Symbol	Symbol
V_{IN}	Input Voltage(IN Pin)(1)	-0.3 to 13.2	V
V_{OUT}	Output Voltage(OUT Pin)	-0.3 to 11	V
V_{EN}	Input Voltage (EN Pin)	-0.3 to 6	V
$T_{J(MAX)}$	Maximum Operating Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
V_{ESD} (2)	Human Body Model	±2000	V
	Charged Device Model	±1000	V

Note1: For safe operation, please refer to the electrical characteristics.

Note2: This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per JEDEC JS-001;
CDM tested per JEDEC JS-002;

Thermal Characteristics

Symbol	Parameters	Value		Unit
		SOT23-5	DFN4	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	193	216	°C/W
$R_{\theta JC(TOP)}$	Thermal Resistance, Junction to the Top of the Case	102	161	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	45.5	162	°C/W
Ψ_{JT}	Thermal Resistance, Junction to the Top of the Package	8.5	5	°C/W
Ψ_{JB}	Thermal Resistance, Junction to the Bottom of the Package	45	161	°C/W
$R_{\theta JC(BOT)}$	Thermal Resistance, Junction to Case	n/a	123	°C/W

Recommended Operating Conditions

Symbol	Parameters	Rating	Unit
V_{IN}	Input Voltage (IN Pin)	2.2 to 12	V
V_{OUT}	Output Voltage	1.2 to 11	V
V_{EN}	Input Voltage (EN Pin)	1.0 to 5.5	V
I_{OUT}	Output Current	0 to 200	mA
T_J	Operating Junction Temperature	-40 to 125	°C

Electrical Characteristics

($V_{IN} = V_{OUT} + 1V$, $V_{EN} = 1.2V$, $I_{OUT} = 10mA$, $C_{IN} = C_{OUT} = 2.2\mu F$. Typical values are at $T_A = 25°C$, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage(3)		2.2		12	V
V_{OUT}	Operating Output Voltage		1.2		11	V
	Operating Voltage Accuracy	$V_{IN} = V_{OUT(NOM)} + 1V$, $0mA \le I_{OUT} \le 200mA$		1		%
I_{OUT}	Output Current			200		mA
Reg_{LINE}	Line Regulation	$V_{OUT(NOM)} + 1V \le V_{IN} \le 12V$		0.03		%/V
Reg_{LOAD}	Load Regulation	$I_{OUT} = 1mA$ to $200mA$		0.004		%/mA
V_{DROP}(4)	Dropout Voltage	$I_{OUT} = 150mA$		170		mV
		$I_{OUT} = 200mA$		230		mV
I_{LIMIT}	Current Limit	$V_{OUT} = 0.9V_{OUT(NOM)}$		300		mA
I_{SC}	Short Current Limit	$V_{OUT} = 0V$		300		mA
I_Q	Quiescent Current	$I_{OUT} = 0mA$		300		μA
I_{SD}	Shutdown Quiescent Current	$V_{EN} \le 0.4V$, $V_{IN} = 0V \sim 12V$			1	μA
V_{ENH}	EN Input Logic Low Voltage			1		V
V_{ENL}	EN Input Logic High Voltage			0.4		V
I_{EN}	EN Pin Current	$V_{EN} = 5V$		0.2	0.5	μA
t_{ON}	Output Turn-on Time	$C_{OUT} = 1\mu F$, from Assertion of V_{EN} to $V_{OUT} - 0.95\ V_{OUT(NOM)}$		100		μs
PSRR (5)	Power Supply Rejection Ratio	$C_{IN} = 100nF$, $I_{OUT} = 10mA$, $f = 100Hz$		100		dB
		$C_{IN} = 100nF$, $I_{OUT} = 10mA$, $f = 1KHz$		95		dB
		$C_{IN} = 100nF$, $I_{OUT} = 10mA$, $f = 10KHz$		85		dB
		$C_{IN} = 100nF$, $I_{OUT} = 10mA$, $f = 100KHz$		60		dB
		$C_{IN} = 100nF$, $I_{OUT} = 10mA$, $f = 1MHz$		40		dB
e_N (5)	Output Noise Voltage	$f = 10Hz$ to $100KHz$, $I_{OUT} = 10mA$		3		μVrms
T_{TSD} (5)	Thermal Shutdown Threshold	T_J Rising		150		°C
T_{HYS} (5)	Thermal Shutdown Hysteresis	T_J Falling from Shutdown		20		°C
R_{DIS}	Output Discharge Resistor	$V_{EN} < 0.4V$		1000		Ω

Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{TRLN} (5)	Line Transient Response	$V_{IN} = V_{OUT(NOM)} + 1V$ to $(V_{OUT(NOM)} + 1.6V)$ in 30μs, $I_{OUT} = 1mA$	-1			mV
		$V_{IN} = V_{OUT(NOM)} + 1.6V)$ to $(V_{OUT(NOM)} + 1V)$ in 30μs, $I_{OUT} = 1mA$			1	mV
V_{TRLD} (5)	Load Transient Response	I_{OUT} = 1mA to 150mA in 10μs	-10			mV
		I_{OUT} = 150mA to 1mA in 10μs			40	mV

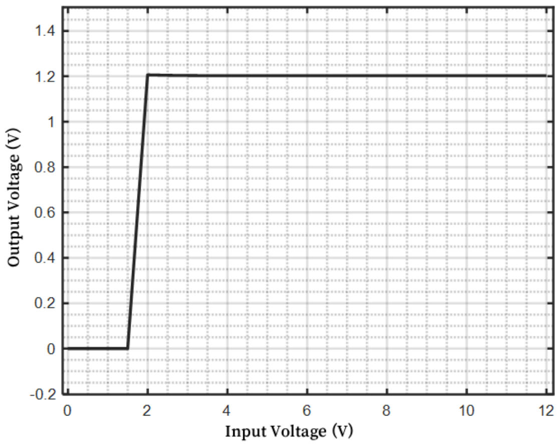
Note3: Here V_{IN} means internal circuit can work normal. If $V_{IN} < V_{OUT}$, Output voltage follows V_{IN} (I_{OUT} = 1mA), circuit is safety.

Note4: V_{DROP} FT test method: test the V_{OUT} voltage at $V_{SET} + V_{DROP\_MAX}$ with 200mA output current.

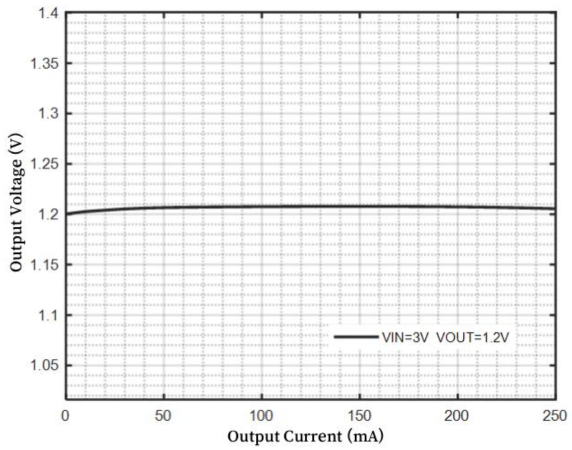
Note5: Guaranteed by design and characterization. not a FT item.

Typical Characteristics

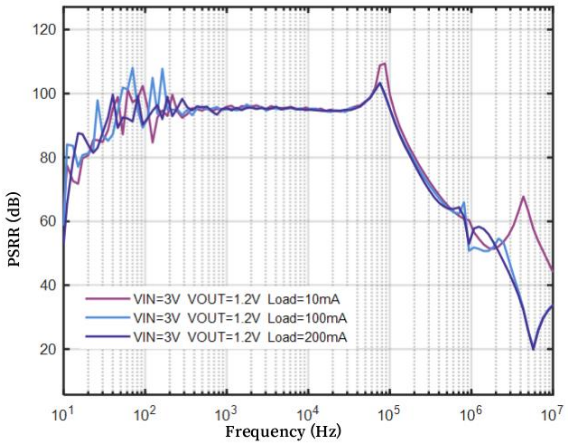
(V_{IN} = V_{OUT} + 1V, V_{EN} = 1.2V, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 2.2μF. Typical values are at T_A = 25°C, unless otherwise noted)



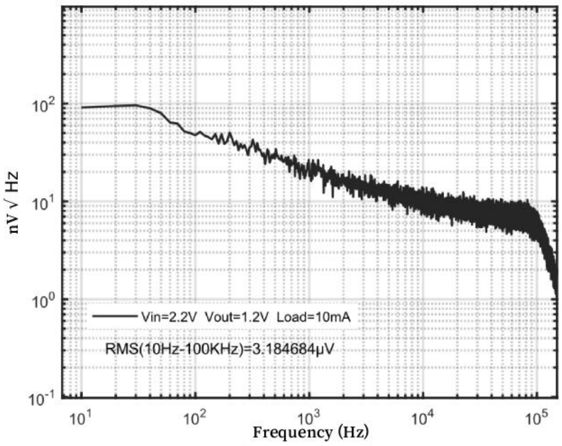
Output Voltage VS Input Voltage



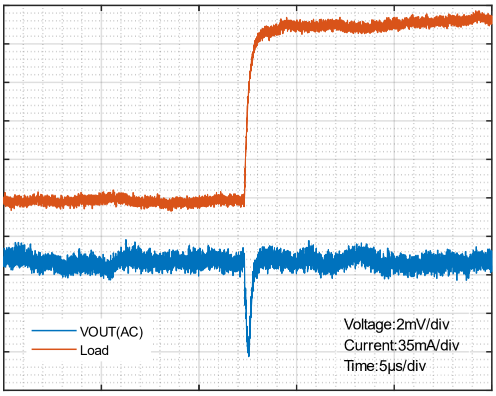
Output Voltage VS Output Current



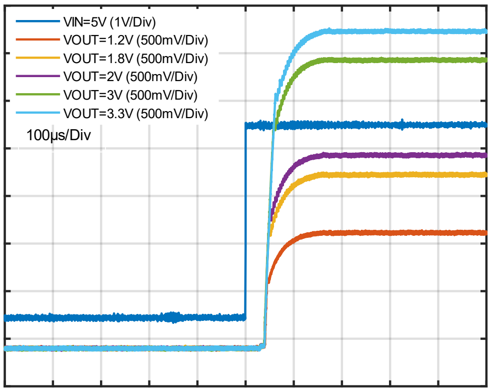
PSRR



Noise



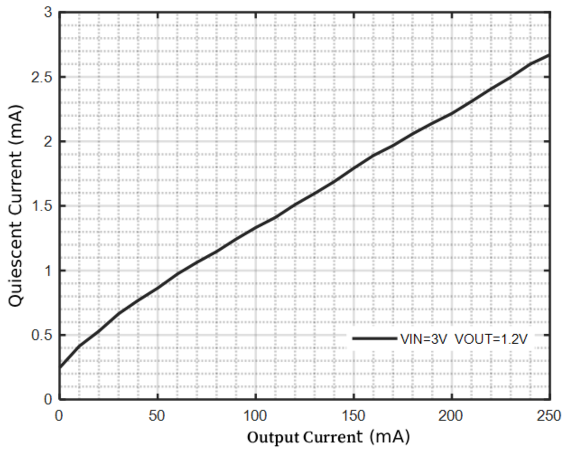
Load Transient



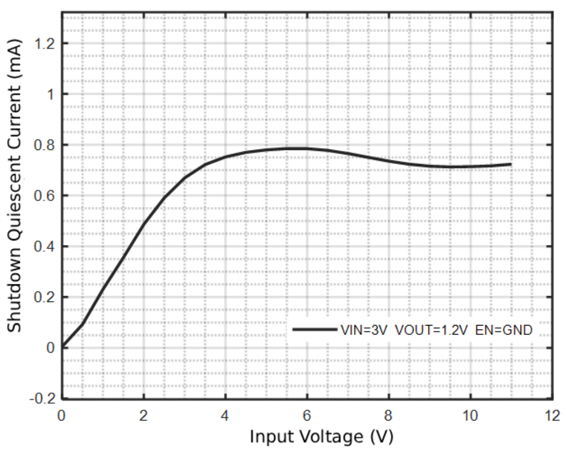
Turn-on Time

Typical Characteristics (Continued)

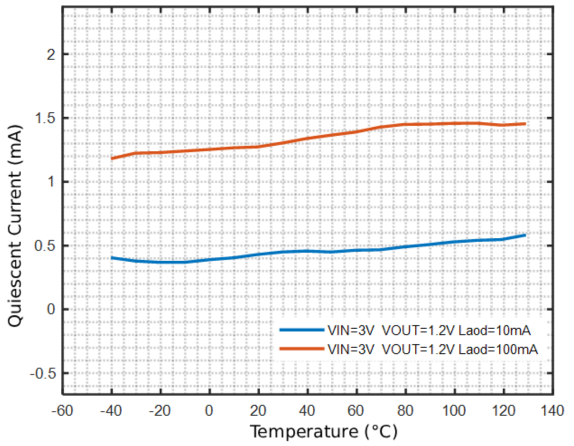
(V_{IN} = V_{OUT} + 1V, V_{EN} = 1.2V, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 2.2μF. Typical values are at T_A = 25°C, unless otherwise noted)



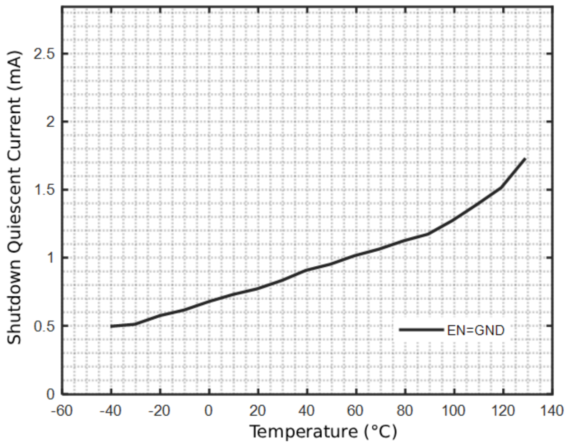
Quiescent Current VS Output Current



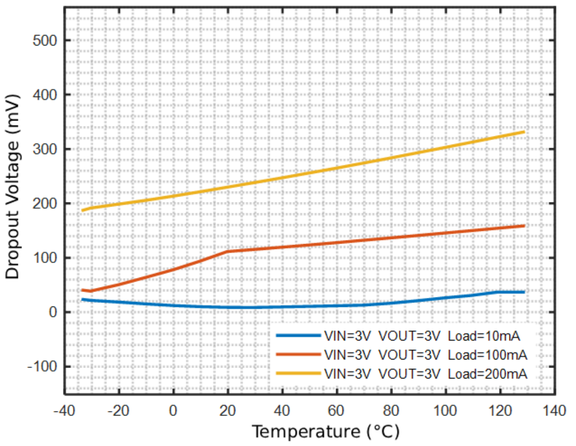
Shutdown Quiescent Current VS Input Voltage



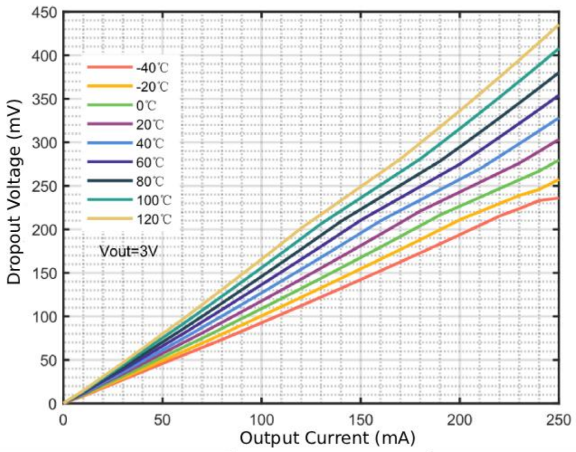
Quiescent Current VS Temperature



Shutdown Quiescent Current VS Temperature

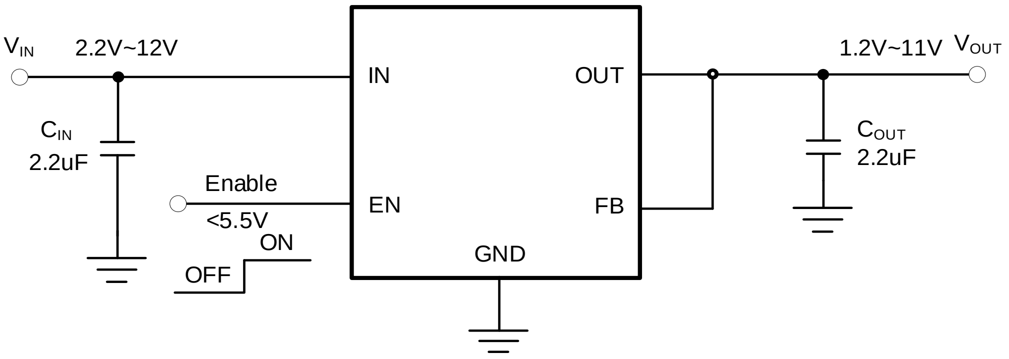


Dropout Voltage VS Temperature

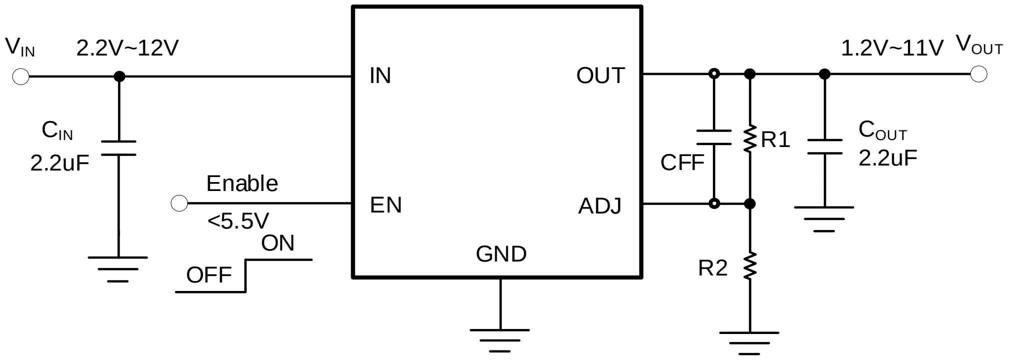


Dropout Voltage VS Output Current

Application Circuits



Fix Output Version

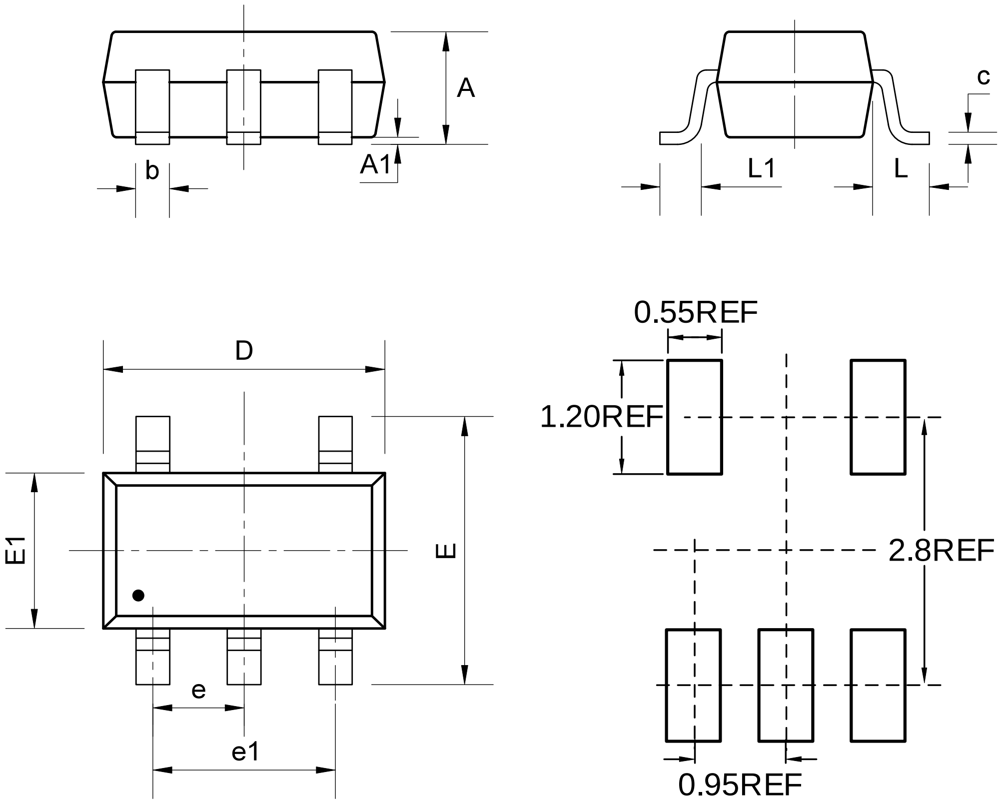


Adjustable Output Version

Figure3. Application Circuits

Package Information

SOT23-5 (1.6mm × 2.9mm)

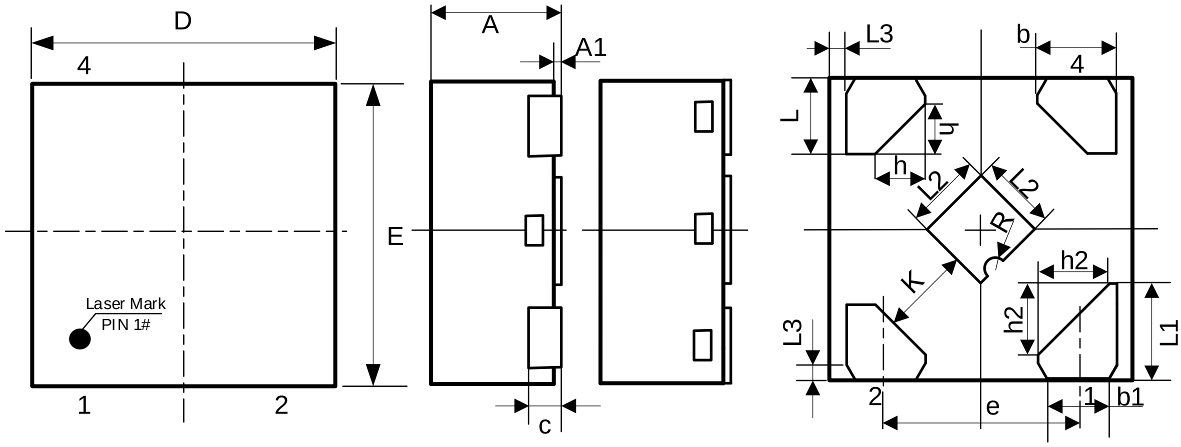


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.45
A1	0.00	-	0.15
b	0.28	0.35	0.50
c	0.08	0.15	0.22
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.60REF		
L1	0.30	0.45	0.60

DFN4 (1mm x 1mm)



Top View Side View Bottom View

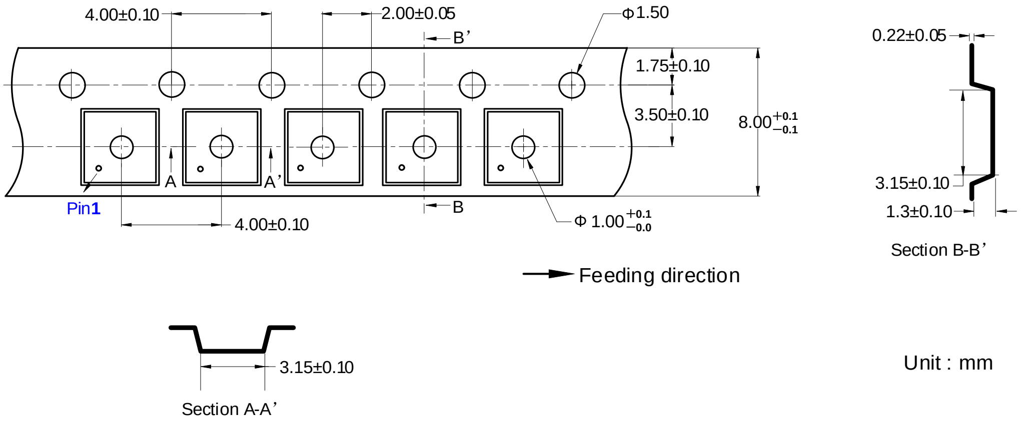
COMMON DIMENSIONS

(Unit: mm)

SIZE LABEL	MIN	NOM	MAX	SIZE LABEL	MIN	NOM	MAX
A	0.34	0.37	0.40	L	0.20	0.25	0.30
A1	0.00	0.02	0.05	L1	0.27	0.32	0.37
b	0.20	0.25	0.30	L2	0.20	0.25	0.30
b1	0.18 REF			L3	0.05 REF		
c	0.127 REF			h	0.17 REF		
D	0.95	1.00	1.05	h2	0.24 REF		
E	0.95	1.00	1.05	K	0.32 REF		
e	0.65 BSC			R	0.05 REF		

Tape Information

SOT23-5 (1.6mm × 2.9mm)



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-07-01	Official Version	Zhang wang	Yang xiaoxu	Liu jiaying