Adjustable Voltage Monitor

General Description

The ET3895B27T low power voltage detector provides monitoring of battery, power-supply, and regulated system voltages. The devices is a very small supervisory circuits that monitor voltages greater than 2.7V with a 0.25% (typical) threshold accuracy and offer adjustable delay time using external capacitors.

The ET3895B27T is available in ultra-small SOT23-5 package and is fully specified the temperature range of T_A = -40°C to 85°C.

Features

- Internally Fixed Threshold 2.7V
- Operate from V_{CC} of 1.7V to 6.5V
- Threshold Accuracy: 1% Over Temperature
- Capacitor-Adjustable Delay Time
- Low Quiescent Current is 8μA Typical
- Temperature Range from -40°C to 85°C
- Package Information:

Part No.	Package	Packing Option	MSL
ET3895B27T	SOT23-5	Tape and Reel, 3k/Reel	Level 3

Application

- Automotive
- DSPs, Microcontrollers and Microprocessors
- Notebook and Desktop Computers
- PDAs and Handheld Products
- Portable and Battery-Powered Products
- Medical Equipment
- FPGAs and ASICs

Pin Configuration

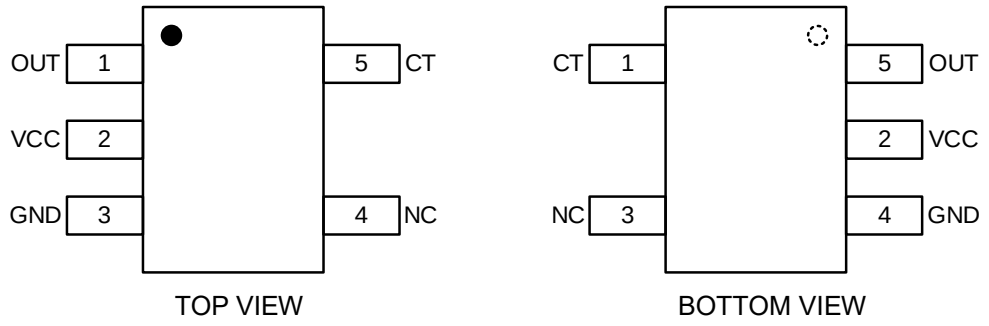


Figure1.

Pin Function

Pin No.	Pin Name	I/O	Pin Function
1	OUT	O	OUT is an push-pull output that is immediately driven low after V_{CC} falls below V_{TH}. OUT goes high after the capacitor-adjustable delay time when V_{CC} is greater than (V_{TH} + V_{HYS}).
2	VCC	I	Power supply input. Connect a 1.7V to 6.5V supply to V_{CC} to power the device. It is good analog design practice to place a 0.1μF ceramic capacitor close to this pin.
3	GND	-	Ground Pin.
4	NC	I	Not connected.
5	CT	I	Capacitor-adjustable delay. The CT pin offers a user-adjustable delay time. Connecting this pin to a ground referenced capacitor sets the delay time for V_{CC} rising above (V_{TH} + V_{HYS}) to OUT asserting. $t_{pd(r)}$ (s) = [C_{CT} (μF) × 6] + 75μs

Block Diagram

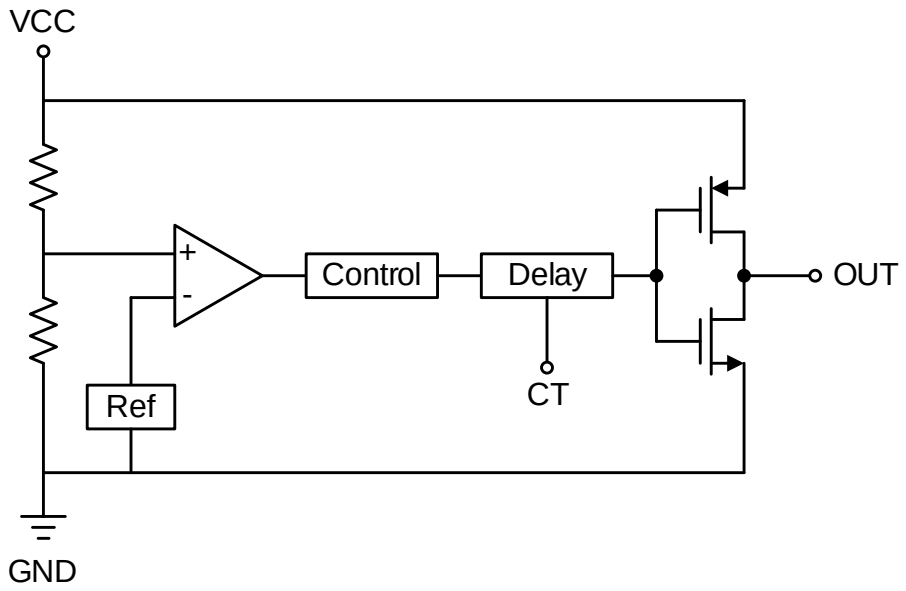


Figure2. ET3895B27T Block Diagram

Operation and Application Description

The ET3895B27T is a ultra-small supervisory circuits. When the VCC pin rises above (V_{TH} + V_{HYS}), the output asserts (OUT goes high) after the capacitor-adjustable delay time.

Feature Description

The ET3895B27T provide push-pull outputs. The logic high level of the outputs is determined by the VCC pin voltage. With this configuration, pull-up resistors are not required and some board area can be saved. However, all the interface logic levels must be examined. All the OUT connections must be compatible with the VCC pin logic level.

The OUT outputs are defined for a V_{CC} voltage higher than 0.8V_{CC}. Table 1 are truth tables that describe how the outputs are asserted or de-asserted. When the conditions are met, the device changes state from de-asserted to asserted after a preconfigured delay time. However, the transitions from asserted to de-asserted are performed almost immediately with minimal propagation delay of 8 us (typical).

Conditions	Output	Status
VCC< V_{TH}	OUT= Low	Output not asserted
VCC > V_{TH}	OUT = High	Output asserted after delay

Table 1. ET3895B27T Truth Table

Power supply input (VCC)

The VCC pin allows any system voltage above V_{TH} to be monitored. If the voltage at the VCC pin exceeds (V_{TH} + V_{HYS}), then the output is asserted after the capacitor-adjustable delay time elapses. When the voltage at the VCC pin drops below V_{TH} , then the output is de-asserted. The comparator has a built-in hysteresis to ensure smooth output assertions and de-assertions.

The ET3895B27T monitor the voltage at V_{CC} with the use of Internal resistor divider, as shown in Figure 3.

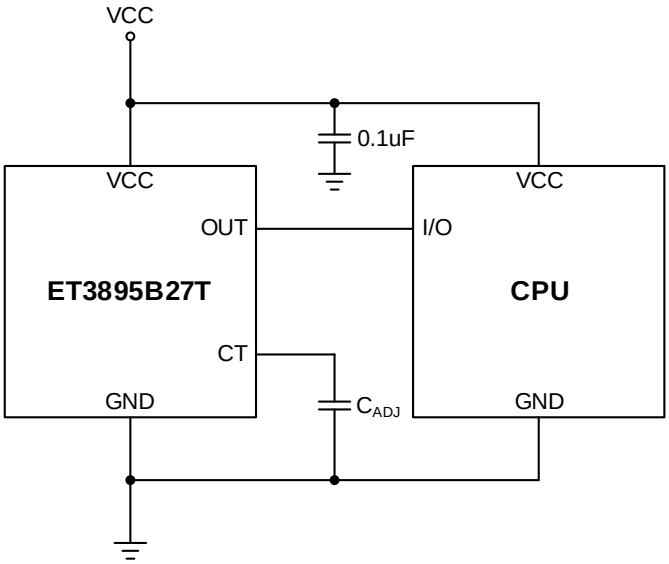


Figure 3. Using ET3895B27T to Monitor User-Defined Threshold Voltage

Output Pin (OUT)

In a typical ET3895B27T application, the OUT outputs are connected to a reset/enable input of the processor (DSP, CPU, FPGA, ASIC, and so on) or connected to the enable input of a voltage regulator.

Output Delay Time Pin (CT)

To program a user-defined, adjustable delay time, an external capacitor must be connected between the CT pin and GND. If the CT pin is left open, there will be a delay of 75us. The adjustable delay time can be calculated through Equation 1:

$$\mathbf{tpd(r)\ (s) = [C_{CT}(\mu F) \times 6] + 75\mu s} \qquad (1)$$

The reset delay time is determined by the time it takes an on-chip, precision 206.7nA current source to charge the external capacitor to 1.24V. When V_{CC} > (V_{TH} + V_{HYS}), the internal current sources are enabled and begin to charge the external capacitors. When the CT voltage on a capacitor reaches 1.24V, the corresponding OUT is asserted. Note that a low-leakage type capacitor (such as ceramic) should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

The more precise of delay time can be calculated through Equation 2:

$$\mathbf{tpd(r)\ (s) = [C_{CT}\ (\mu F) \times 6] *(206.7nA/I_{CT})*(V_{CT}/1.24)+ 75\ \mu s} \qquad (2)$$

I_{CT} is the CT pin charge current;

V_{CT} is the CT pin comparator threshold voltage.

Immunity To VCC Pin Voltage Transients

The ET3895B27T is relatively immune to short negative transients on the V_{CC} pin. Sensitivity to transients depends on threshold overdrive.

PCB Layout Guide

Follow these guidelines to lay out the printed-circuit-board (PCB) that is used for the ET3895B27T.

Place the V_{CC} decoupling capacitor close to the device.

Avoid using long traces for the V_{CC} supply node. The V_{CC} capacitor (C_{VCC}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum V_{CC} voltage.

Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range from 1.7V to 6.5V. Though not required, it is good analog design practice to place a 0.1uF ceramic capacitor close to the VCC pin.

Single-Rail Monitoring

The ET3895B27T can be used to monitor the supply rail for devices such as digital signal processors (DSPs), central processing units (CPUs), or field-programmable gate arrays (FPGAs). The downstream device is enabled by the ET3895B27T once the voltage on the VCC pin is above threshold voltage minus the hysteresis voltage (V_{TH} + V_{HYS}) set by the resistor divider. The downstream device is disabled by the ET3895B27T when V_{CC} is falls below the threshold voltage V_{TH}.

Detailed Design Procedure

If an output delay time is required, connect a capacitor from CT to GND; see the Output Delay Time Pin (CT) section for more information. If no CT cap is connected, the delay time is 75us.

Absolute Maximum Ratings

Parameter	Rating	Unit
VCC Voltage	-0.3 to 7.0	V
CT, OUT Voltage	-0.3 to V_{CC} + 0.3	V
OUT Current	-10 to 10	mA
Power Dissipation	200	mW
Package Thermal Resistance (θ_{JA})	250	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-65 to 150	°C

Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Input supply voltage	V_{CC}	1.7	6.5	V
OUT pin voltage	V_{OUT}	0	V_{CC}	V
OUT pin current	I_{OUT}	0.0003	1	mA

Electrical Characteristics

V_{CC} = 1.7V to 6.5V, T_A = -40°C to +85°C, unless otherwise specified.

Typical values are at V_{CC} = 3.3V and T_A = +25°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Operating voltage range	T_A = 0°C to 85°C	1.7		6.5	V
V_{POR}	Power-on reset voltage	$V_{OL\ (MAX)}$ = 0.2V , I_{OUT} =15μA			1	V
I_{CC}	Supply current (into VCC pin)	V_{CC} = 3.3V , no load		7.5	11	uA
		V_{CC} = 6.5V , no load		9.5	11	
V_{TH}	Reset Threshold	V_{CC} falling	2.673	2.7	2.727	V
V_{HYS}	Hysteresis voltage	V_{CC} rising		0.05*V_{TH}		V
I_{CT}	CT pin charge current		173.3	206.7	233.3	nA
V_{CT}	CT pin comparator threshold voltage		1.18	1.24	1.28	V
R_{CT}	CT pin pull-down resistance			200		Ω

Timing Requirements

V_{CC} = 1.7V to 6.5V, T_A = -40°C to +85°C, unless otherwise specified.

Typical values are at V_{CC} = 3.3V and T_A = +25°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{pd(r)}$	VCC (rising) to VCC-OUT propagation delay	$V_{(CC)}$ rising, $C_{(CT)}$ = open		75		us
		$V_{(CC)}$ rising, $C_{(CT)}$ = 4.7nF		28.3		ms
$t_{pd(f)}$	VCC (falling) to VCC-OUT propagation delay	$V_{(CC)}$ falling		8		us
t_{star}	Start-up delay(1)			50		us

Notes：

1. During power on, V_{CC} must exceed 1.7V for at least 50us (plus propagation delay time, $t_{pd(r)}$) before output is in the correct state.

Timing Diagram

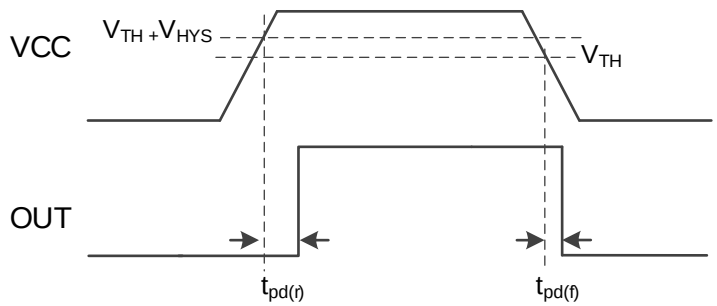


Figure 4. ET3895B27T Timing

Application Circuits

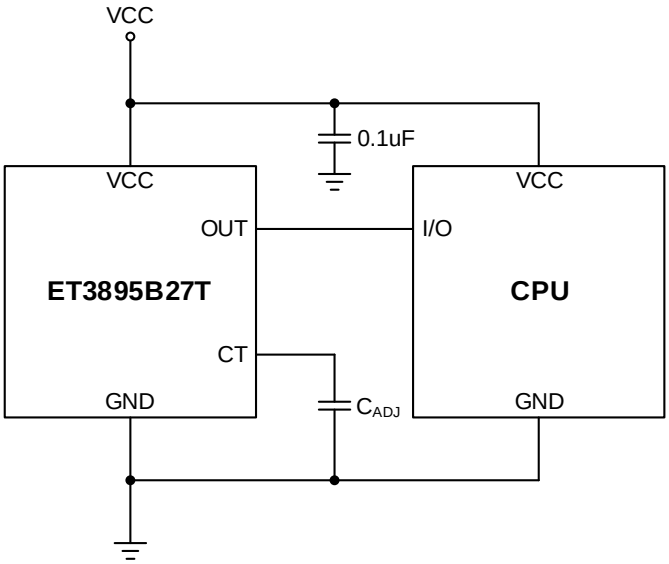
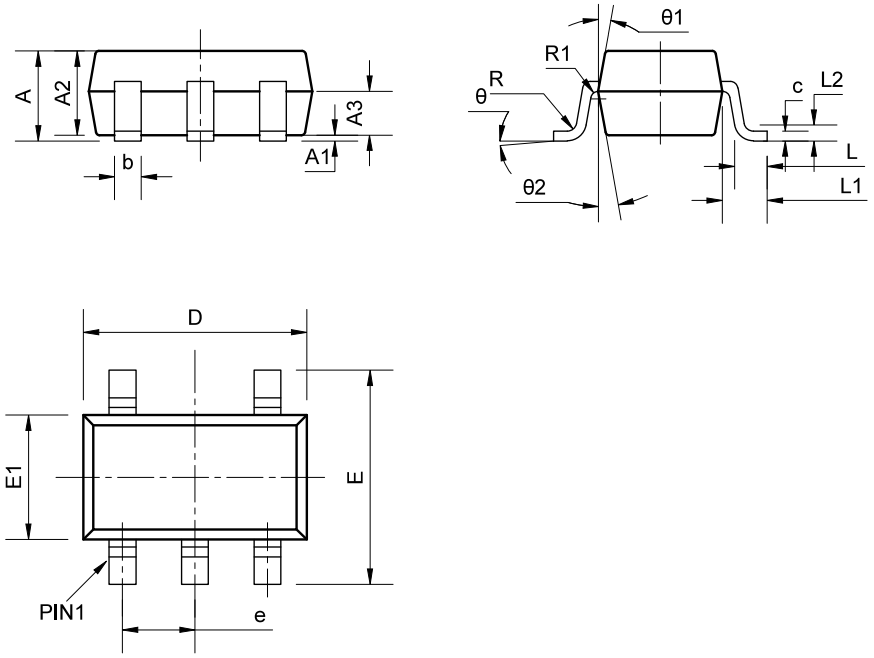


Figure 5. ET3895B27T Typical Application

Package Dimension



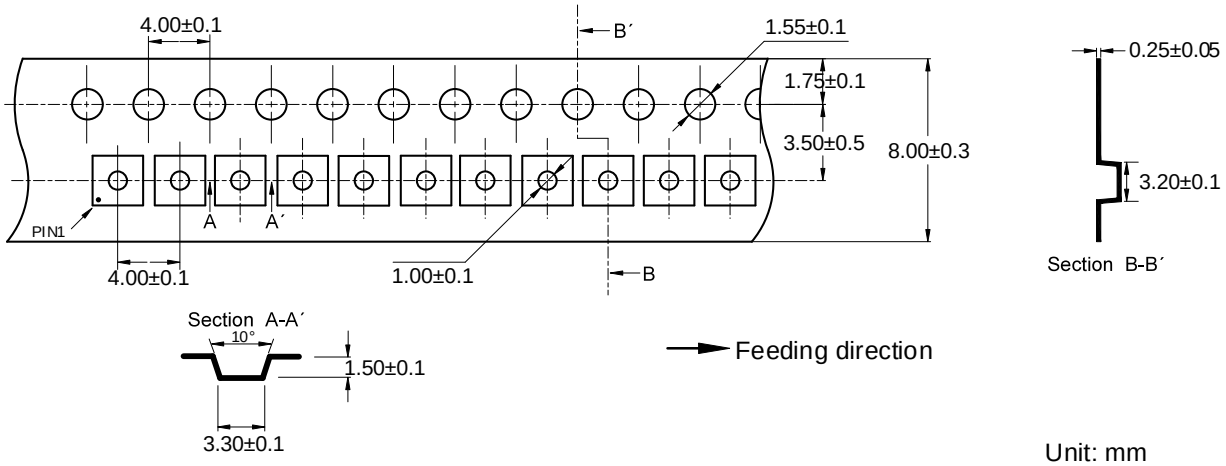
COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

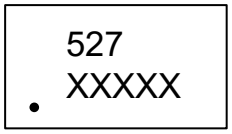
SYMBOL	MIN	NOM	MAX
A	-	-	1.26
A1	0.01	0.06	0.11
A2	1.05	1.10	1.15
A3	0.62	0.65	0.68
b	-	0.35	-
c	-	0.127	-
D	2.87	2.92	2.97
E	2.70	2.80	2.90
E1	1.55	1.60	1.65
e		0.95BSC	
L	0.32	0.40	0.48
L1		0.59REF	
L2		0.25BSC	
R	-	0.10	-
R1	-	0.10	-
θ	0°	-	6°
θ1	-	10°	-
θ2	-	12°	-

Tape Information

SOT23-5



Marking Information



527 - Part Number

XXXXX - Tracking Number

Note：X (Tracking Number) is variable, according to the wafer lot number.

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-08-26	Original Version	Wanghd	Liuyg	Liujy