Single SPDT Analog Switch

General Description

The ET3328 is an advanced CMOS analog switch with POGO OVP function fabricated in Sub-micron silicon gate CMOS technology. VCC=Max(VCC1,POGO). ET3328 operate state diagram showed as Figure 2.

Features

- Low R_{ON}:
  - R_{ON} (POGO to CHG) = 0.1Ω
  - R_{ON} (POGO to UART) = 4.0Ω
- VCC Voltage:1.65V-5.5V
- OVP_TH: 5.8V
- High Off-Channel Isolation
- Low Standby Current
- Low Distortion
- Break-Before-Make (TBBM) switching
- Part No. and Package Information:

Part No.	Package	Packing Option	MSL
ET3328	QFN14L (1.8mm×1.4mm)	Tape and Reel ,3K	Level 1

Application

- Smart Phones
- Tables
- USB Type-C
- PC/Notebook

Pin Configuration

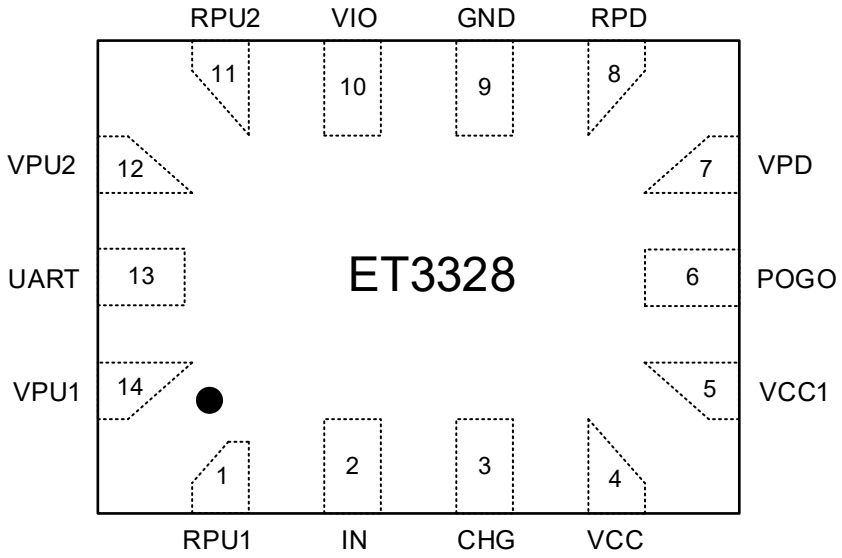


Figure 1. Top View

Pin Function

Pin No.	Pin Name	Description
1	RPU1	Pull-up Control Pin
2	IN	Logic Control Pin
3	CHG	Analog Switch Input
4	VCC	Power supply (Connect to POGO in internal circuit)
5	VCC1	Power Supply
6	POGO	Analog Switch Common (Connect to VCC in internal circuit)
7	VPD	QOD Pin of POGO
8	RPD	QOD Control Pin
9	GND	Ground
10	VIO	QOD Power Supply
11	RPU2	Pull-up Control Pin
12	VPU2	Pull-up Pin
13	UART	Analog Switch Input
14	VPU1	Pull-up Pin

Operate state diagram

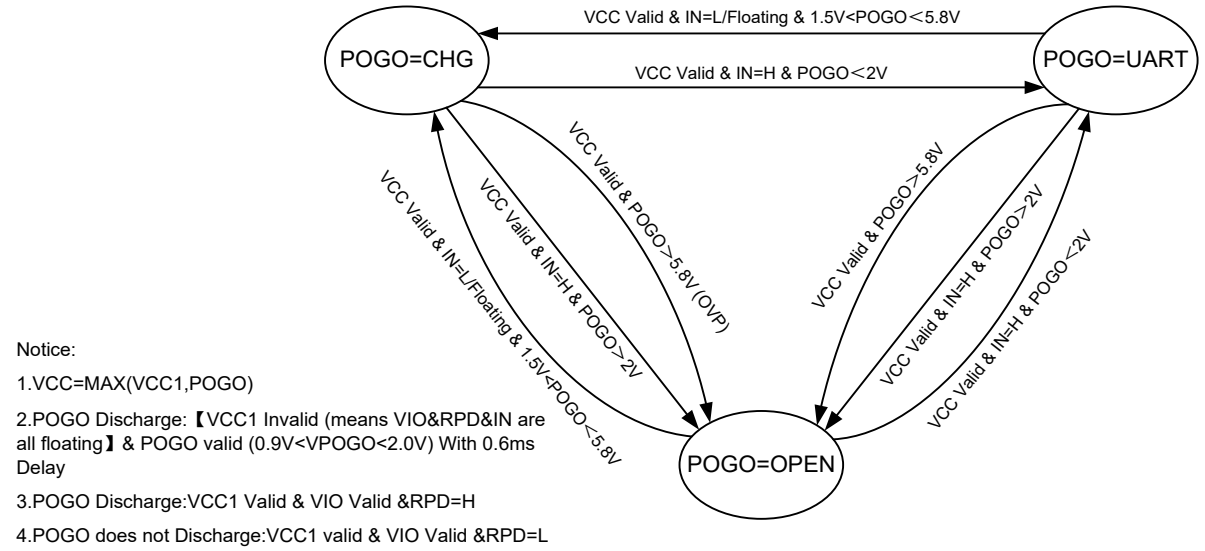


Figure 2. ET3328 Operate state diagram

Truth Table

VCC1	VCC	RPD	VIO	IN	V_{POGO}	Function
Invalid	VCC=POGO	Floating	Floating	Floating	0.9V<V_{POGO}<2.0V	POGO Discharge
Invalid	VCC=POGO	Floating	Floating	Floating	2.0V<V_{POGO}<5.8V	POGO Connected to CHG
Valid	VCC=POGO	H	Valid	/	/	POGO Discharge
Valid	VCC=POGO	L	Valid	/	/	POGO not Discharge
Valid	/	/	/	H	V_{POGO}>2V	POGO Open
/	VCC=POGO	/	/	H	V_{POGO}>2V	POGO Open
Valid	VCC=POGO	/	/	H	V_{POGO}>2V	POGO Open
Valid	/	/	/	/	V_{POGO}>5.8V	POGO Open
/	VCC=POGO	/	/	/	V_{POGO}>5.8V	POGO Open
Valid	VCC=POGO	/	/	/	V_{POGO}>5.8V	POGO Open
Valid	/	/	/	L/Floating	1.5V<V_{POGO}<5.8V	POGO Connected to CHG
Valid	VCC=POGO	/	/	L/Floating	1.5V<V_{POGO}<5.8V	
Valid	/	/	/	H	V_{POGO}<2V	POGO Connected to UART
/	VCC=POGO	/	/	H	V_{POGO}<2V	
Valid	VCC=POGO	/	/	H	V_{POGO}<2V	

The Timing Flow Chart

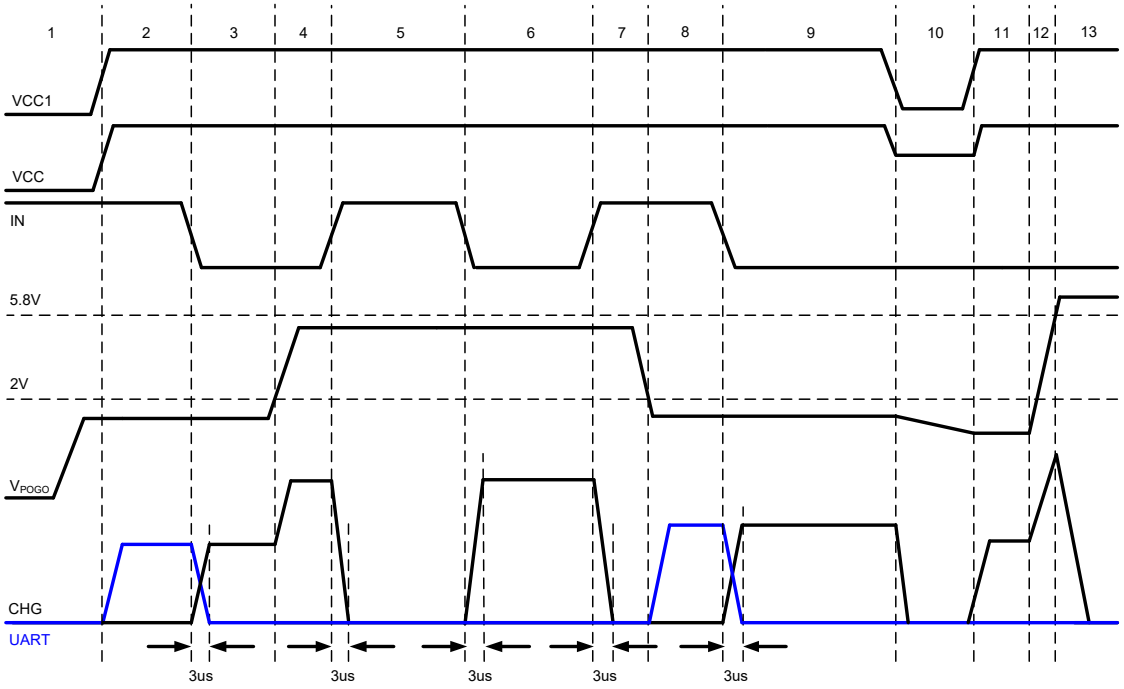


Figure 3. ET3328 Timing Flow

Note:

1.VCC1 Invalid & POGO=0V, the whole circuit do not operate normally;

2.VCC1 Valid, IN=H & POGO<2.0V, POGO=UART;

3.VCC1 Valid & IN=H to L & 1.5V<POGO<2V, POGO=CHG;

4.VCC1 Valid & IN=L & 2V<POGO<5.8V, POGO=CHG;

5.VCC1 Valid & IN=L to H & 2V<POGO<5.8V, POGO OPEN;

6.VCC1 Valid & IN=H to L & 2V<POGO<5.8V, POGO=CHG;

7.VCC1 Valid & IN=L to H & 2V<POGO<5.8V, POGO OPEN;

8.VCC1 Valid & IN=H & POGO<2V, POGO=UART;

9.VCC1 Valid & IN=H to L & 1.5V<POGO<2V, POGO=CHG;

10.VCC1 Invalid (VCC=POGO) & IN=VIO=RPD=Floating& 0.9V<POGO<2V, POGO OPEN, after0.6ms POGO Discharge;

11.VCC1 Valid & IN=L & 1.5V<POGO<2V, POGO=CHG;

12.VCC1 Valid & IN=L & 2V<POGO<5.8V, POGO=CHG;

13.VCC1 Valid & IN=L & POGO>5.8V, POGO OVP Occurred POGO OPEN;

The Timing Flow Chart (Continued)

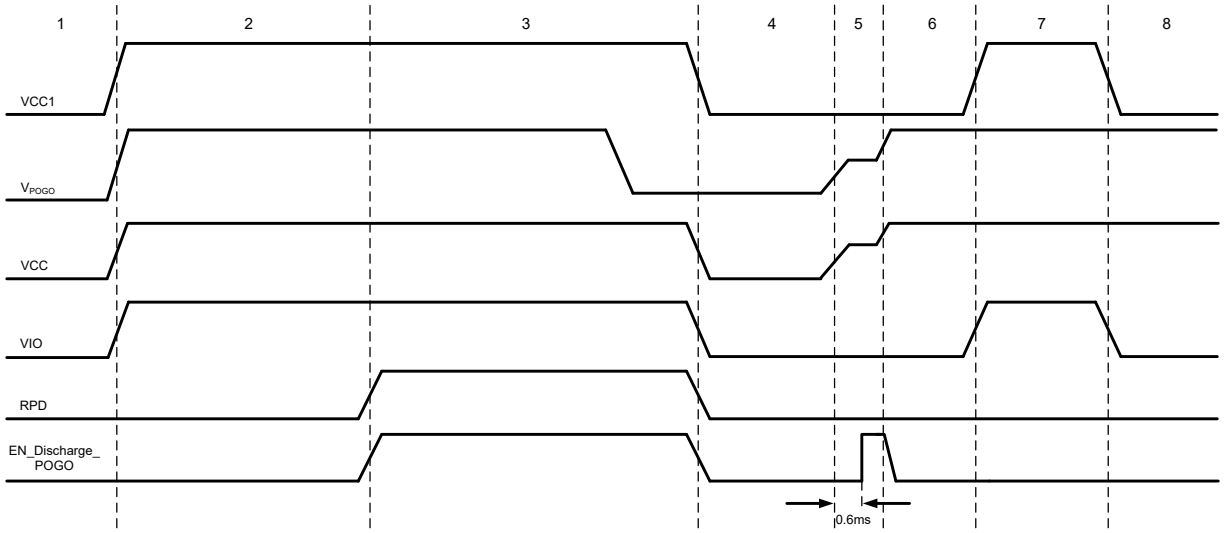


Figure 4. POGO Discharge Timing Flow

Note:

EN_Discharge_POGO=H (Discharge), EN_Discharge_POGO=L (do not Discharge)

1.VCC1 Invalid & POGO=0V, POGO discharge circuit does not operate normally;

2.VCC1 valid & VIO valid & RPD=L, POGO discharge circuit does not discharge;

3.VCC1 valid & VIO valid & RPD=H, POGO discharge circuit discharge without time delay;

4.VCC1 Invalid (VIO=Floating, RPD=Floating) & POGO=0V, POGO discharge circuit does not discharge;

5.VCC1 Invalid (VIO=Floating, RPD=Floating, IN=L/Floating) & POGO from L to H = 0 to (0.9V~2.0V), POGO OPEN and discharge circuit discharge after about 0.6ms time delay;

6.VCC1 Invalid (VIO=Floating, RPD=Floating, IN=L/Floating) & POGO=2.0V~5.8V, POGO connected to CHG;

7.VCC1 valid & VIO valid & RPD=L, POGO discharge circuit does not discharge;

8.VCC1 Invalid (VIO=Floating, RPD=Floating) & POGO=H, POGO discharge circuit does not discharge;

Block Diagram

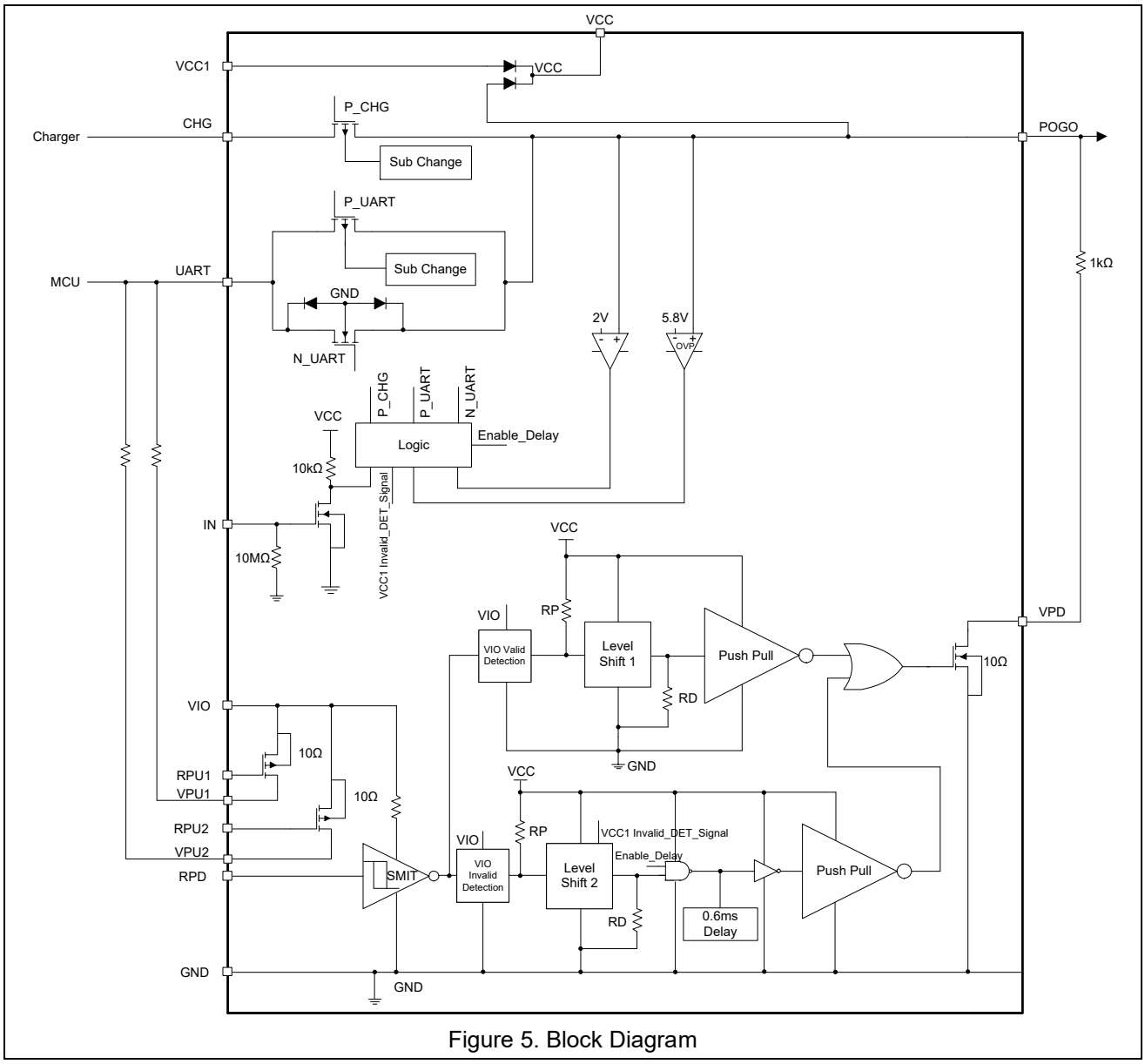


Figure 5. Block Diagram

Absolute Maximum Ratings

Symbol	Pins	Parameter		Value	Unit
V_{CC}	VCC1	Supply Voltage Range		-0.3~7.0	V
	VCC			-0.3~7.0	V
V_{IS}	POGO	Analog Input/Output Voltage		-0.3~7.0	V
	CHG	Analog Input/Output Voltage		-0.3~7.0	V
	UART	Analog Input/Output Voltage		-0.3~7.0	V
$V_{I/O}$	VPU1, VPU2	Pull-up		-0.3~7.0	V
	VIO	RPD Supply Voltage		-0.3~7.0	V
	VPD	Pull-down Voltage		-0.3~7.0	V
V_{IN}	IN	Logic Control Voltage		-0.3~7.0	V
	RPU1, RPU2, RPD	Pull-up/Pull-down Control Voltage		-0.3~7.0	V
T_{STG}		Storage Temperature Range		-65 to 150	°C
T_J		Maximum Operating Junction Temperature		150	°C
HBM		ESD	Human Body Model (1)	±2000	V
CDM			Charge-Device Model (1)	±1000	V
I_{LATCH}		Latch up Current Maximum Rating (1)		±100	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Note1. This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per ESDA/JEDEC JS-001-2017.

CDM tested per ESDA/JEDEC JS-002-2018.

Latch up Current Maximum Rating tested per JEDEC78.

Recommended Operating Conditions

Symbol	Pins	Parameter	Min	Max	Unit
V_{CC}	VCC1	Supply Voltage	1.65	5.5	V
	VCC		1.65	5.5	V
V_{IS}	POGO	Analog Input/Output Voltage	0	5.5	V
	CHG	Analog Input/Output Voltage	1.5	5.5	V
	UART	Analog Input/Output Voltage	0	1.9	V
$V_{I/O}$	VPD	Input/Output Voltage	0	5.5	V
	VPU1, VPU2		0	1.9	V
	VIO		0	1.9	V
V_{IN}	IN	Input Voltage	0	5.5	V
	RPU1, RPU2, RPD		0	1.9	V
T_A		Operating Temperature Range	-40	+85	°C

Electrical Characteristics

Unless otherwise noted, V_{CC}=1.65V to 5.5V, T_A=-40 to 85°C. Typical values are at V_{CC}=5.0V and T_A=25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC1}	Supply Voltage		1.65	5.0	5.5	V
V_{CC}	Supply Voltage		1.65	5.0	5.5	V
Leakage Current						
I_{CC1}	Active Supply Current	V_{CC1}=5.5V, IN=V_{CC1}/GND, Other pin is floating		5.0	12	uA
		V_{CC1}=5.0V, IN=V_{CC1}/GND, Other pin is floating		4.8	11	
		V_{CC1}=2.5V, IN=V_{CC1}/GND, Other pin is floating		3.0	7.0	
		V_{CC1}=1.65V, IN=V_{CC1}/GND, Other pin is floating		2.5	5.0	
I_{CC}	Active Supply Current Of VCC PIN	V_{CC}=5.5V, IN=V_{CC}/GND, Other pin is floating		5.0	12	uA
		V_{CC}=5.0V, IN=V_{CC}/GND, Other pin is floating		4.8	11	
		V_{CC}=2.5V, IN=V_{CC}/GND, Other pin is floating		3.0	7.0	
		V_{CC}=1.65V, IN=V_{CC}/GND, Other pin is floating		2.5	5.0	
I_{ON}	CHG ON Leakage Current	V_{CC1}=5.0V, IN=0V, CHG=1.5V, Other pin is floating		0.25	0.6	uA
		V_{CC1}=5.5V, IN=0V, CHG=5.0V, Other pin is floating		0.8	2.5	
	UART ON Leakage Current	V_{CC1}=IN=5.5V, UART=1.8V, Other pin is Floating		0.3	1.0	
		V_{CC1}=IN=5.0V, UART=1.8V, Other pin is floating		0.3	1.0	
	POGO to CHG ON Leakage Current	V_{CC1}=5.5V, IN=0V, POGO=2.5V, Other pin is floating		0.4	1.2	
		V_{CC1}=5.5V, IN=0V, POGO=5.0V, Other pin is floating		0.8	2.0	
	POGO to UART ON Leakage Current	V_{CC1}=IN=5.5V, POGO=1.8V, Other pin is floating		0.35	1.0	

Electrical Characteristics (Continued)

Unless otherwise noted, V_{CC}=1.65V to 5.5V, T_A=-40 to 85°C. Typical values are at V_{CC}=5.0V and T_A=25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OFF}	CHG OFF Leakage Current	V_{CC1}=IN=2.5V, CHG=2.5V, Other pin is floating		0.01	0.5	uA
		V_{CC1}=IN=5.0V, CHG=5.0V, Other pin is floating		0.01	0.5	
		V_{CC1}=IN=5.5V, CHG=5.5V, Other pin is floating		0.01	0.5	
	UART OFF Leakage Current	V_{CC1}=2.5V, IN=0V, UART=1.8V, Other pin is floating		0.01	0.5	
		V_{CC1}=5.0V, IN=0V, UART=1.8V, Other pin is floating		0.01	0.5	
		V_{CC1}=5.5V, IN=0V, UART=1.8V, Other pin is floating		0.01	0.5	
	POGO OFF Leakage Current	V_{CC1}=IN=5.5V, POGO=2.5V, Other pin is floating		0.4	1.0	
		V_{CC1}=IN=5.5V, POGO=5.0V, Other pin is floating		0.8	2.0	
I_{VIO}	V_{IO}=1.8V, VIO leakage current	V_{IO}=RPU1=RPU2=1.8V		0.01	0.5	uA
I_{IN}	V_{IN}=0~5.5V, IN leakage current, Select Inputs	V_{IN}=V_{CC1}=5.5V		0.5	1.0	uA
Digital Characteristics						
V_{IH_IN}	High-Level Input Voltage, IN	V_{CC1}=1.65V~5.5V	0.9			V
V_{IL_IN}	Low-Level Input Voltage, IN	V_{CC1}=1.65V~5.5V			0.4	V
V_{IH_RPD}	High-Level Input Voltage, RPD	V_{IO}=1.2V	0.9			V
V_{IL_RPD}	Low-Level Input Voltage, RPD	V_{IO}=1.2V			0.4	V
$V_{IH\_RPU1/2}$ (4)	High-Level Input Voltage, RPU1/2	V_{IO}=1.2V	1.2			V
$V_{IL\_RPU1/2}$ (4)	Low-Level Input Voltage, RPU1/2	V_{IO}=1.2V			0.4	V
V_{IH_POGO}	POGO Pin Positive Threshold	V_{CC1}=1.65V~5.5V	1.9	2.0	2.1	V
$V_{IH\_POGO\_HYS}$	POGO Pin Threshold hysteresis	V_{CC1}=1.65V~5.5V		60		mV

Electrical Characteristics (Continued)

Unless otherwise noted, V_{CC}=1.65V to 5.5V, T_A=-40 to 85°C. Typical values are at V_{CC}=5.0V and T_A=25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OVP_POGO}	POGO Pin OVP Positive Threshold	V_{CC1}=1.65V~5.5V	5.6	5.8	6.0	V
$V_{OVP\_POGO\_HYS}$	POGO Pin OVP Threshold hysteresis	V_{CC1}=1.65V~5.5V		250		mV
Resistance						
R_{ON}	On-Resistance (2)(3)	V_{CC1}=5.0V I_{POGO}= -100mA, V_{CHG}=3.3V~5.0V		0.1		Ω
		V_{CC1}=5.0V I_{POGO}= -20mA, V_{UART}=0~1.8V		4.0		
AC Characteristics						
t_{ON}	Turn-On Time (2)	V_{CC1}=5.0V, POGO=1.8V, R_CHG=50Ω, C_CHG=35pF, IN From 5.0V to 0V, t_{ON}=0.9*CHG-0.5*IN Figure 6		2.0		us
		V_{CC1}=5.0V, POGO=1.8V, R_UART=50Ω, C_UART=35pF, IN From 0V to 5.0V, t_{ON}=0.9*UART-0.5*IN Figure 7		0.3		us
t_{OFF}	Turn-Off Time (2)	V_{CC1}=5.0V, POGO=1.8V, R_CHG=50Ω, C_CHG=35pF, IN From 0V to 5.0V, t_{ON}=0.9*CHG-0.5*IN Figure 6		50		ns
		V_{CC1}=5.0V, POGO=1.8V, R_UART=50Ω, C_UART=35pF, IN From 5.0V to 0V, t_{ON}=0.9*UART-0.5*IN Figure 7		40		ns

Electrical Characteristics (Continued)

Unless otherwise noted, V_{CC}=1.65V to 5.5V, T_A=-40 to 85°C. Typical values are at V_{CC}=5.0V and T_A=25°C.

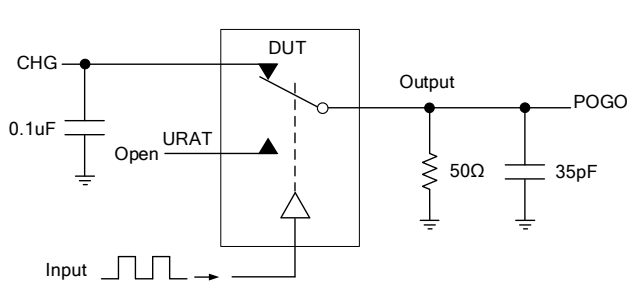
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PD}	POGO-UART t_{PD} (2)	V_{CC1}=5.0V, R_UART=50Ω, C_UART=35pF, POGO From 0V to 1.8V, t_{PD}=0.5*UART-0.5*POGO Figure 8		5		ns
	POGO-CHG t_{PD} (2)	V_{CC1}=5.0V, R_CHG=50Ω, C_CHG=35pF, POGO From 0V to 5.0V, t_{PD}=0.5*CHG-0.5*POGO Figure 9		10		ns
t_{BBM}	Break-Before-Make Time (2)	V_{CC1}=1.65~5.5V C_L=35pF, R_L=50Ω, V_{CHG}=V_{UART}=1.8V Figure 10		2.5		us
T_delay	POGO Discharge Delay	V_{CC1} invalid, V_{IO}=RPD=Floating, IN=L/Floating, V_{CC}=POGO=0.9V~2.0V, V_{PD} connect to POGO with 1kΩ, T_delay=0.5*V_{PD}-0.5*POGO		0.6		ms
BW	On-Channel -3dB Bandwidth or Frequency Response (2)	R_L=50Ω Figure 11		65		MHz
V_{ISO}	POGO-CHG channel (2)	F_{IS} = 100kHz, V_{IN} =GND to V_{CC1} C_L=5pF, R_L= 50Ω V_{IS}=1V_{RMS} Figure 12		-50		dB
	POGO-UART channel (2)	F_{IS} = 100kHz, V_{IN} =GND to V_{CC1} C_L=5pF, R_L= 50Ω V_{IS}=1V_{RMS} Figure 12		-70		dB
Q	Charge Injection Select Input to Common I/O (2)	V_{IN} = 0 or V_{CC1}, R_{IS}=0Ω, C_L=100pF, R_L=1MΩ, Q=C_L×ΔV_{Out} Figure 13		25		pC

Note2. Guaranteed by design.

Note3. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

Note4. Consider the PMOS gate threshold voltage of turn off and turn on.

Timing Diagram



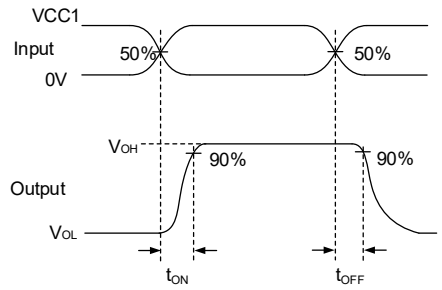
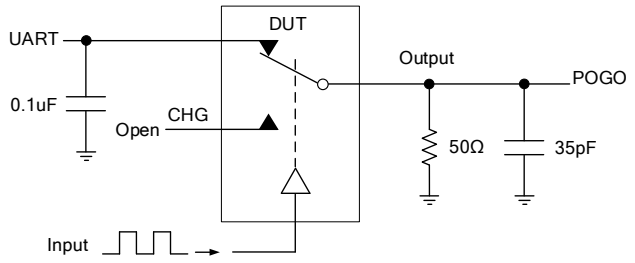


Figure 6. POGO-CHG t_{ON}/t_{OFF}



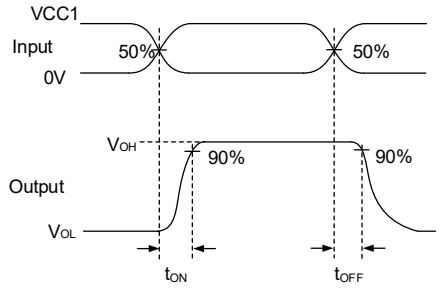
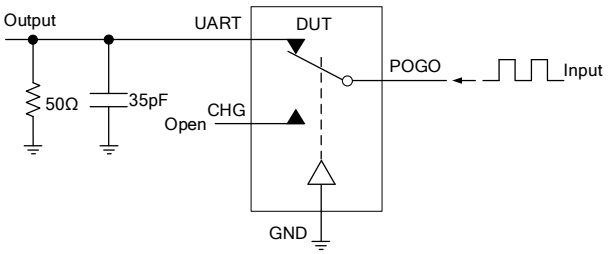


Figure 7. POGO-UART t_{ON}/t_{OFF}



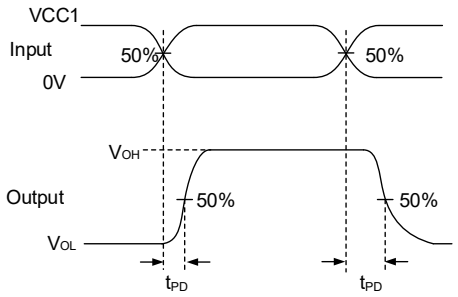
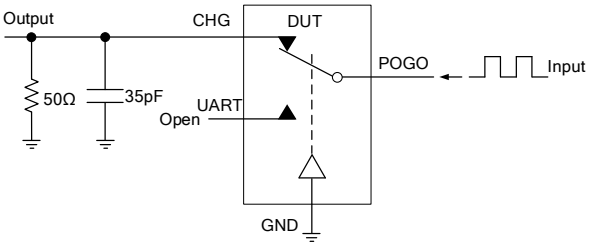


Figure 8. POGO-UART t_{PD}



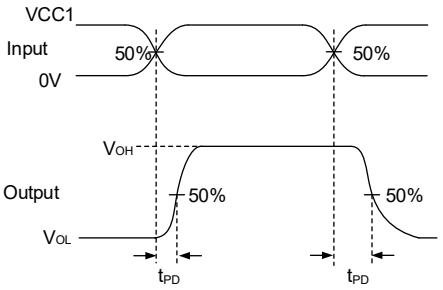


Figure 9. POGO-CHG t_{PD}

Timing Diagram (Continued)

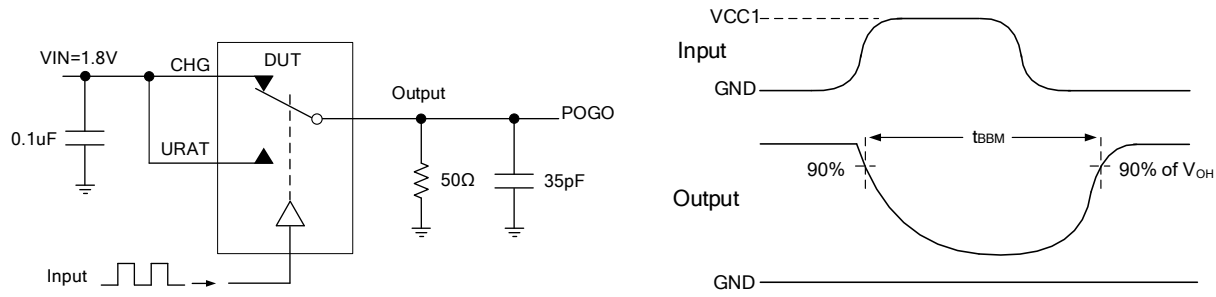


Figure 10. t_{BBM}

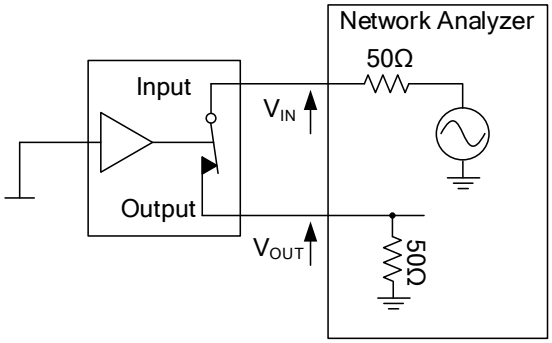


Figure 11. Bandwidth

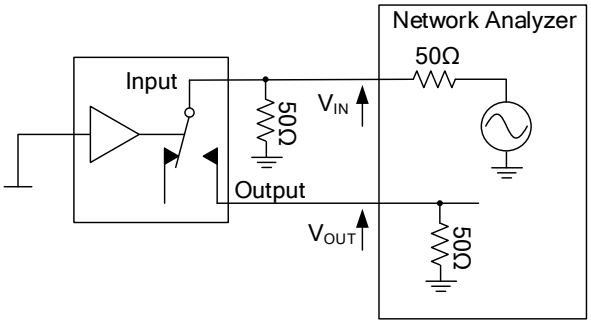


Figure 12. Channel Off Isolation

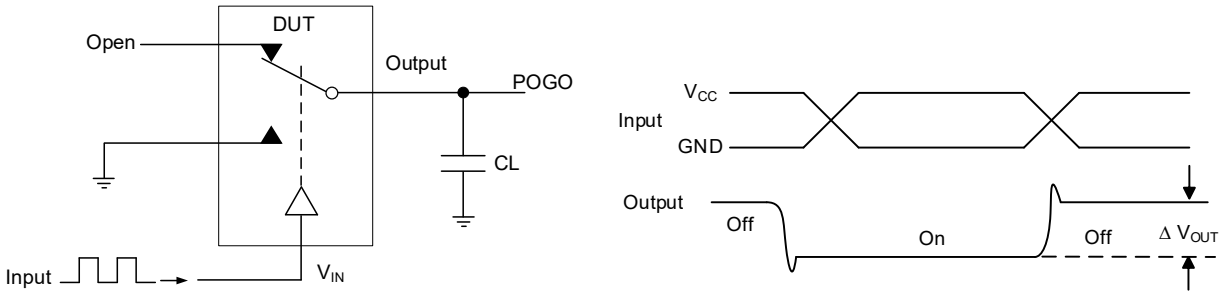


Figure 13. Charge Injection

Application Circuit

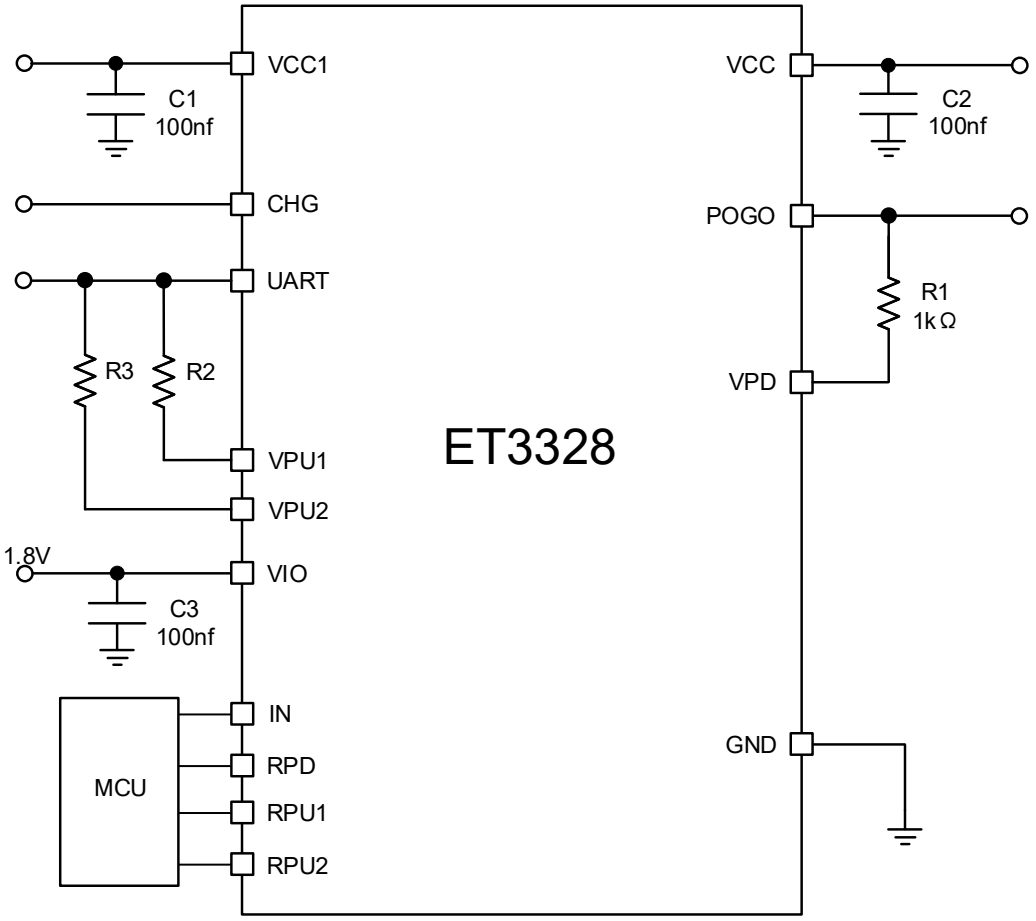
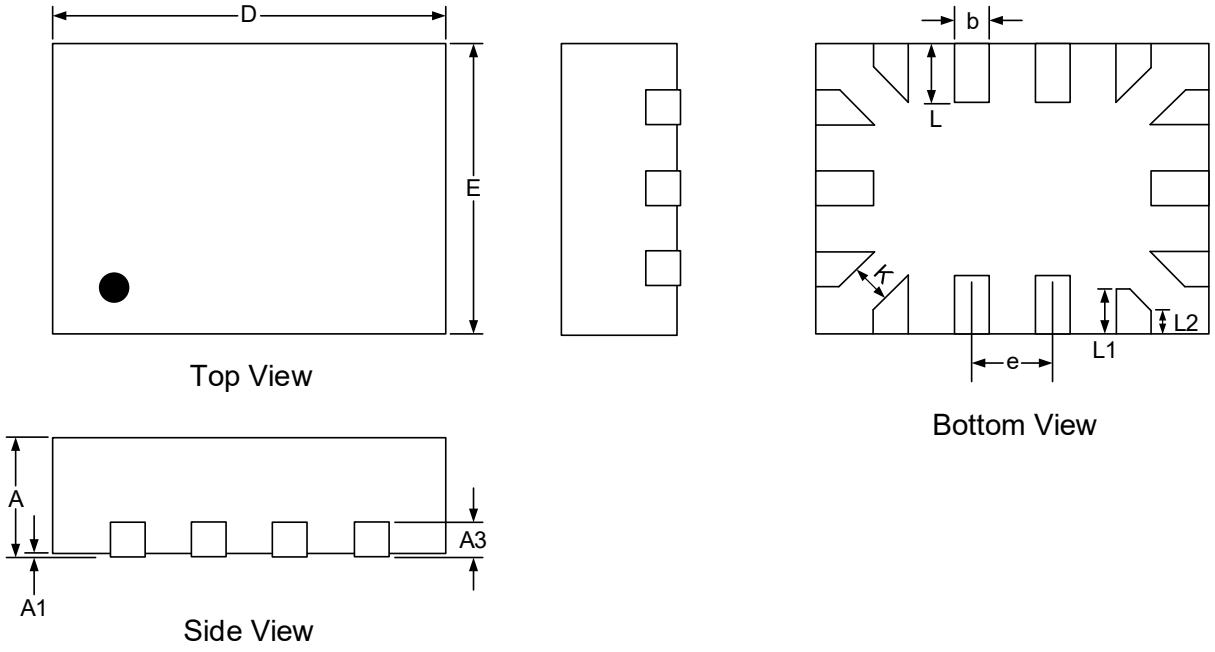


Figure 14. Typical Application Circuit of ET3328

Note. R2=R3=10kΩ and just for reference.

Package Dimension

QFN14L(1.8mm*1.4mm)

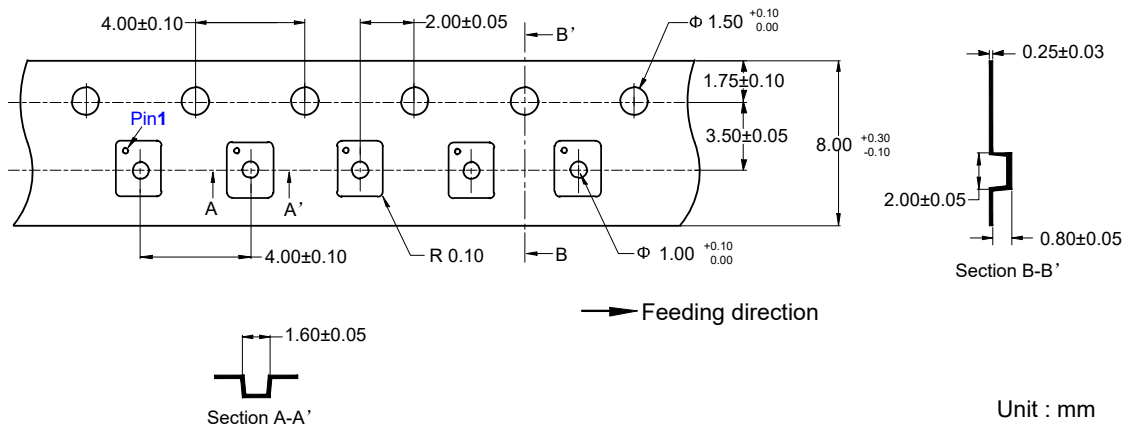


COMMON DIMENSIONS

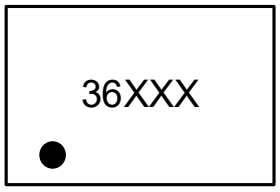
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	-	0.05
A3		0.15 REF	
E	1.35	1.40	1.45
D	1.75	1.80	1.85
b	0.15	0.20	0.25
K		0.20 REF	
L	0.15	0.25	0.35
L1	0.10	0.20	0.30
L2		0.058 REF	
e		0.40 BSC	

Tape Information



Marking Information



36 – Part Number

XXX – Tracking Number

Note：X (Tracking Number) is variable, according to the wafer lot number.

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-01-23	Original Version	Pan Shun Ye	Lu hao	Liu Jia Ying
1.1	2025-03-31	Add V_{IH} and V_{IL} of RPD and RPU1/2	Yin Peng	Lu hao	Liu Jia Ying
1.2	2025-06-25	Update Tape and Marking Information	Pan Shun Ye	Lu hao	Liu Jia Ying
1.3	2025-07-03	Preliminary Version Modify the Discharge Function	Pan Shun Ye	Lu hao	Liu Jia Ying
1.4	2025-09-04	Update Block Diagram	Pan Shun Ye	Lu hao	Liu Jia Ying
1.5	2025-10-28	Update Recommend Operation Voltage Table Spec	Pan Shun Ye	Lu hao	Liu Jia Ying