Over-Voltage and Over-Current Protection IC and Li+ Charger Front-End Protection IC with Reverse Block

General Description

The ET20125 device is a highly integrated circuit (IC) designed to provide protection to Li-ion batteries from failures of the charging circuit. The device continuously monitors the input voltage, the input current, and the battery voltage. In case of an input over-voltage condition, the device immediately removes power from the charging circuit by turning off an internal switch. In the case of an over-current condition, it limits the system current to a safe value for a blanking duration before turning the switch off. Battery voltage may also be monitored and if the battery voltage exceeds the specified value the internal switch is turned off. Additionally, the device also monitors its own die temperature and switches off if it becomes too hot.

The input over-current threshold can be increased using an external resistor. The device also offers protection against reverse voltage at the input.

The ET20125 is available in DFN8L(3.0mm × 3.0mm) package.

Features

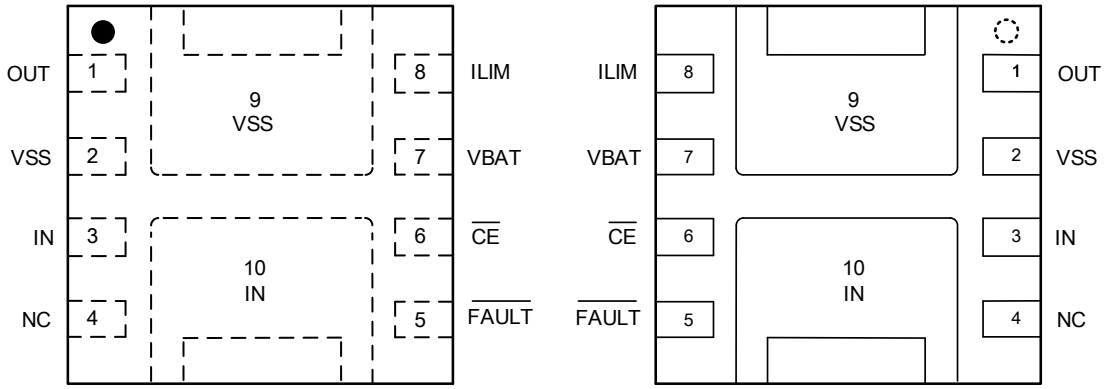
- Provides Protection for Three Variables
  -- Input Over-Voltage
  -- Input Over-Current with Current Limiting
  -- Battery Over-Voltage
- Maximum Input Voltage of 30V
- Supports 0.3A ~ 2A Current Limit
- Soft-Start and Soft-Stop Function
- Thermal Shutdown
- LDO Mode Voltage Regulation of 5.1V
- Fault Status Indication
- ESD Protected: Human Body Model: ESDA/JEDEC JS-001-2024
- Device and Package Information

Part No.	Package	Packing Option	MSL
ET20125	DFN8L (3mm × 3mm)	Tape and Reel, 3K/Reel	3

Application

- Mobile and Smart Phones
- PDAs
- Low-Power Handheld Devices
- Bluetooth™ Headsets

Pin Configuration



TOP VIEW BOTTOM VIEW

DFN8L (3mm × 3mm)

Figure 1. Pin Configuration

Pin Function

Pin	Name	Description
1	OUT	Output Terminal to the Charging System. Connect a ceramic capacitor (1μF Typ) between OUT and GND.
2, 9	VSS	Ground Pin.
3, 10	IN	Power Input Pin. Connect a ceramic capacitor (1μF Typ) between IN and GND.
4	NC	Do not connect to any external circuit. This pin may have internal connections used for test purposes.
5	$\overline{\text{FAULT}}$	Open-Drain Device Status Output Pin. It is recommended to VOUT reaches 90% before checking the $\overline{\text{FAULT}}$ signal.
6	$\overline{\text{CE}}$	Active-Low Chip Enable Input Pin.
7	VBAT	Battery Voltage Sense Input Pin. Connect a 10kΩ resistor to pack positive terminal.
8	ILIM	Overload Current Protection Programming Pin. Connect a resistor to VSS to set the overload current protection threshold: $I_{LIM}(A)=1000/R_{LIM}(\Omega)$.

Block Diagram

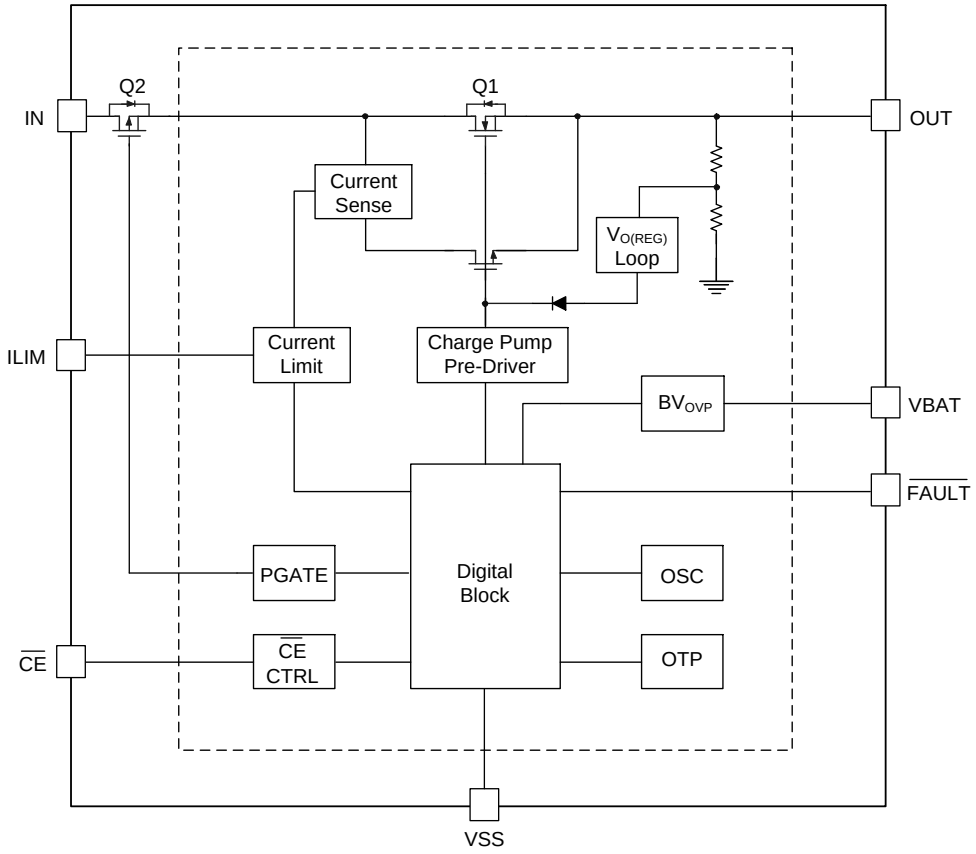


Figure 2. Block Diagram

Functional Description

The ET20125 device is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The device continuously monitors the input voltage, the input current, and the battery voltage. In case of an input over-voltage condition, the device immediately removes power from the charging circuit by turning off an internal switch. In the case of an over-current condition, it limits the current to a safe value for a blanking duration before turning the switch off. It can be approximated with equation below. Additionally, the device also monitors its own die temperature and switches off if it becomes too hot.

The input and over-current threshold is user-programmable. The device can be controlled by a processor using the $\overline{CE}$ pin.

Input Over-Voltage Protection

The ET20125 device integrates an input over-voltage protection feature to protect downstream devices from faulty input sources. If the input voltage rises above V_{OVP}, the internal N-FET Q1 is turned off, removing power from the circuit. The response is very rapid, with the FET turning off in less than a microsecond. When the input voltage returns below $V_{OVP} – V_{HYS(OVP)}$ (but is still above UVLO), the Q1 is turned on again after a deglitch time of $t_{ON(OVP)}$ to ensure that the input supply has stabilized.

Current Limit

A sense FET is employed to check for over current conditions. When an over current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. ET20125 will limit the current until the overload condition is removed or the device begins to thermal cycle.

When ET20125 is turned on, it can provide a limited current of 0.3A~2A. The current limit can be programmed by an external resistor. It can be approximated with equation (1).

$$I_{LIM}(A) = \frac{1000}{R_{LIM}(\Omega)} \quad (1)$$

If the current limit condition lasts longer than 2ms, the ET20125 will be shutdown and restart after 500ms, the IC enters hiccup mode with 2ms of on time and 500ms of off time.

The ET20125 allows ILIM to be floated during operation. The internal fixed current limit threshold is set at 1.5A. When short ILIM to GND, the normal current limit function is disabled.

Battery Over-Voltage Protection

The battery over-voltage threshold V_{BOVP} is internally set to 4.535V. If the battery voltage exceeds the V_{BOVP} threshold for longer than $t_{DGL(BOVP)}$, the Q1 is turned off. This switch-off is also a soft-stop.

The Q1 is turned ON (soft-start) once the battery voltage drops to V_{BOVP} - $V_{HYS(VBOVP)}$.

Reverse-Blocking

The ET20125 offers protection against input reverse polarity up to -30V. When an input source with correct polarity is connected, the device first turns on due to current flow through the body-diode of the P-FET.

When $\overline{CE}$ is low, the P-FET is opened by pulling down the gate voltage to GND, V_{GS_P}= -V_{IN} (when V_{IN} is higher than 12V, V_{GS_P} will be clamped at -12V, see Figure 3).

In the off state (when $\overline{CE}$ is high), the device also offers protection against reverse voltage, the gate of the P-FET will be pulled up to until V_{GS_P} = 0V, block the pathway from OUT to IN.

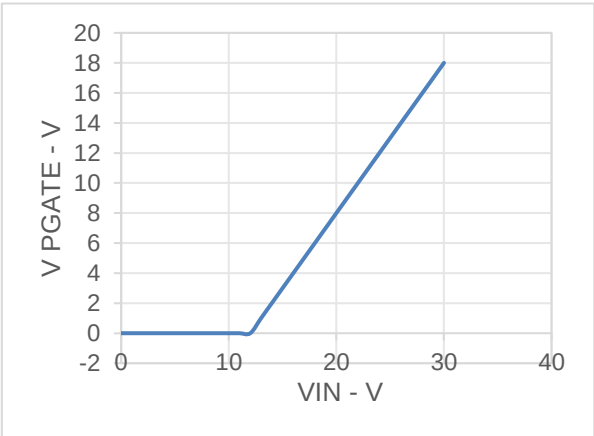


Figure 3. PGATE Voltage vs Input Voltage

Fault

The $\overline{\text{FAULT}}$ pin is open drain output and external pull-up resistor is required. When the Input over-voltage Protection, Current Limit, Battery-OVP, or Thermal protection occurs, $\overline{\text{FAULT}}$ is pulled down to GND. It is returned to high impedance when the above events are removed.

Thermal Protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The ET20125 implements a thermal sensing to monitor the operating junction temperature of the power MOSFET. In an over-current or short-circuit condition, the junction temperature rises due to excessive power dissipation.

Once the die temperature rises to approximately 145°C due to over-current conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. The chip will restart when re-enable or re-power-on.

Absolute Maximum Ratings

Symbol	Parameters		Min	Max	Unit
V_{IN}	IN, PGATE (with respect to VSS)		-30	30	V
V_{OUT}	OUT (with respect to VSS)		-0.3	12	V
V_{ILIM} , V_{CE} , V_{BAT} V_{FAULT}	ILIM, $\overline{\text{CE}}$, VBAT, $\overline{\text{FAULT}}$ (with respect to VSS)		-0.3	7	V
I_{OUT}	Maximum Continuous Current of switch IN-OUT			2.5	A
T_J	Junction Temperature		-40	+150	°C
T_{STG}	Storage Junction Temperature		-65	+150	°C
T_{SOLD}	Soldering Temperature (reflow)			+260	°C
V_{ESD}	Electrostatic Discharge Capability	Human Body Mode, ESDA/JEDEC JS-001-2024	-2.0	+2.0	KV
		Charged Device Mode, ESDA/JEDEC JS -002-2025	-1.5	+1.5	KV

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage Range	3.3	26	V
I_{OUT}	Output current, OUT pin		2	A
I_{LIM}	Limit Current	0.3	2	A
R_{ILIM}	OCP Programming Resistor	0.5	3.33	KΩ
T_A	Operating Temperature Range	-40	+125	°C

P-FET Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$(1)	Drain-to-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	-30			V
$I_{D(Device\ Ref.)}$(1)	Continuous Drain Current	T_A = 25°C			-4.4	A
R_{DSON}(1)	Static Drain-to-Source On-Resistance	V_{GS} = -10V, I_D = -1A		35	48	mΩ
		V_{GS} = -4.5V, I_D = -1A		40	53	mΩ
		V_{GS} = -2.5V, I_D = -1A		61	90	mΩ
$V_{GS(th)}$(1)	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	-0.60	-0.85	-1.3	V
I_{DSS}(1)	Drain-to-Source Leakage Current	V_{DS} = -30V, V_{GS} = 0V,T_A = 25°C			1	μA
I_{GSS}(1)	Gate-to-Source Leakage Current	V_{GS} = ±12V			±100	nA
Ciss(1)	Input Capacitance	V_{GS} = 0V, V_{DS} = -20V,f = 1MHz		570		pF
R_G(1)	Gate Resistance	V_{GS} = 0V, V_{DS} = 0V, f = 1MHZ		7.6		Ω
EAS(1)	Avalanche Energy, Single Pulse	L = 0.5mH， V_{DS} = -24V			9.4	A

Note1: Guaranteed by design.

Electrical Characteristics

Unless otherwise noted, $\overline{CE}$ = Low, T_A=-40°C to 85°C, typical value is tested at T_A=25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{UVLO}	Under-Voltage Lockout, Input Power Detected Threshold	V_{IN} Rising,V_{IN} = 0V to 3V	2.5	2.65	2.8	V
		V_{IN} Falling,V_{IN} = 3V to 0V		2.425		V
$V_{HYS(UVLO)}$	Hysteresis on UVLO	UVLO Hysteresis		225		mV
$t_{DGL(PGOOD)}$	Deglitch Time, Input Power Detected Status	Time measured from V_{IN} = 0V to 5V 1µs rise-time		9		ms
I_{DD}	Operating Current	V_{IN} = 5V, no load on OUT pin		100	200	µA
I_{STDBY}	Standby Current	$\overline{CE}$ = High, V_{IN} = 5.5V		12	20	µA
Input-to-Output Characteristics						
I_{OFF}	Q1 Off-State Leakage Current	$\overline{CE}$ = High, V_{IN} = 5.5V			5	µA
V_{DO}	Dropout Voltage IN to OUT	V_{IN} = 5V, I_{OUT} = 0.5A		75	105	mV
Input Over-Voltage Protection						
$V_{O(REG)}$	Output Voltage	V_{IN} = 5.5V to V_{OVP} - $V_{HYS(OVP)}$, no load on OUT pin	4.9	5.1	5.3	V
V_{OVP}	Input Over-Voltage Protection Threshold	OVP Rising Threshold	6.35	6.8	7.05	V
		OVP Falling Threshold		6.6		V
$V_{HYS(OVP)}$	Hysteresis on OVP	Output OVP Hysteresis	0.05	0.2	0.3	V
$t_{PD(OVP)}$[(1)]	Input Over-Voltage Protection Propagation Delay	V_{IN} = 6V to 9V		200		ns
$t_{REC(OVP)}$	Recovery Time from Input Over-Voltage Condition	Time measured from V_{IN} = 9V to 6V, 1µs fall-time		9		ms
Battery Over-Voltage Protection						
V_{BOVP}	Battery Over-Voltage Protection Threshold	V_{OVP} - $V_{HYS(OVP)}$ > V_{IN} > 4.5V	4.475	4.535	4.61	V
$V_{HYS(VBOVP)}$	Hysteresis on V_{BOVP}	V_{OVP} - $V_{HYS(OVP)}$ > V_{IN} > 4.5V	0.19	0.255	0.32	V
I_{VBAT}	Input Bias Current on VBAT Pin			20	180	nA
$t_{DGL(BOVP)}$	Deglitch Time, Battery Over-Voltage Detected	V_{IN} > 4.5V, time measured from V_{BAT} rising from 4.1V to 5V to $\overline{FAULT}$ going low		180		µs

Electrical Characteristics (Continued)

Unless otherwise noted, $\overline{CE}$ =Low, T_A=-40°C to 85°C, typical value is tested at T_A=25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input Over-Current Protection						
I_{LIM}[2]	Internal Input Over-Current Protection Threshold	V_{IN} = 5V, R_{LIM} floating	1.35	1.5	1.65	A
		V_{IN} = 5V, R_{LIM}=1KΩ	0.9	1	1.1	A
ΔI_{OCP}[1]	OCP Threshold Accuracy	T_A = 0°C to 85°C		±10%		
		T_A = -40°C to 85°C		±13%		
$t_{BLANK(OCP)}$[1]	Blanking Time, Input Over-Current Detected	$\overline{CE}$ = Low		2		ms
$t_{REC(OCP)}$[1]	Recovery Time from Input Over-Current Condition	$\overline{CE}$ = Low		500		ms
Logic Levels on $\overline{CE}$						
V_{IH}	Logic High Input Voltage		1.4			V
V_{IL}	Logic Low Input Voltage				0.4	V
I_{IL}	Input Low Current			0.3	1.5	µA
I_{IH}	Input High Current	$\overline{CE}$ = 1.8V		6	15	µA
Logic Levels on $\overline{FAULT}$						
V_{OL}	Output Low Voltage	I_{SINK} = 5mA		0.14	0.3	V
I_{IKG}	Off-State Leakage Current, HI-Z	V_{FAULT} = 5V		0.01	25	µA
P-FET GATE Driver						
V_{GS_P}[1]	Gate-to-Source Voltage	V_{IN} = 5V, $\overline{CE}$ = Low		-5		V
		V_{IN} > 12V, $\overline{CE}$ = Low		-12		V
		$\overline{CE}$ =High		0		V
Thermal Protection						
T_{SHDN}[1]	Thermal Shutdown			145		°C
T_{HYS}[1]	Thermal Hysteresis			15		°C

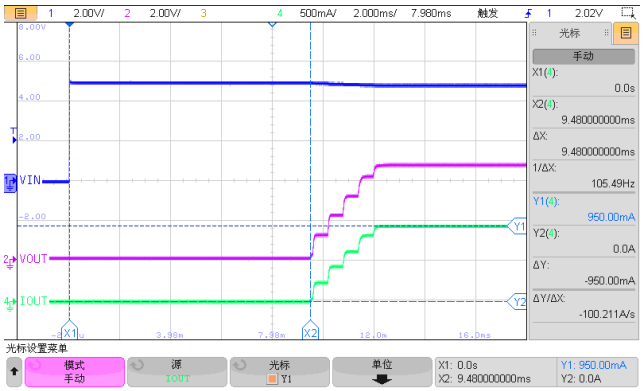
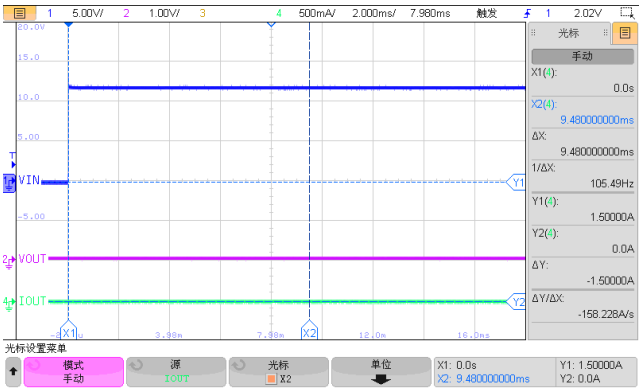
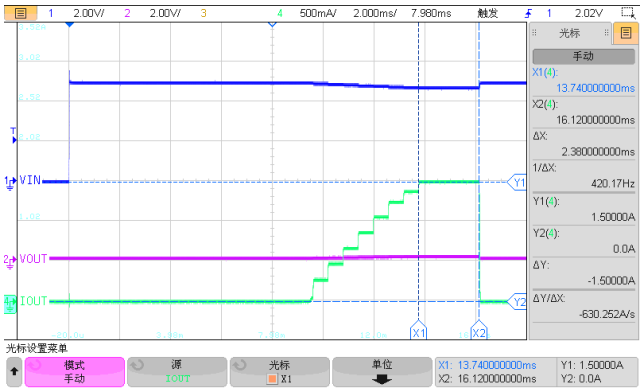
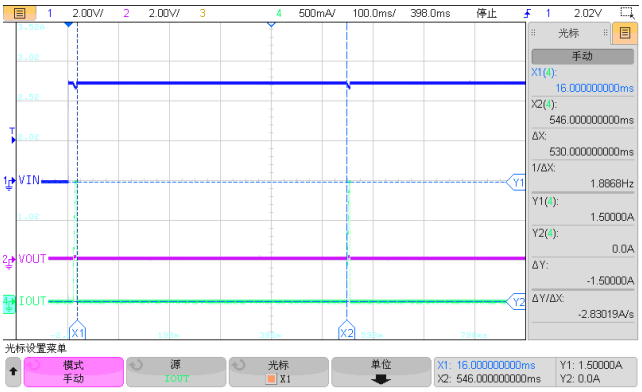
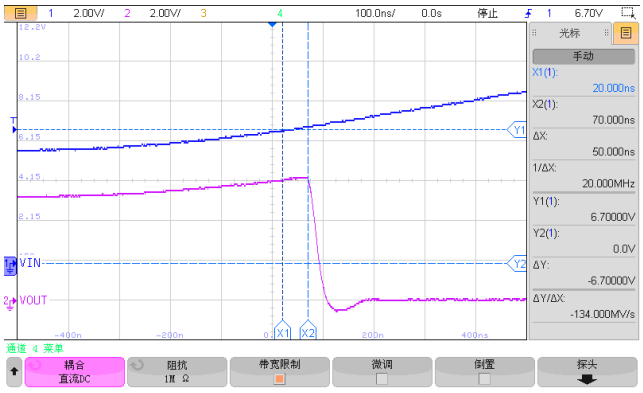
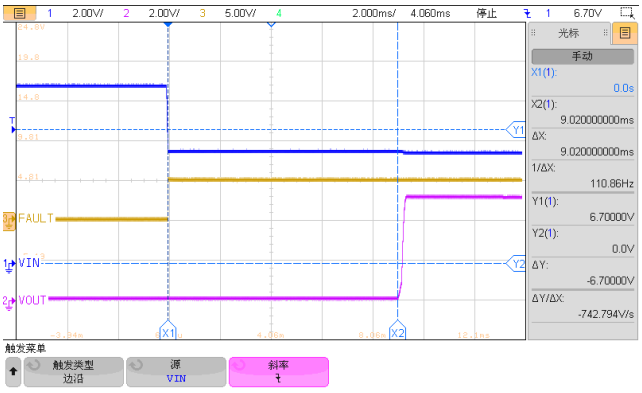
Note1: Guaranteed by design.

Note2: The current limit can be approximated with equation below.

$$I_{LIM}(A) = \frac{1000}{R_{LIM}(\Omega)} \quad (1)$$

Typical Performance Characteristics

Unless otherwise noted, V_{IN} = 5V, $\overline{CE}$ = Low, R_{LIMIT} = Float, C_{OUT} = 1uF, T_A=25°C.

<table>
<tr><td colspan="2">Start-up Test</td></tr>
<tr><td>Start-up through Input voltage (RL = 5Ω)
 
2ms/div</td><td>OVP, Start-up through Input voltage (VIN = 12V)
 
2ms/div</td></tr>
<tr><td>OCP, Start-up through Input voltage (RL = 0Ω)
 
2ms/div</td><td>OCP, Start-up through Input voltage (RL = 0Ω)
 
100ms/div</td></tr>
<tr><td colspan="2">VIN Over-Voltage Protection Test</td></tr>
<tr><td>OVP Response for Input Step
 
100ns/div</td><td>OVP Recovery for Input Step
 
2ms/div</td></tr>
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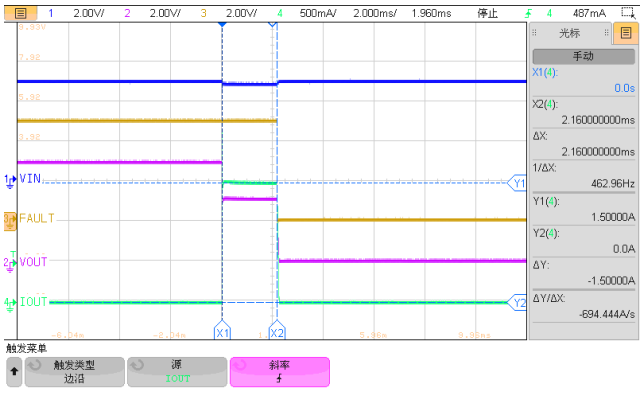
Typical Performance Characteristics

Unless otherwise noted, V_{IN} = 5V, $\overline{CE}$ = Low, R_{LIMIT} = Float, C_{OUT} = 1uF, T_A=25°C.

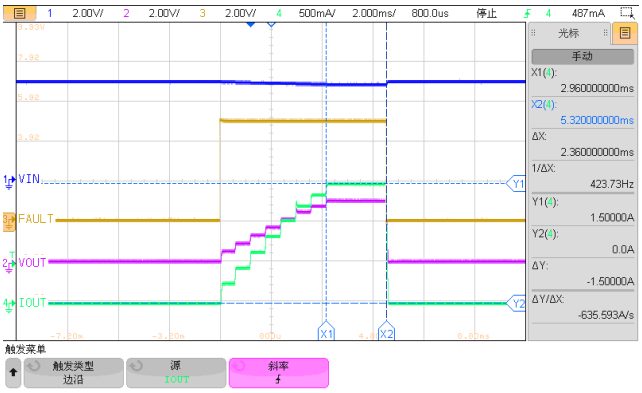
Current Limit Test

Current Limit (RL = 2Ω)



2ms/div

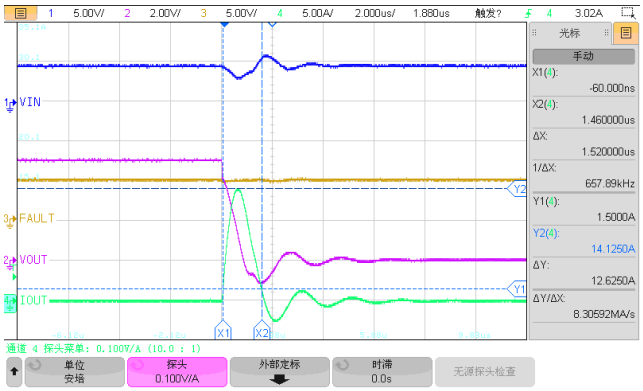
Current Limit (RL = 2Ω)



2ms/div

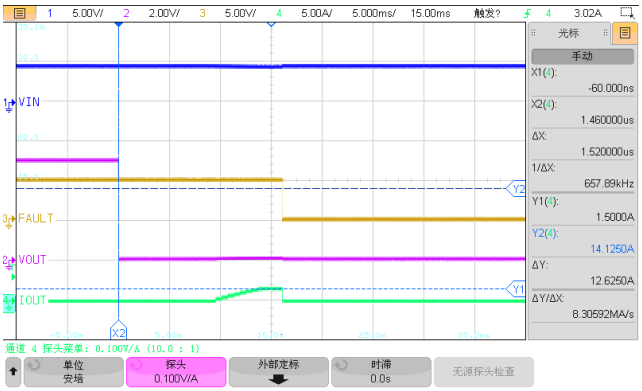
Short Circuit Test

Short Circuit during Normal Operation



2us/div

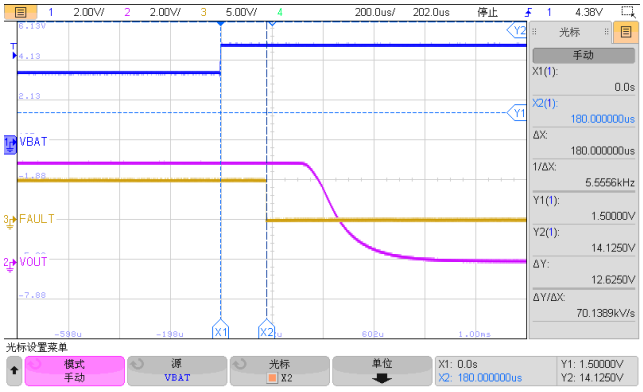
Short Circuit during Normal Operation



5ms/div

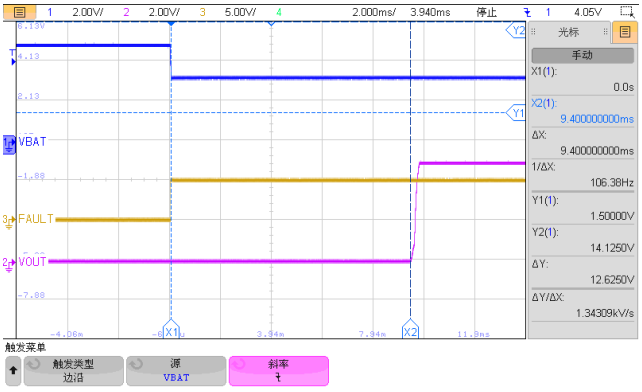
Battery Over-Voltage Protection Test

Battery OVP Response



200us/div

Battery OVP Recovery



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Timing Waveform

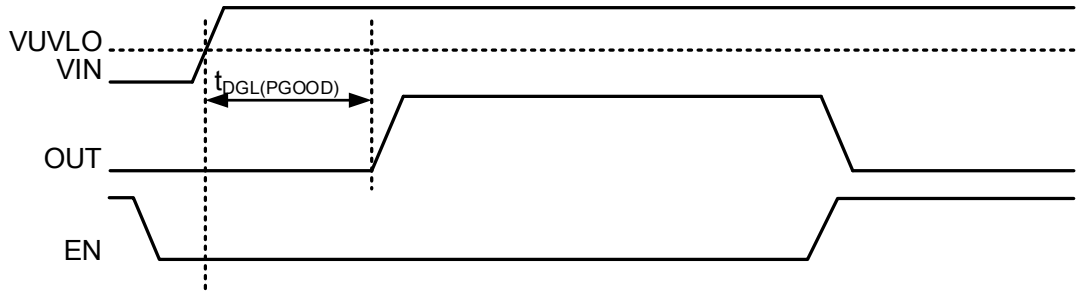


Figure 4. Timing for Power up and Normal Operation

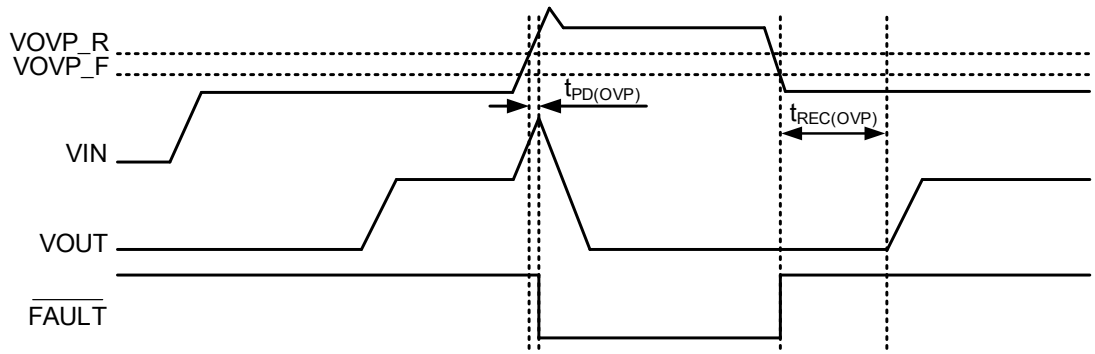


Figure 5. Timing for Input OVP Trip

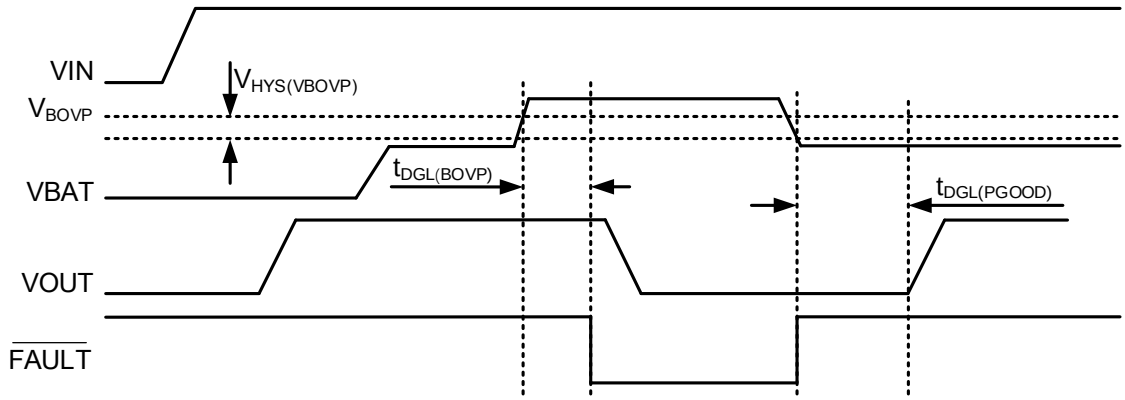


Figure 6. Timing for Battery OVP Trip

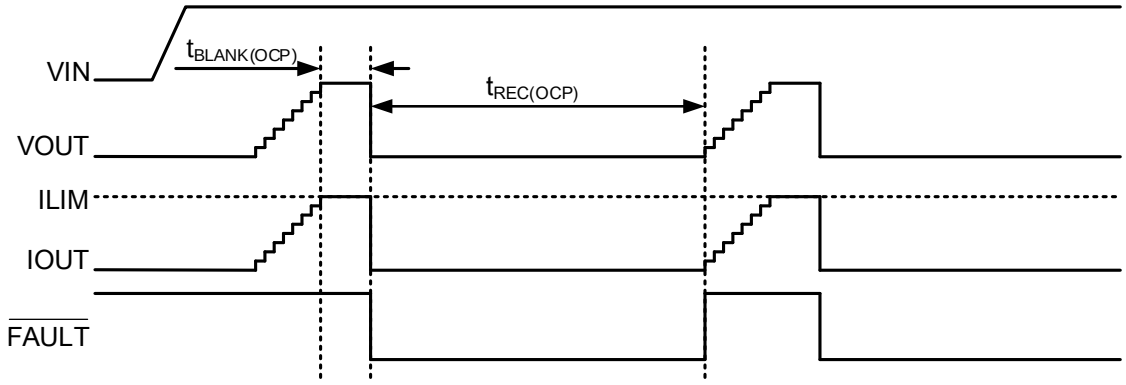
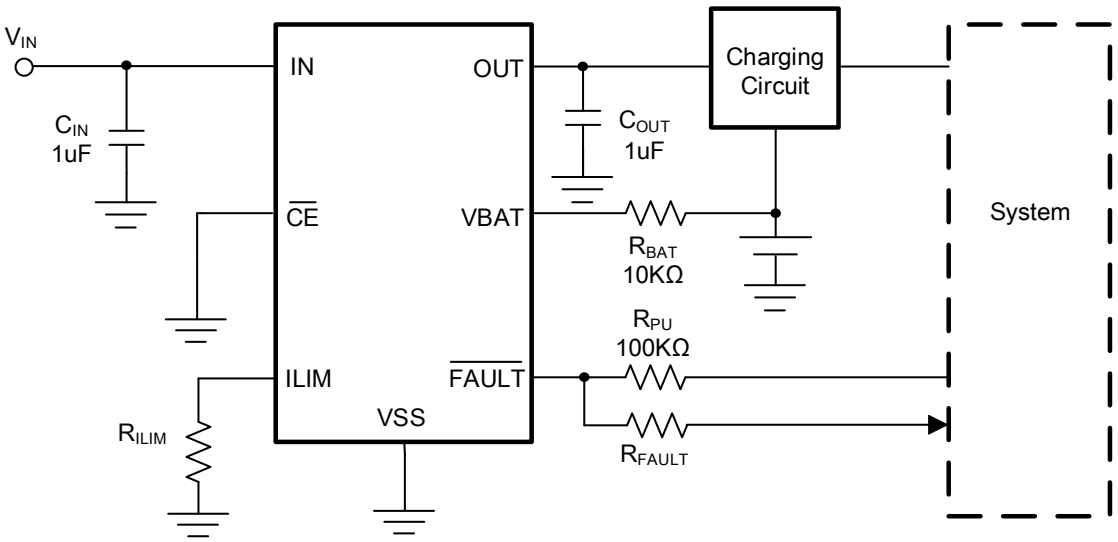


Figure 7. Timing for OCP Trip

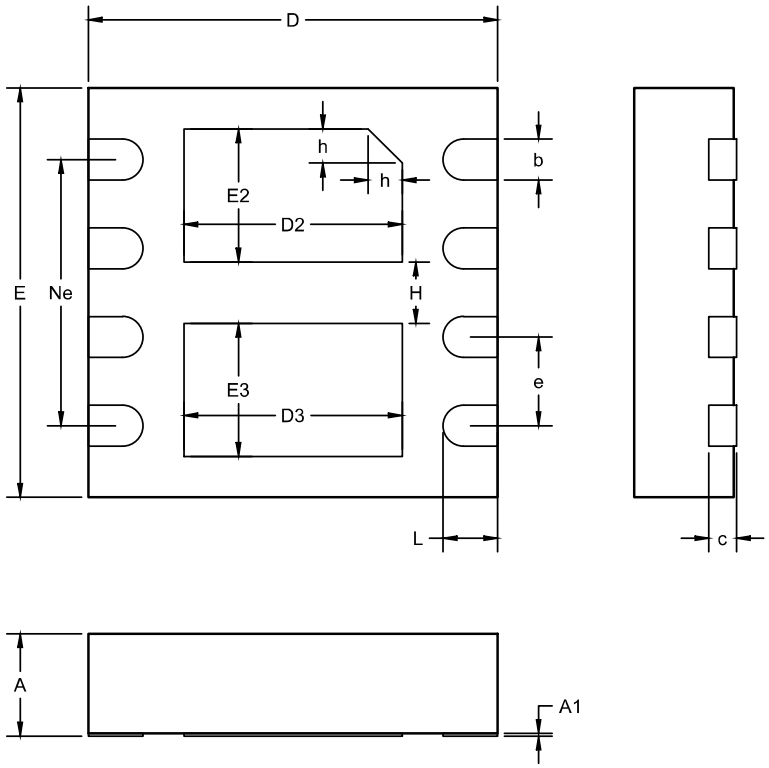
Application Circuits



*:This electric circuit only supplies for reference.

Package Dimension

DFN8L

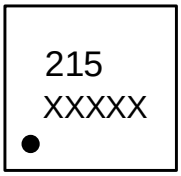


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	-	0.020	0.050
b	0.250	0.300	0.350
c		0.203REF	
D	2.900	3.000	3.100
D2	1.500	1.600	1.700
D3	1.500	1.600	1.700
e		0.650BSC	
Ne		1.950BSC	
E	2.900	3.000	3.100
E2	0.875	0.975	1.075
E3	0.875	0.975	1.075
L	0.350	0.400	0.450
H	0.400	0.450	0.500
h	0.200	0.250	0.300

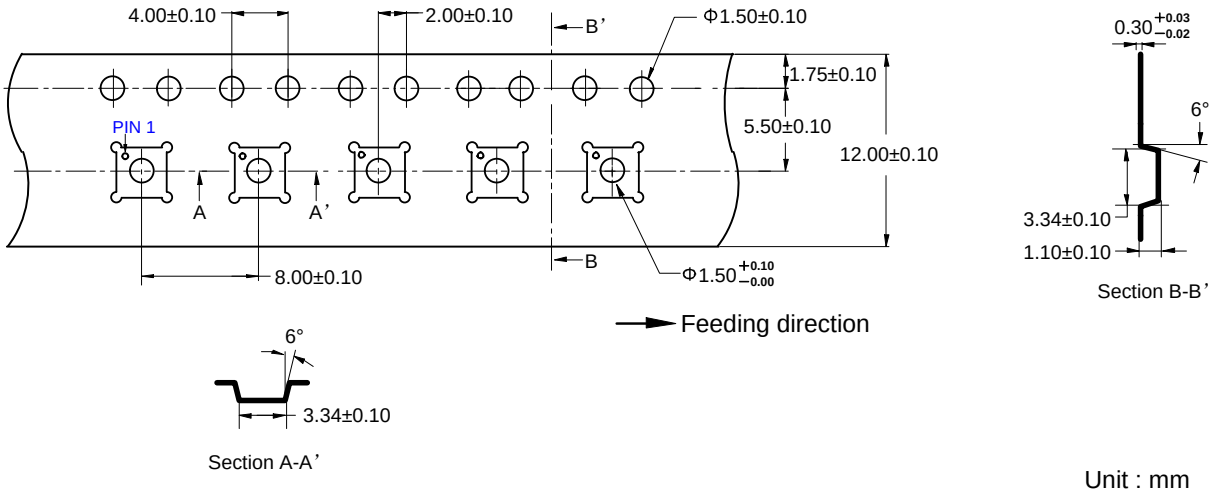
Marking



215 - Part Number

XXXXX - Tracking Number (year and week)

Tape Information



Unit : mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2025-04-21	Preliminary Initial Version	Zoucm	Xuw	Xuw
1.0	2025-10-28	Offical Version	Zoucm	Xuw	Liujy