

High-Voltage High-Current Darlington Transistor Arrays

General Description

The ET2003HV is high-voltage high-current Darlington transistor arrays each containing seven open collector common emitter pairs. Each pair is rated at 500mA. Suppression diodes are included for inductive load driving, the inputs and outputs are pinned in opposition to simplify board layout.

These devices are capable of driving a wide range of loads including solenoids, relays, DC motors, LED displays, filament lamps, thermal print-heads and high-power buffers.

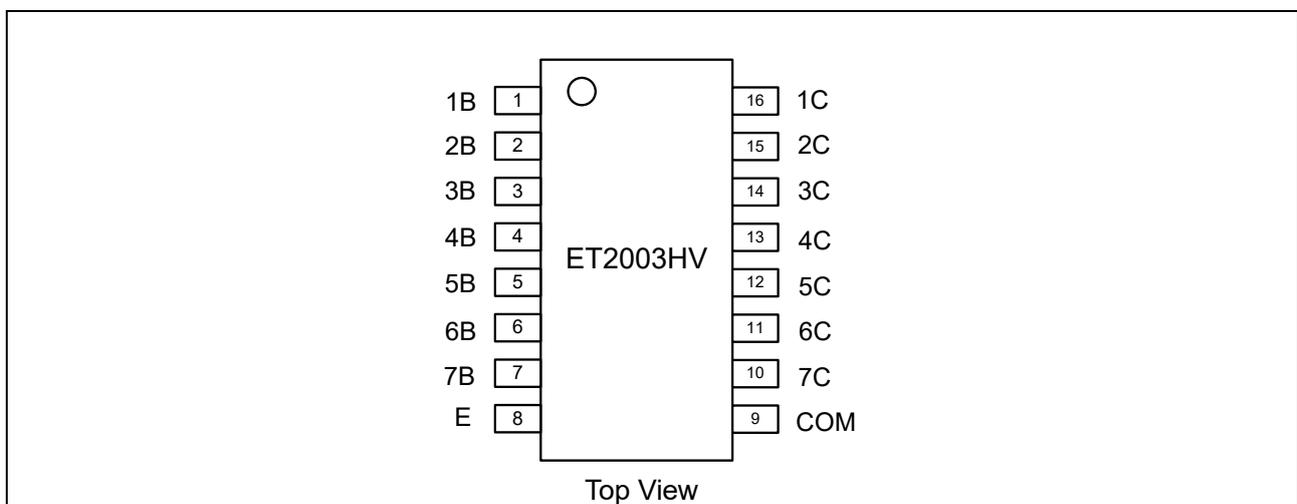
The ET2003HV is offered SOP16 package.

Features

- 500mA Rated Collector Current(single output)
- High-Voltage Outputs: 50V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications
- Part No. and Package

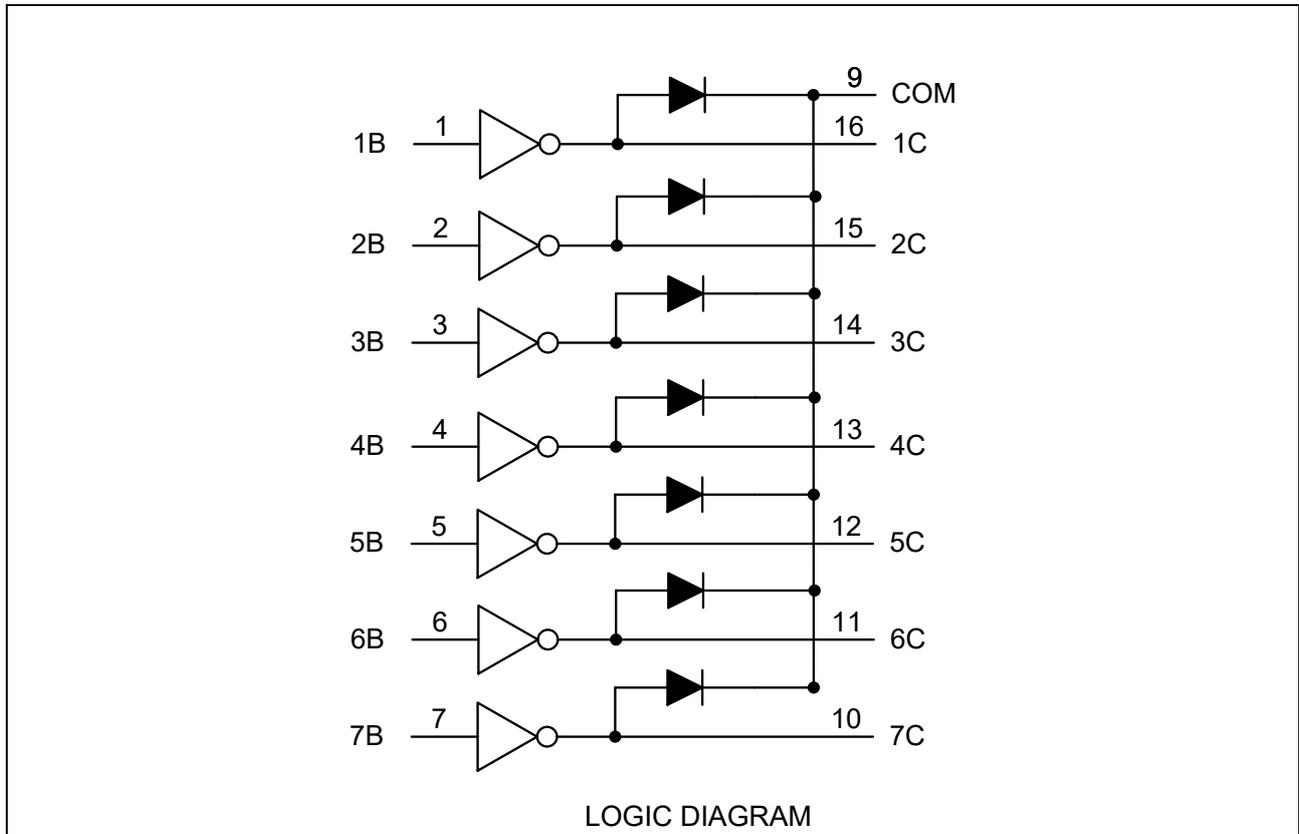
| Part No. | Package |
|----------|---------|
| ET2003HV | SOP16 |

Pin Configuration



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Connection Diagram

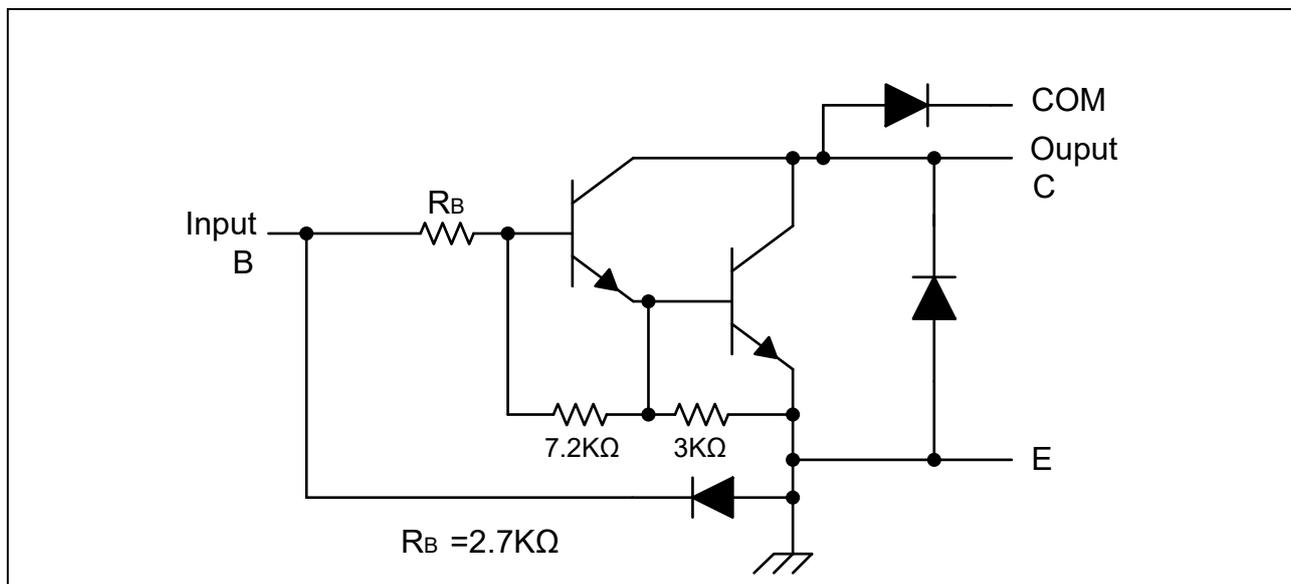


Pin Function

| Pin Name | Pin No. | Description |
|----------|---------|-------------------------|
| 1B | 1 | Input pair1 |
| 2B | 2 | Input pair1 |
| 3B | 3 | Input pair1 |
| 4B | 4 | Input pair1 |
| 5B | 5 | Input pair1 |
| 6B | 6 | Input pair1 |
| 7B | 7 | Input pair1 |
| E | 8 | Common Emitter (ground) |
| COM | 9 | Common Clamp Diodes |
| 7C | 10 | Output pair7 |
| 6C | 11 | Output pair6 |
| 5C | 12 | Output pair5 |
| 4C | 13 | Output pair4 |
| 3C | 14 | Output pair3 |
| 2C | 15 | Output pair2 |
| 1C | 16 | Output pair1 |

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Functional Block Diagram



Note1: All resistor values shown are nominal.

Note2: The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collector(s) go below ground an external Schottky diode should be added to clamp negative undershoots.

Absolute Maximum Ratings⁽³⁾

At 25°C free-air temperature (unless otherwise noted)

| Symbol | Parameters | Min | Max | Unit |
|------------------|---|-----|------|-------|
| V _{CC} | Collector to emitter voltage | -- | 50 | V |
| V _R | Clamp diode reverse voltage | -- | 50 | V |
| V _I | Input voltage | -- | 30 | V |
| I _{CP} | Peak collector current | -- | 500 | mA |
| I _{OK} | Output clamp current | -- | 500 | mA |
| I _{TE} | Total emitter-terminal current | -- | -2.5 | A |
| T _A | Operating free-air temperature range | -40 | 105 | ° C |
| θ _{JA} | Thermal Resistance Junction-to-Ambient ⁽⁴⁾ | -- | 90 | ° C/W |
| θ _{JC} | Thermal Resistance Junction-to-Case ⁽⁵⁾ | -- | 55 | |
| T _J | Operating virtual junction temperature | -40 | +150 | ° C |
| T _{STG} | Storage temperature range | -65 | +150 | ° C |
| ESD | Human Body Mode | 2 | -- | 2KV |

Note3: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note4: Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is PD = (T_{J(max)} - T_A) / θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.

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Note5: Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JC} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $PD = (T_J(\text{max}) - T_A) / \theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

Recommended Operating Conditions

| Symbol | Parameters | Min | Max | Unit |
|----------|-------------------------------|-----|------|------|
| V_{CC} | Collector to Emitter voltage | -- | 50 | V |
| T_A | Operating Ambient Temperature | -40 | +105 | °C |

Electrical Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise specified)

| Symbol | Parameter | Test Figure | Test Conditions | | Min | Typ | Max | Unit |
|----------------------|--------------------------------------|-------------|--|--------------------------|-----|------|------|------|
| $V_{I(\text{on})}$ | On-State Input Voltage | Figure 6 | $V_{CE} = 2V$ | $I_C = 200\text{mA}$ | -- | -- | 2.4 | V |
| | | | | $I_C = 250\text{mA}$ | -- | -- | 2.7 | |
| | | | | $I_C = 300\text{mA}$ | -- | -- | 3.0 | |
| $V_{CE(\text{sat})}$ | Collector-Emitter Saturation Voltage | Figure 5 | $I_I = 250\mu\text{A}$, | $I_C = 100\text{mA}$ | -- | 0.9 | 1.1 | V |
| | | | $I_I = 350\mu\text{A}$, | $I_C = 200\text{mA}$ | -- | 1.0 | 1.3 | V |
| | | | $I_I = 500\mu\text{A}$, | $I_C = 350\text{mA}$ | -- | 1.2 | 1.6 | V |
| I_{CEX} | Collector Cutoff Current | Figure 1 | $V_{CE} = 50V$, | $I_I = 0$ | -- | -- | 50 | uA |
| | | Figure 2 | $V_{CE} = 50V$, $T_A = +105^\circ\text{C}$ | $I_I = 0$ | -- | -- | 100 | |
| V_F | Clamp Forward Voltage | Figure 8 | $I_F = 350\text{mA}$ | | -- | 1.7 | 2 | V |
| $I_{I(\text{off})}$ | Off-State Input Current | Figure 3 | $V_{CE} = 50V, I_C = 500\mu\text{A}$ | | 50 | 65 | -- | uA |
| I_I | Input Current | Figure 4 | $V_I = 3.85V$ | | -- | 0.93 | 1.35 | mA |
| | | | $V_I = 5V$ | | -- | 1.5 | 1.85 | |
| | | | $V_I = 12V$ | | -- | 4.2 | 4.55 | |
| I_R | Clamp Reverse Current | Figure 7 | $V_R = 50V$ | | -- | -- | 50 | uA |
| | | | | $T_A = 70^\circ\text{C}$ | -- | -- | 100 | |
| C_i | Input Capacitance | | $V_I = 0, f = 1\text{MHz}$ | | -- | 15 | 25 | pF |

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Switching Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|-----------|--|--|------------|------|-----|------|
| t_{PLH} | Propagation Delay Time, Low to High Level Output | See Figure 9 | | 0.25 | 1 | us |
| t_{PHL} | Propagation Delay Time, High to Low Level Output | See Figure 9 | | 0.25 | 1 | us |
| V_{OH} | High Level Output Voltage after Switching | $V_S = 50\text{V}$, $I_O = 50\text{mA}$, See Figure 9 | $V_S - 20$ | | | mV |

Parameter Measurement Information

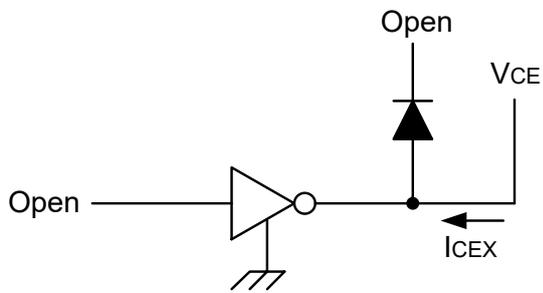


Figure 1. I_{CEX} Test Circuit

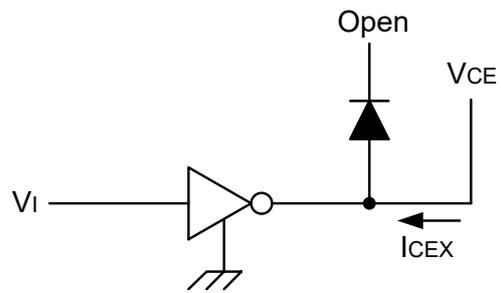


Figure 2. I_{CEX} Test Circuit

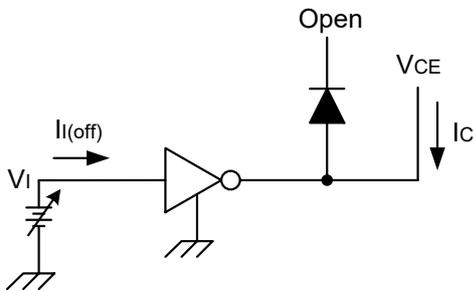


Figure 3. $I_{I(off)}$ Test Circuit

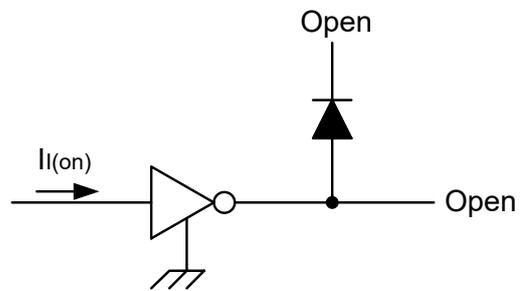


Figure 4. I_I Test Circuit

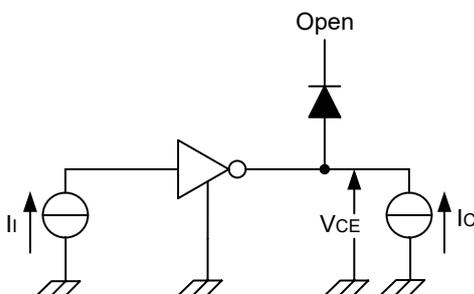


Figure 5. $V_{CE(sat)}$ Test Circuit

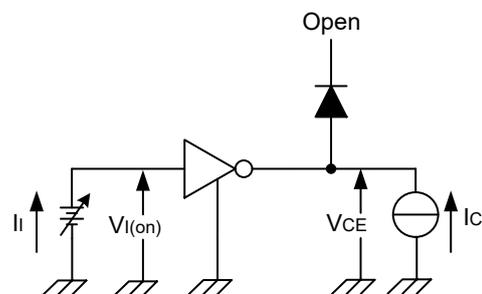


Figure 6. $V_{I(on)}$ Test Circuit

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Parameter Measurement Information (Continued)

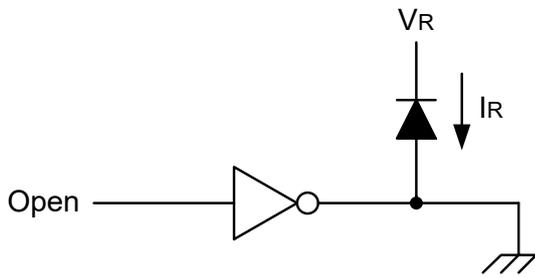


Figure 7. ICEX Test Circuit

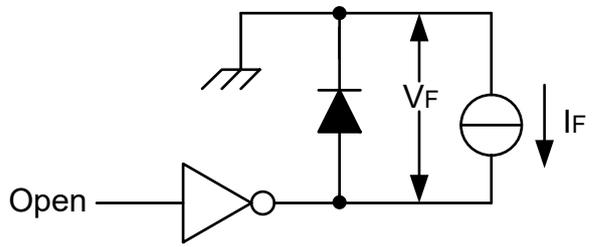
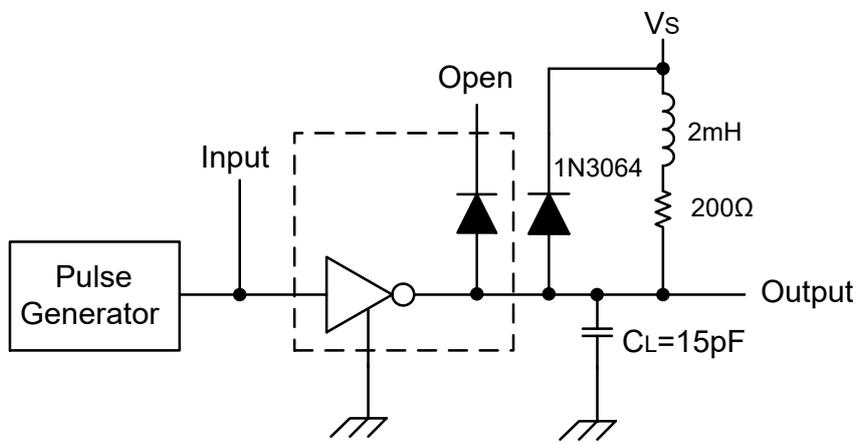
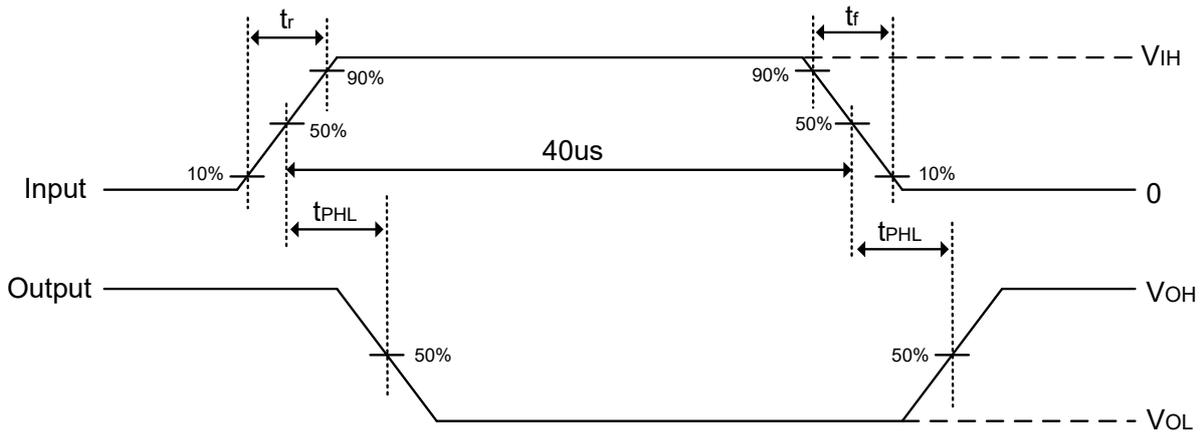


Figure 8. VF Test Circuit



t_{ON} , t_{OFF} , Test Circuit (6)(7)



Voltage Waveform (8)

Figure 9. Latch-Up Test Circuit and Voltage Waveform

Note6: The pulse generator has the following characteristics: Pulse Width=12.5Hz, output impedance 50Ω, $t_r \leq 5ns$, $t_f \leq 10ns$.

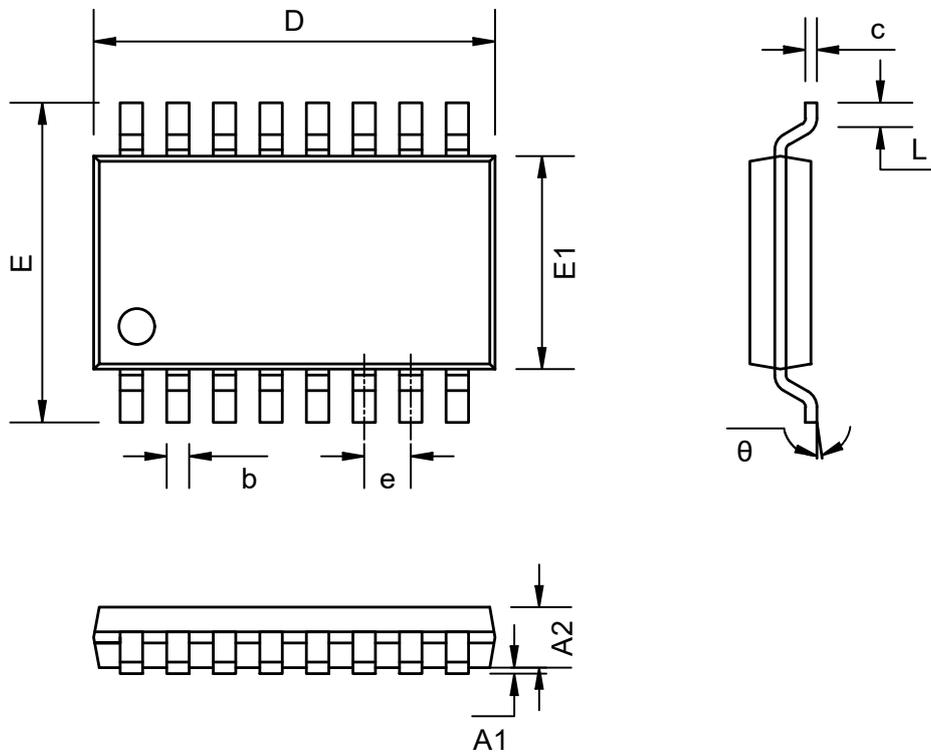
Note7: C_L includes probe and jig capacitance.

Note8: $V_{IH} = 3V$.

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Package Dimension

SOP16



Dimensions Table (Units:mm)

| Symbol | Min | Non | Max |
|--------|---------|-------|-------|
| A1 | 0.10 | 0.20 | 0.30 |
| A2 | 1.35 | 1.45 | 1.55 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.17 | 0.20 | 0.25 |
| D | 9.80 | 10.00 | 10.20 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.27BSC | | |
| L | 0.4 | -- | 1.27 |
| θ | 0° | -- | 8° |

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Revision History and Checking Table

| Version | Date | Revision Item | Modifier | Function & Spec Checking | Package & Tape Checking |
|---------|------------|---------------------|----------|--------------------------|-------------------------|
| 0.0 | 2025-03-19 | Preliminary Version | Liu j | Liu j | Liu j y |
| 1.0 | 2025-08-15 | Initial Version | Cao j c | Wu h s | Liu j y |
| | | | | | |