I²C Controlled Dual Phase Switched Capacitor Charger

General Description

The ET95967 is a high efficiency switched capacitor converter used for fast charging. It can deliver up to 8A output current to charge the battery with single cell in series. It integrates one reverse blocking FET and two phases of switched capacitor converter. Each phase is enabled with 50% duty cycle to allow the cable current to be half of the charging current into the battery. The two phases operate with interleave mode which can optimize the output voltage ripple.

The ET95967 is available in WLCSP36 (2.773mm × 2.773 mm) package.

Features

- Up to 40V Sustainable Voltage with AC Sense Pin and N-Channel MOSFET Driver
- Fast Response Timer (<200ns) of AC Over-voltage Protection to Turn Off the External MOSFET
- VBAT, IBAT Regulation via External OVP FET
- Integrated the Reverse Blocking FET and Input Current Sense Resister
- Integrated Dual Phase Switched Capacitor Converter with Low Ron
- 200kHz to 1200kHz Frequency with Dithering

Multiple System Protections

- VBUS Over-voltage Protection
- VOUT Over-voltage Protection
- VBAT Over-voltage Protection
- IBUS Over-current Protection
- IBUS Under-current Protection
- IBAT Over-current Protection
- TDIE Over-temperature Protection
- Multiple Switched Capacitor Converter Protection
   -- VBUS High Voltage Protection before Switching
   -- VBUS Low Voltage Protection before Switching
   -- Fly Capacitor Short and Open Detection before Switching
   -- Power FET Over-current Protection during Switching
   -- VBUS Short-circuit Protection
   -- Reverse Current Protection
- FLAG and MASK Options for Interrupt
- Integrated 12-bit Effective ADC for 5 Channels

▪ VBUS Voltage	▪ VBAT Voltage
▪ IBUS Current	▪ IBAT Current
▪ Junction Temperature	

ET95967

Device Information

Part No.	Package	MSL
ET95967	WLCSP36 (2.773mm×1.55mm,0.35mm pitch)	1

Applications

- Smart-phone
- Tablet PC

Pin Configuration

● VAC A1	VBUS A2	VBUS A3	VBUS A4	VBUS A5	GATE A6
BST1 B1	PMID B2	DP B3	DM B4	PMID B5	BST2 B6
CFH1 C1	CFH1 C2	SDA C3	SCL C4	CFH2 C5	CFH2 C6
VOUT D1	VOUT D2	BATN/SRP D3	SRN D4	VOUT D5	VOUT D6
CFL1 E1	CFL1 E2	BATP E3	/INT E4	CFL2 E5	CFL2 E6
GND F1	GND F2	AGND F3	REGN F4	GND F5	GND F6
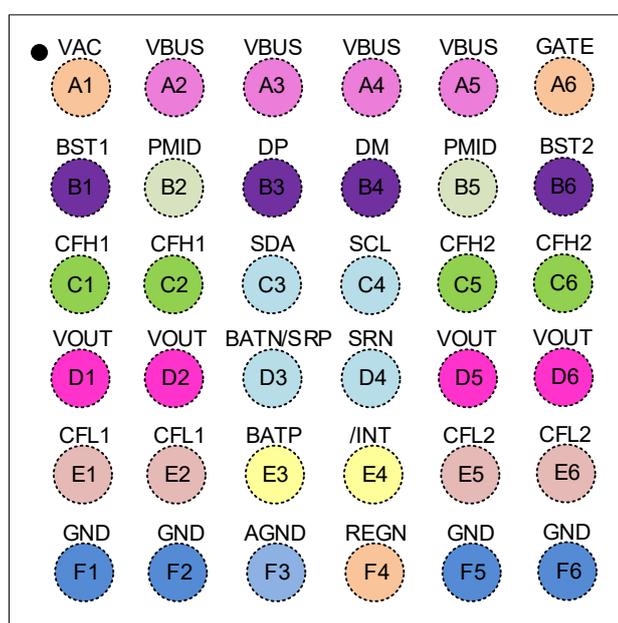
TOP View (Bumps Down) WLCSP36

Pin Function

| Pin No.	Pin Name	Pin Function
A1	VAC	Device power input. Connect 10µF/35V capacitor to VAC.
A2, A3, A4, A5	VBUS	Device power input. Place a 1µF/25V bypass capacitor to GND as close as possible to these pins.
A6	GATE	External OVP FET N-channel gate drive pin. Float if not in use.
B1	BST1	Boot-strap voltage for gate drive. Place a 100nF/16V between BST1 and CFH1.
B2, B5	PMID	Input terminal of the switched capacitor power stage. Connect 10µF/16V capacitor to PMID.
B3	DP	USB data line differential pair.
B4	DM	USB data line differential pair.

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Pin Function(Continued)

B6	BST2	Boot-strap voltage for gate drive. Place a 100nF/16V between BST2 and CFH2
C1, C2	CFH1	Positive input of the flying capacitor CFLY1. Connect 2 x 22µF/10V capacitor in parallel between CFH1 and CFL1.
C3	SDA	I²C data line. Pull up to system I/O voltage via 1k resistor.
C4	SCL	I²C clock line. Pull up to system I/O voltage via 1k resistor.
C5, C6	CFH2	Positive input of the flying capacitor CFLY2. Connect 2 x 22µF/10V capacitor in parallel between CFH2 and CFL2.
D1, D2, D5, D6	VOUT	Power output. Place a 10µF/10V decoupling capacitor to GND.
D3	BATN_SRP	Negative input for battery voltage sensing and positive input for low-side battery current sensing. Place 100Ω series resistance between pin and negative signal.
D4	SRN	Negative input for low-side battery current sensing. Place a 2mΩ or 5mΩ RSENSE between SRN and SRP. Short BATN_SRP and SRN together and to GND if not used.
E1, E2	CFL1	Negative input of the flying capacitor CFLY1. Connect 2 x 22µF/10V capacitor in parallel between CFH1 and CFL1.
E3	BATP	Positive input for battery voltage sensing. Connect to positive terminal of battery pack. Place a 100Ω series resistance between pin and positive signal.
E4	/INT	Open-drain Output. Active low interrupt output. Pull up to voltage supply with 10kΩ resistor
E5, E6	CFL2	Negative input of the flying capacitor CFLY2. Connect 2 x 22µF/10V capacitor in parallel between CFH2 and CFL2.
F1, F2, F5, F6	GND	Power Ground.
F3	AGND	Analog ground. Connect to GND through single point on PCB.
F4	REGN	LDO output. Connect a 4.7µF/10V cap between this pin and GND.

Block Diagram
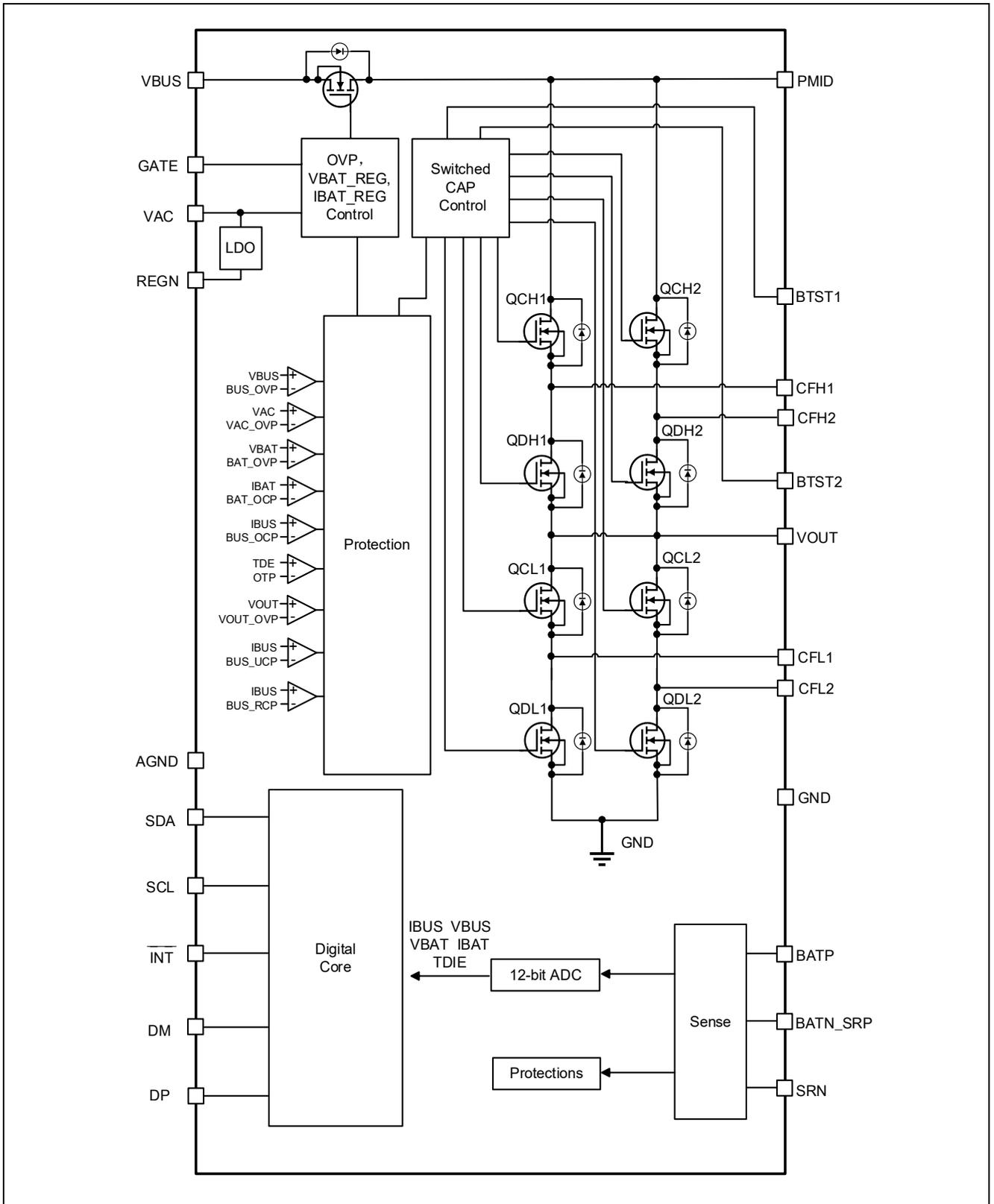
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Functional Description

Charging System

The ET95967 is a single-cell high efficiency switched capacitor charger, used in parallel with a switching mode charger to achieve fast charging in constant current charge stage. A host must set up the desired protection thresholds prior to enabling the ET95967. The ET95967 is able to support the direct charging to the battery by configure the operation mode to bypass mode.
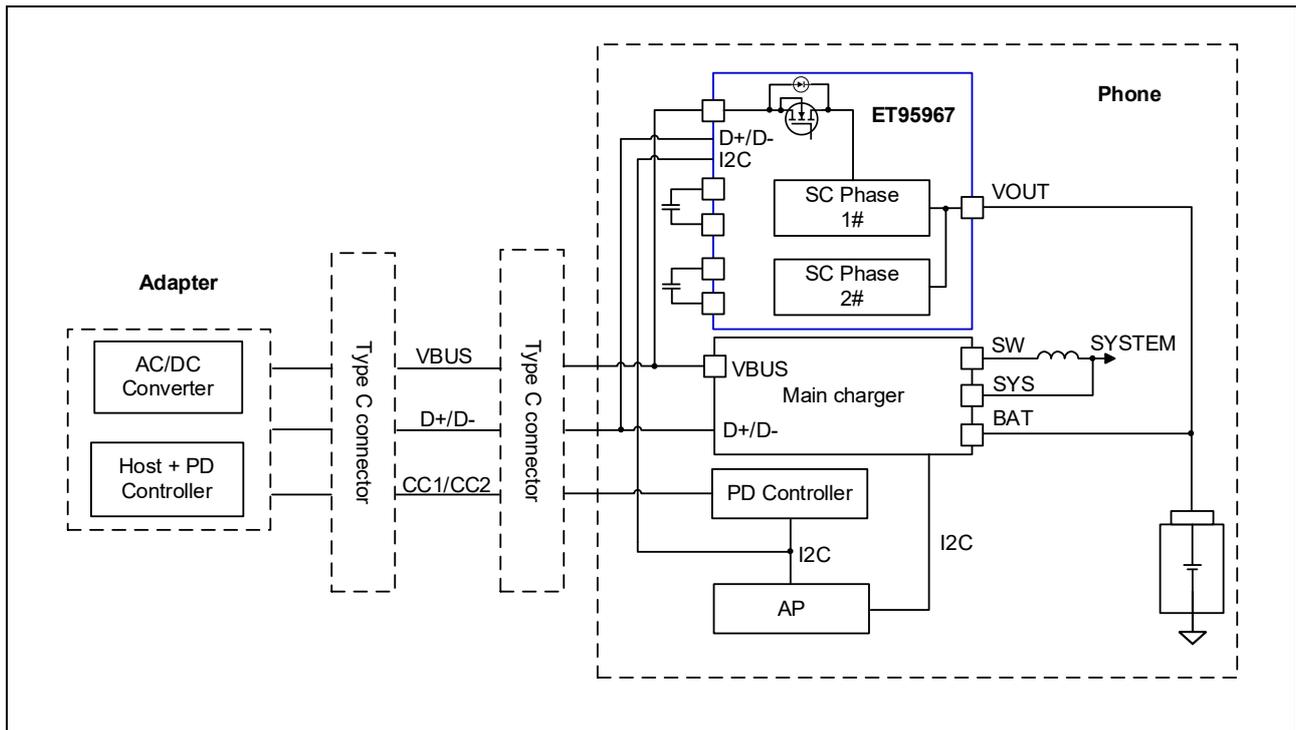

Figure 1.   Charging System of the Direct Charging

Battery Charging Profile

The system will have a specific and unique battery charging profile due to the switched capacitor architecture. The charging will be controlled by the main charger until the system voltage reaches minimum system regulation voltage (VSYS_REG_MIN). Once the battery voltage reaches VSYS_REG_MIN, the adapter can negotiate for a higher bus voltage and enable ET95967 by regulating the current on VBUS to charge the battery. In the constant current charge phase, the protection in ET95967 will not regulate the battery voltage, but will provide feedback to the system to increase and decrease current as needed, as well as disable the blocking and switching FETs if the voltage is exceeded. Once the constant voltage point is reached, the ET95967 will provide feedback to the adapter to reduce the current, effectively tapering the current until a point where the main charger takes over again.
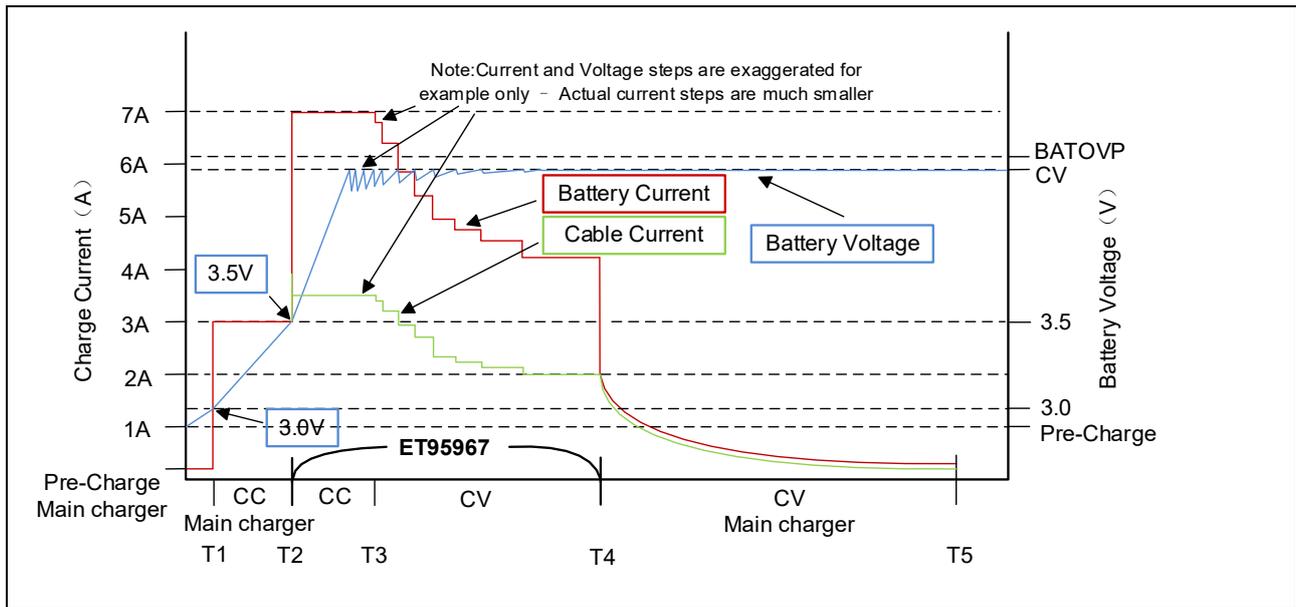
Figure 2. System Charging Profile

Device Power Up

The device is powered from the higher of VAC, VBUS or VOUT (Battery). The voltage must be greater than the VAC_UVLO, VBUS_UVLO or VOUT_UVLO threshold to be a valid supply. Once VAC rises above VAC_UVLO or VBUS rises above VBUS_UVLO or VOUT rises above VOUT_UVLO, I²C interface is ready for communication and all the registers are reset to default value. But the host needs to wait VBUS_PRES_FLAG and VBAT_PRES_FLAG go high before charging.

The device will not charge when first powered up, as the default charge state is always not enabled. The ADC is available prior to enabling charge so the system parameters are known to the host before enabling charge. If the VOUT voltage is not greater than 3V, the charge can not be enabled. The lowest charge voltage allowed on VOUT is 2.8V falling. When VAC is not present the charge can not be enabled.

Operation Mode

There are two operation modes in the ET95967. One is switched cap mode (2:1 mode), the other is bypass mode (1:1 mode).

Switched Capacitor Operation

The power stage used in the ET95967 is a parallel-series switched cap architecture with two phases. The output voltage of the power stage is half of the input voltage. The output current of the power stage is twice the input current. By controlling the constant current source input to the power stage, the CC and CV charging phases can be achieved.
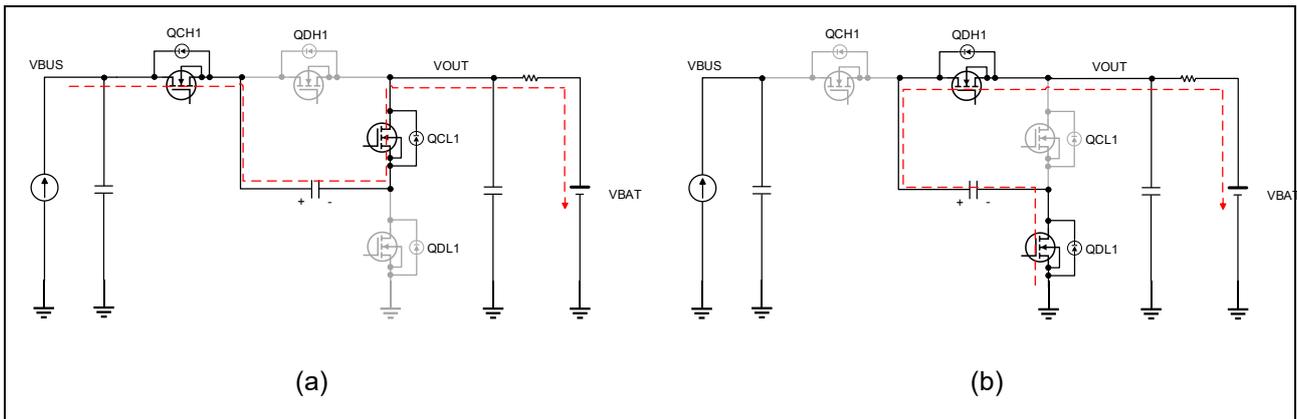
Figure 3.   Operation Principle of the Switched Capacitor

The power stage of the device is shown in the block diagram, and a simplified single phase circuit is shown in Figure 3. When operating, the device switches at a 50% duty cycle with QCH1 and QCL1 turned on and off at the same time, while QDH1 and QDL1 are turned on and off simultaneously.

Bypass Mode

When host determines the adapter support bypass mode charging, the device can enable Bypass Mode. Blocking FET (QB) and switching FET (QCH1, QDH1, QCH2, QDH2, QDL1, QDL2) are turned on to charge from adapter to battery. During Bypass Mode, when fault occurs, switching stopped and Bypass Mode is reset.
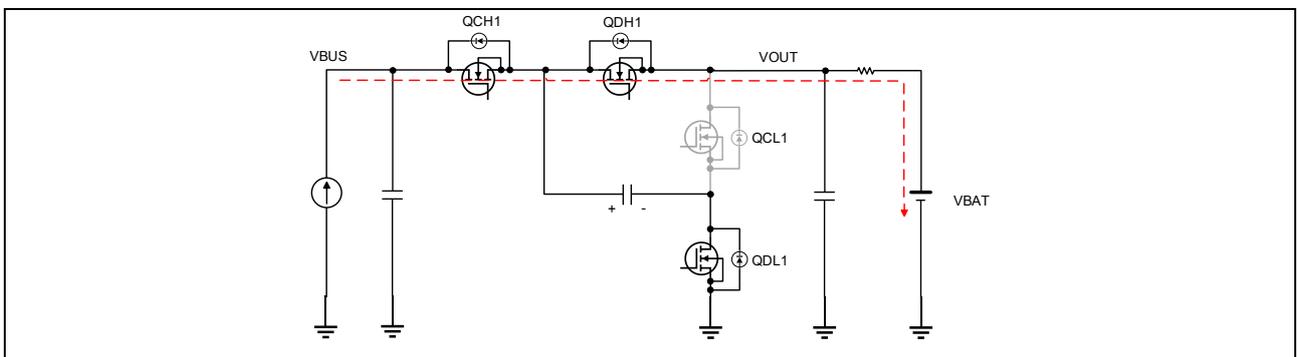
Figure 4.   Operation Principle of Bypass Mode

To change from Bypass Mode to Switched Cap Mode or from Switched Cap to Bypass Mode, the host would first set off mode to stop the converter. The host sets applicable adapter voltage and desired protection threshold before choosing operation mode

Charge Condition Qualification

Prior to enabling charging, set all the protections to the desired thresholds. Protections available are BAT_OVP, BAT_OCP, AC_PROTECTION, BUS_OVP, BUS_OCP_UCP. The *_OVP and *_OCP registers set the thresholds where if these conditions are met, the charger stops switching.

VBUS In-range Check

Before switching starts, the BUS voltage must be between VBUS_ERR_LO and VBUS_ERR_HI for the part to start switching. Register 0x02h, bit [5:0] is used to enable the qualification and configure the threshold. Register 0x0Dh contains the registers to check if these conditions have been met.

Bit	Name (0X02H)	Default	Type	Description
5	VBUS_ERR_LOW_EN	1	R/W	VBUS low voltage check enable. 0: Disable, 1: Enable.
4	VBUS_ERR_HIGH_EN	1	R/W	VBUS high voltage check enable. 0: Disable, 1: Enable.
3	VBUS_ERR_LOW_REF [1]	1	R/W	VBUS low voltage check threshold.
2	VBUS_ERR_LOW_REF [0]	1		00: 1.01, 01: 1.02, 10: 1.03, 11: 1.04.
1	VBUS_ERR_HI_REF [1]	0	R/W	VBUS high voltage check threshold.
0	VBUS_ERR_HI_REF [0]	0		00: 1.1, 01: 1.15, 10: 1.2, 11: 1.25.

- In switched cap mode, VBUS_ERR_HI threshold is VBUS/VOUT > 2 x REG02h bits [1:0], while VBUS_ERR_LO threshold VBUS/VOUT < 2 x REG02h bits [3:2]. A 100mV hysteresis is required for VBUS_ERR_HI fault recovery

- In bypass mode, VBUS_ERR_HI threshold is VBUS/VOUT > 1 x REG02h bits [1:0], while VBUS_ERR_LO threshold VBUS/VOUT < 1 x REG02h bits [3:2]. A 100mV hysteresis is required for VBUS_ERR_LO fault recovery.

When VBUS in-range is enabled, before switching start if the VBUS/VOUT > VBUS_ERR_HI threshold, the both switched cap and bypass mode can't be enabled. If the VBUS/VOUT < VBUS_ERR_LO threshold, the Switched Cap or Bypass Mode can be changed but the switching will not start until the VBUS exceeds VBUS_ERR_LO.

If REGECh bit [7] is 1, the VBUS in-range will be always active after switching. After switching start, if VBUS/VOUT >VBUS_ERR_HI threshold for 17µs, the switching will be suspended and Switched Cap or Bypass Mode reset, while VBUS/VOUT <VBUS_ERR_LO for 17µs the Switched Cap or Bypass Mode will not be reset but switching will be suspended.

Bit	Name (0XECH)	Default	Type	Description
7	VBUS_ERR_OPT	0	R/W	This bit set whether VBUS_ERR check still works after switching starts. 0: VBUS_ERR will be disabled after switching starts. (Only works before switching starts); 1: VBUS_ERR will be always active.

When VBUS_ERR_HI or VBUS_ERR_LO fault is triggered, the responding flag bit will be set. It can be cleared after the bit is read.

Bit	Name (0X0DH)	Default	Type	Description
2	VBUS_ERR_LOW_FLAG	0	RC	VBUS low voltage error flag. Will be set to 1 when the fault has happened. Will be reset to 0 after host read this bit.
1	VBUS_ERR_HIGH_FLAG	0	RC	VBUS high voltage error flag. Will be set to 1 when the fault has happened. Will be reset to 0 after host read this bit

The VBUS In-range check can be disabled by REG02h bit [5] and bit [4].

When VBUS in-range check is disabled, VBUS in-range will not be checked either before or after switching.

That means before switching the Switched Cap or Bypass Mode can be configured always and switching will start if no other fault happens, and after switching the switching will not be suspended when the VBUS/VOUT is out of VBUS in-range.

As details the relative VBUS Low Voltage and High Voltage behavior is as below:

Fault	Cases	Enabled VBUS_ERR_OPT =1	Disabled VBUS_ERR_OPT=0/1	Enabled VBUS_ERR_OPT =0
VBUS_ERR_LOW	Before Switching	Charge mode can be configured, but switching is suspended.	Charge mode can be configured, switching will NOT be suspended.	Switching will NOT be stopped. Charge mode will NOT be reset
	After Switching	Switching is stopped, Charge mode will NOT be reset	Switching will NOT be stopped. Charge mode will NOT be reset	Switching will NOT be stopped. Charge mode will NOT be reset.
VBUS_ERR_HIGH	Before Switching	Charge mode can NOT be configured, switching is suspended.	Charge mode can be configured, switching will NOT be suspended	Charge mode can NOT be configured, switching is suspended.
	After Switching	Switching is stopped, Charge mode will be reset to 0	Switching will NOT be stopped. Charge mode will NOT be reset.	Switching will NOT be stopped. Charge mode will NOT be reset.

The host can start charging following below steps

- Both VBUS and VOUT needs to be present.
- Host set all protection thresholds.
- Host set applicable VBUS
- Host set the switching frequency if selecting SC mode.
- Host set the IBUS_UCP Rising Threshold
- Host select switched cap mode or bypass mode to enable charge.

External OVP FET Control

VAC Over-voltage Protection

The ET95967 has a high voltage sense pin VAC to monitor the adapter voltage. When VAC voltage exceeds the present threshold, the integrated OVPFET driver will turn on the external N-channel OVPFET after 20ms immunity time if VAC voltage is lower than VAC OVP threshold. When VAC voltage exceeds the VAC OVP threshold, the OVPEFT needs to be turned off within 200ns. When VAC voltage decreases lower than VAC OVP threshold, the OVPFET will be turned on again after 20ms deglitch time.

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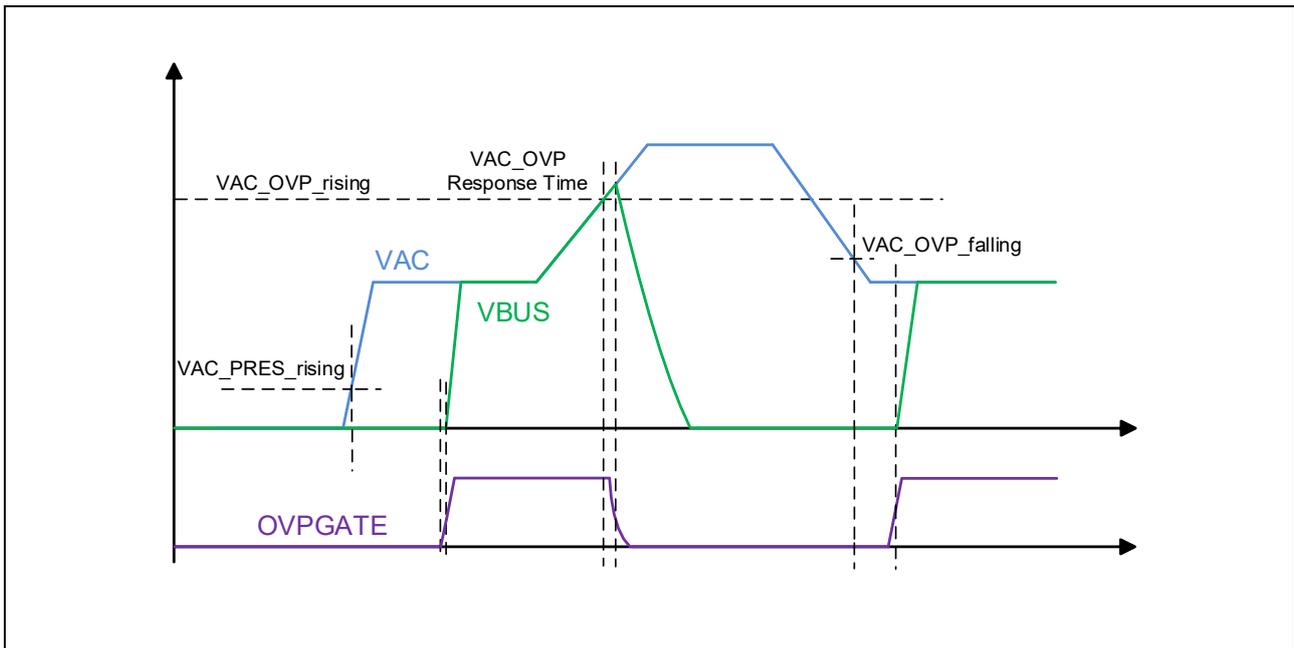
Figure 5.   OVPGATE Timing

The VAC OVP block can be disabled via REG04h, bit [5]. When this block is disabled, the OVPGATE output is HIZ state. The VAC OVP block is enabled as default, the OVPGATE driver outputs 5V versus VBUS to drive the external OVPFET.

Another bit REG04h, bit [4] is designed to disable the OVP protection which means the OVPFET will be always on no matter what the VAC voltage is. While the OVP protection is enabled, the OVP threshold can be configured via REG04h, bits [3:0]. When the VAC OVP has occurred, the FLAG bit of REG0Bh, bit [7] is set. The bit will be cleared once it's read.

Bit	Name (0X04H)	Default	Type	Description
5	VAC_OVP_BLOCK_EN	1	R/W	VAC OVP Block Enable. 0: Disable OVP block, 1: Enable OVP block
4	VAC_OVP_EN	1	R/W	VAC OVP enabled. 0: Disable, 1: Enable.
3	VAC_OVP [3]	1	R/W	VAC OVP threshold VAC_OVP = 4V + VAC_OVP [3:0] x 1V. Default value is 12V.
2	VAC_OVP [2]	0		
1	VAC_OVP [1]	0		
0	VAC_OVP [0]	0		

VAC Pull-Down

A VAC pull-down path of 100Ω is integrated. When REG05h bit [7] is set to 1, the VAC will be pulled down via 100Ω resistor for 400ms. After 400ms pull-down resistor is disconnected automatically and the REG05h, bit [7] will be back to 0.

VBAT and IBAT Regulation via External OVP FET

By controlling the external OVP FET, the device has a regulation feature to protect against system transients and wall adapter transients. The feature can be enabled or disabled in REG0Ah.

Bit	Name (0X0AH)	Default	Type	Description
5	IBATREG_EN	1	R/W	Enable the IBAT Regulation. 0: Disable, 1: Enable
4	IBATREG [1]	0	R/W	IBAT regulation reference. (lower than IBAT OCP)
3	IBATREG [0]	0		00: 200mA; 01: 300mA; 10: 400mA; 11: 500mA;
2	VBATREG_EN	1	R/W	Enable the VBAT regulation. 0: Disable, 1: Enable
1	VBATREG [1]	0	R/W	VBAT regulation reference. (lower than VBAT OVP)
0	VBATREG [0]	0		00: 50mV; 01: 100mV; 10: 150mV; 11: 200mV;

The regulation is accomplished by controlling the channel resistance of the external OVP FET if the regulation thresholds are met. The response time needs to be lower than 100µs when VBAT or IBAT exceeds the regulation threshold. The regulation reference can be configured via REG0Ah, bits [4:3], REG0Ah, bits [1:0]. A flag bit of REG0Dh is set when VBAT_REG or IBAT_REG has been active. The bit will be cleared once it's read. If the ET95967 stays in the regulation state for 650ms, the switching will be disabled and the Switched Cap or Bypass Mode will be reset.

VDROP Over Voltage Protection

Additionally, during the regulation if the voltage between VAC and VBUS exceeds the VDROP_OVP the threshold for configurable deglitch time, the switching will be stopped and Switched Cap or Bypass Mode is reset. If regulation is disabled, VDROP_OVP is ignored. If the regulation lasts for $t_{REG\_TIMEOUT}$, the charging will be also disabled.

Bit	Name (0X05H)	Default	Type	Description
4	VDROP_OVP_DGL	0	R/W	VDROP OVP deglitch time. 0: 10µs, 1: 5ms;
2	VDROP_OVP [2]	1	R/W	VDROP OVP threshold
1	VDROP_OVP [1]	0		VDROP_OVP = 50mV + VDROP_OVP [2:0] x 50mV.
0	VDROP_OVP [0]	1		

Comprehensive Fault Diagnostic Function

After Charge mode is enabled, before the power stage starts switching the ET95967 will implement below fault diagnostic one by one to check whether any of power pins are short. If any of short circuit condition is diagnosed, the switching will be prevented and a short circuit flag will be asserted.

● CFLY Short Circuit Diagnostic

● BUMP Short Circuit Diagnostic

● PRECONFIG short Circuit Diagnostic

CFLY Short Circuit Diagnostic

The CFLY short circuit implementation can be disabled via REG02h, bit [7].

Bit	Name (0X02H)	Default	Type	Description
7	CFLY_DIAG_EN	**OTP**	R/W	Flying capacitor short protection enable 0: Disable, 1: Enable.

Bit	Name (0X0FH)	Default	Type	Description
0	CFLY_SHORT_FLAG	0	RC	Flying capacitor short circuit flag. Set to 1 when the flying capacitor short circuit has occurred.

BUMP Short Circuit Diagnostic

The ET95967 also implements other BUMP short protection including CFL1/2 to GND, CFL1 to CFL2, CFH1/2 to VOUT, CFH1 to CFH2. It may take 1 second to go through all of the detection. An OTP to disable of the BUMP short protection can be chosen.

Bit	Name (0XECH)	Default	Type	Description
1	BUMP_DIAG_OPT	**OTP**	R/W	Bump short diagnostic enable 0: Disable 1: Enable (need OTP to change default)
Bit	**Name (0XEDH)**	**Default**	**Type**	**Description**
5	BUMP_SHORT_FLAG	0	RC	0: BUMP_SHORT is not detected 1: BUMP_SHORT is detected.

PRECONFIG short Circuit Diagnostic

The CFLY pre-charge is checked before power stage start switching. CFL1/2 short to VOUT, CFH1/2 short to PMID are detected during the pre-charge of CFLY. Charge mode is reset after PRECONFIG failed.

Protections

Prior to enable charging, set all the protections to the desired thresholds. Protections available are as below table. If any of the protection thresholds are met, the charger stops switching. The Charge mode will be reset.

Protections	Registers
WTD_TO REG00h	WTD_TO REG00h
VAC_OVP REG04h	VAC_OVP REG04h
VBUS_OVP REG06h	VBUS_OVP REG06h
IBUS_UCP REG07h	IBUS_UCP REG07h
IBUS_OCP REG07h	IBUS_OCP REG07h
VBAT_OVP REG08h	VBAT_OVP REG08h
IBAT_OCP REG09h	IBAT_OCP REG09h
VOUT_OVP Fixed: 4.9V	VOUT_OVP Fixed: 4.9V
VOUT_SCP REGEC	VOUT_SCP REGEC
RCP REGEC	RCP REGEC
TSHUT Fixed: 150°C	TSHUT Fixed: 150°C

Watchdog Time Out Protection

The Watchdog can be enabled via REG00h over I2C communication with a programmed timer from 0.5 to 80 seconds, the processor shall reset the timer by writing or reading any register before the timer is expired. If the processor fails to reset the timer before the timer is expired, charge mode is reset and watchdog timer is reset

to the default value.

Bit	Name (0X00H)	Default	Type	Description
3	WTD_DIS	0	R/W	0: Watchdog is enabled 1: Watchdog is disabled
2	WTD [2]	0	R/W	Watchdog timer setting: 000: 0.5s; 001: 1s; 010: 2s 011: 5s; 100: 10s; 101: 20s 110: 40s; 111: 80s
1	WTD [1]	0		
0	WTD [0]	0		

IBUS Under Current Protection

Once Switched Cap or Bypass Mode has been enabled, the CFLY pre-charge starts, and current will start to flow to the battery after CFLY pre-charged successfully. Raising the BUS voltage will increase the current to the battery. If using a current limited source, the voltage can be raised until reaching the current limit.

IBUS must reach IBUS_UCP rising threshold within the SS_TIMEOUT time. If the IBUS does not rise above IBUS_UCP rising threshold within SS_TIMEOUT, switching stops and Charge mode is reset. A flag bit is set if the IBUS rises above the IBUS_UCP threshold. After that, if the BUS current falls below IBUS_UCP falling, the device will stop switching. A flag bit is set if the IBUS falls under the IBUS_UCP threshold.

Bit	Name (0X0BH)	Default	Type	Description
1	IBUS_UCP_RISE_FLAG	0	RC	0: IBUS hasn't risen above the IBUS_UCP threshold. 1: IBUS has risen above the IBUS_UCP threshold.
0	IBUS_UCP_FALL_FLAG	0	RC	0: No IBUS_UCP_FALL. 1: IBUS_UCP_FALL event has occurred.

The IBUS UCP can be disabled via REG07h, bit [7]. The IBUS_UCP rising threshold can be configured in REG07h bit [6].

Bit	Name (0X07H)	Default	Type	Description
7	IBUS_UCP_EN	1	R/W	IBUS UCP enable. 0: Disable; 1: Enable.
6	IBUS_UCP_THRS	0	R/W	IBUS UCP Threshold. 0: 300mA rising, 150mA falling. 1: 500mA rising, 250mA falling.

Battery Over-voltage Protection

The device integrates both over-voltage and over-current protection for the battery. The device monitors the battery voltage on BATP and BATN. In order to reduce the possibility of battery terminal shorts during manufacturing, series resistors on BATP and BATN are required. VBAT measurement accuracy must be met with a 100Ω series resistor, but the device must still be operational with a 1kΩ resistor. If VBAT_OVP is reached for 1µs, charging stops and the Charge mode reset. Start-up sequence must be followed to resume charging.

The battery OVP threshold can be configured via REG08h, bits [5:0]. It can be disabled via REG08h, bit[7].

Bit	Name (0X08H)	Default	Type	Description
7	VBAT_OVP_EN	1	R/W	VBAT OVP enable. 0: Disable; 1: Enable.
5	VBAT_OVP [5]	0		
4	VBAT_OVP [4]	0		
3	VBAT_OVP [3]	1	R/W	VBAT_OVP threshold
2	VBAT_OVP [2]	1		VBAT_OVP = 4V + REG [5:0] * 0.025, Default value is 4.35V.
1	VBAT_OVP [1]	1		
0	VBAT_OVP [0]	0		

Battery Over-current Protection

The device monitors current through the battery by monitoring the voltage across the external series battery sense resistor. The differential voltage of this sense resistor is measured on SRP and SRN. If IBAT_OCP is reached for 50μs, charging stops and the Charge mode reset. Then the start-up sequence must be followed to resume charging.

The battery over current protection threshold can be configure via REG09h, bits [5:0]. It can be disabled via REG09h, bit [7].

Bit	Name (0X09H)	Default	Type	Description
7	IBAT_OCP_EN	1	R/W	IBAT OCP enable. 0: Disable; 1: Enable.
5	IBAT_OCP [5]	1		
4	IBAT_OCP [4]	1		
3	IBAT_OCP [3]	1	R/W	IBAT_OCP threshold
2	IBAT_OCP [2]	1		IBAT_OCP = 2A+REG [5:0]*0.1, Default value is 8.3A.
1	IBAT_OCP [1]	1		
0	IBAT_OCP [0]	1		

Output Over-voltage Protection

A fixed VOUT_OVP threshold is implemented to protect the device if the battery is removed. If VOUT_OVP is reached, the switched capacitor converter is disabled within 1μs, charge mode is reset, and the start-up sequence must be followed to resume charging. The VOUT OVP can be disabled via REGECh, bit [4].

Bit	Name (0XECH)	Default	Type	Description
4	VOUT_OVP_EN	0	R/W	VOUT OVP enable. 0: Disable; 1: Enable.

BUS Over-voltage Protection

The VBUS_OVP threshold can be configured in REG06h, bits [6:0]. When VBUS_OVP is tripped with a reaction time of 200ns, switched cap or bypass mode is disabled immediately. The VBUS OVP can be disabled

via REG06h, bit [7].

Bit	Name (0X06H)	Default	Type	Description
7	VBUS_OVP_EN	1	R/W	VBUS OVP enable. 0: Disable; 1: Enable.
6	VBUS_OVP [6]	1	R/W	VBUS OVP threshold VBUS OVP = 4V+REG [6:0]*0.1 Default value is 14V.
5	VBUS_OVP [5]	0		
4	VBUS_OVP [4]	0		
3	VBUS_OVP [3]	1		
2	VBUS_OVP [2]	0		
1	VBUS_OVP [1]	1		
0	VBUS_OVP [0]	1		

VBUS Pull-Down

The ET95967 also integrates a pull-down path of 0.9kΩ resistor to discharge the voltage if required. The VBUS pull-down path can be enabled via REG05h, bit [6]. When the REG05h, bit [6] is 1, the pull-down path will be always on (note: enable VAC pull-down will not). When the REG05h, bit [6] is 0. The pull-down path will be off normally, but it will be on automatically when external OVPFET is off caused by VAC_OVP.

Bit	Name (0X05H)	Default	Type	Description
6	VBUS_PD_EN	0	R/W	Force VBUS Pull-down enable. 0: Disable; 1: Enable.

BUS Over-current Protection

The ET95967 also monitors the current flow into VBUS. The over-current protection threshold is adjustable in the REG07h. When IBUS_OCP is tripped for 100µs, Switched Cap or Bypass Mode is disabled. The IBUS OCP can be disabled via REG07h, bits [5].

Bit	Name (0X07H)	Default	Type	Description
5	IBUS_OCP_EN	1	R/W	IBUS OCP enable. 0: Disable; 1: Enable.
4	IBUS_OCP [4]	1	R/W	IBUS OCP threshold SC mode. IBUS OCP =0.5+REG[4:0]*0.1 Bypass mode IBUS OCP =2.5+REG[4:0]*0.1
3	IBUS_OCP [3]	1		
2	IBUS_OCP [2]	0		
1	IBUS_OCP [1]	0		
0	IBUS_OCP [0]	1		

Output Short-circuit Protection

The ET95967 always measures the current flowing through reverse blocking FET, when the current exceeds the short-circuit current threshold, all of the switching FETs will be turned off immediately within 200ns and Charge mode will be reset. The VOUT SCP can be disabled via REGECh, bit [5].

Reverse Current Protection (VBUS Short-circuit Protection)

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The ET95967 also measures reverse current flowing through blocking FET from PMID to VBUS, when the reverse current is higher than 1A, all of the switching FETs will be turned off immediately within 200ns and Charge mode will be reset. The VBUS SCP can be disabled via REGECh, bit [6].

Thermal Shutdown

The device has an internal die temperature measurement, the device will automatically stop switching when it reaches the TDIE_SHUT threshold.

Fault FLAG, MASK Registers and INT Pin

The ET95967 also has numbers of flag register to indicate any flag has occurred or not. If any fault happened the corresponding register bit will be set to 1. It will be cleared to 0 after the bit is read.

REG Address	Bits	R/W	Description
0x0BH	7	RC	VAC_OVP flag.
	6	RC	VAC_PD flag.
	5	RC	VBUS_PD flag.
	4	RC	VDROP_OVP flag
	3	RC	VBUS_OVP flag
	2	RC	IBAT_OCP flag
	1	RC	IBUS_UCP_RISE flag
	0	RC	IBUS_UCP_FALL flag
0x0DH	7	RC	VBAT_OVP flag
	6	RC	IBUS_OCP flag
	5	RC	VBAT_REG flag
	4	RC	IBAT_REG flag
	3	RC	TDIE_OTP flag
	2	RC	VBUS_ERR_LOW flag
	1	RC	VBUS_ERR_HIGH flag
	0	RC	CONV_OCP flag
0x0FH	7	RC	VBUS_PRES flag
	6	RC	VBAT_PRES flag
	5	RC	WTD_TO flag
	4	RC	VAC_UVLO flag
	3	RC	VBUS_UVLO flag
	2	RC	IBUS_UCP_TO flag
	1	RC	ADC_DONE flag
	0	RC	CFLY_SHORT flag
0xEDH	7	RC	VOUT_SCP FLAG
	6	RC	RCP FLAG
	5	RC	BUMP_SHORT_FLAG
	4	RC	VOUT_OVP_FLAG

When any of above events happened, the ET95967 can be configured to send an INT pulse or not. The below

registers are designed to mask the INT output or not.

REG Address	Bits	R/W	Description
0x0CH	7	R/W	VAC_OVP INT MASK
	6	R/W	VAC_PD INT MASK
	5	R/W	VBUS_PD INT MASK
	4	R/W	VDROP_OVP INT MASK
	3	R/W	VBUS_OVP INT MASK
	2	R/W	IBAT_OCP INT MASK
	1	R/W	IBUS_UCP_RISE INT MASK
	0	R/W	IBUS_UCP_FALL INT MASK
0x0EH	7	R/W	VBAT_OVP INT MASK
	6	R/W	IBUS_OCP INT MASK
	5	R/W	VBAT_REG INT MASK
	4	R/W	IBAT_REG INT MASK
	3	R/W	TDIE_OTP INT MASK
	2	R/W	VBUS_ERR_LOW INT MASK
	1	R/W	VBUS_ERR_HIGH INT MASK
	0	R/W	CONV_OCP INT MASK
0x10H	7	R/W	VBUS_PRES INT MASK
	6	R/W	VBAT_PRES INT MASK
	5	R/W	WTD_TO INT MASK
	4	R/W	VAC_UVLO INT MASK
	3	R/W	VBUS_UVLO INT MASK
	2	R/W	IBUS_UCP_TO INT MASK
	1	R/W	ADC_DONE INT MASK
	0	R/W	CFLY_SHORT INT MASK
0xEEH	7	R/W	VOUT_SCP INT MASK
	6	R/W	RCP INT MASK
	5	R/W	BUMP_SHORT INT MASK
	4	R/W	VOUT_OVP INT MASK

When any of $\overline{INT}$ output is masked (configure to 1), the $\overline{INT}$ pulse will not be asserted when the event has occurred.

The ET95967 has an open-drain output used to launch an active-low pulse of 256µs to notify whether any fault has happened. A pull-up resistor is required to connect with system IO voltage. If the event has occurred during the I²C read operation by the host processor, the device generates the interrupt signal after a read operation. If more than one faults occurred within 500µs, only one $\overline{INT}$ pulse is asserted.

ADC

The integrated 12-bit ADC of the device allows the user to get critical system information for optimizing the behavior of the charger control. The control of the ADC is done through the ADC_CTRL register. The ADC_EN bit provides the ability to enable and disable the ADC. To enable the ADC, the ADC_EN bit must be set to '1'.

The ADC is allowed to operate if either the VBUS > VBUS_PRES or VOUT > VOUT_PRES is valid. If ADC_EN is set to '1' before VBUS or VOUT reach their respective present threshold, then the ADC conversion will be postponed until one of the power supplies reaches the threshold.

ADC Sample Channels

There are 5 channels of parameter which can be measured by ADC. By default, all ADC parameters will be converted unless disabled by configuring the REG11h, bits [5:1].

If an ADC parameter is disabled by setting the corresponding bit, then the value in that register will be from the last valid ADC conversion or the default POR value (all zeros if no conversions have taken place).

If an ADC parameter is disabled in the middle of an ADC measurement cycle, the device will finish the conversion of that parameter, but will not convert the parameter starting the next conversion cycle. Even though no conversion takes place when all ADC measurement parameters are disabled, the ADC circuitry is active and ready to begin conversion as soon as one of the channels is enabled.

ADC One-shot Mode and Continuous Mode

The integrated ADC has two rate conversion options: a one-shot mode and a continuous conversion mode set by the ADC_RATE bit. (REG11h, bit [6]).

When REG11h, bit [6] = 0, the ADC operates in continuous mode. The ADC measures selected channels constantly round by round.

When REG11h, bit [6] = 1, the ADC operates in one-shot mode. The ADC measures selected channels and stop at the end of a completed cycle of conversion. In one-shot mode, an ADC_DONE flag bit is used to indicate the conversion is completed. It has no meaning and is always 0 in continuous mode. ADC_EN will be automatically cleared to "0" after conversion is done in one-shot mode. ADC conversion operates independently of the faults present in the device. ADC conversion will continue even after a fault has occurred (such as one that causes the power stage to be disabled), and the host must set ADC_EN = '0' to disable the ADC. ADC readings are only valid for DC states and not for transients.

When the host writes ADC_EN = '0', the ADC stops immediately. If the host wants to exit ADC more gracefully, it is possible to do either of the following:

1. Write ADC_RATE to one-shot, and the ADC will stop at the end of a complete cycle of conversions

2. Write all the DIS bits high, and the ADC will stop at the end of the current measurement.

Serial Port Interface (I^{2}C)

Bus Interface

Baseband Processor can transmit data with ET95967 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected. The I2C circuitry is powered from the battery in active battery mode. The battery voltage must stay above VBAT_UVLO when no VAC is present to maintain proper operation.

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Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET95967 will send a low level response signal with one period width to the SDA port. During the reading mode, ET95967 will not send response signal and the host will send a high response signal one period width to the SDA.

Figure 6.　I^{2}C write mode
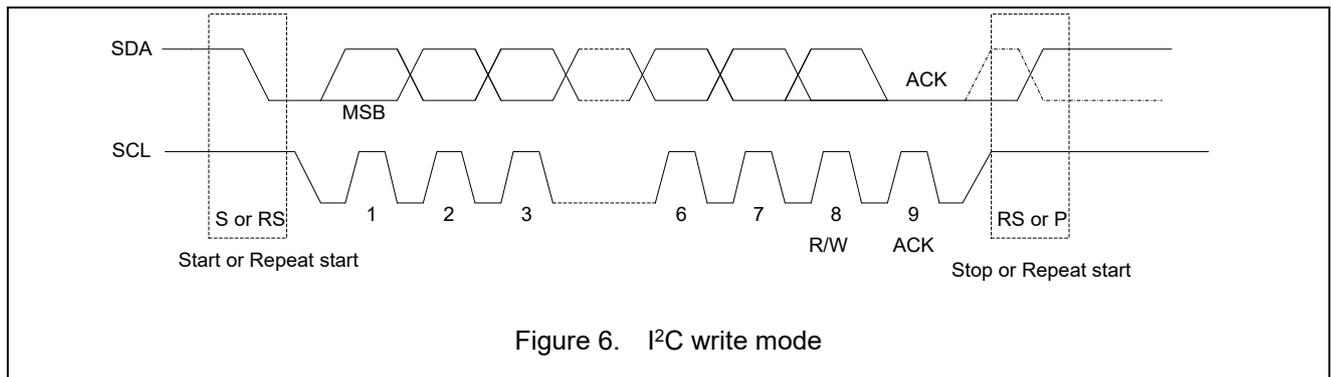
- ACK=Acknowledge
- MSB=Most Significant Bit
- S=Start Conditions
- RS=Restart Conditions
- P=Stop Conditions
- Fastest Transmission Speed =1000KBITS/S

  Restart: SDA-level turnover as expressed by the dashed line waveform

I^{2}C Slave Address

The default 7bit I^{2}C slave address is 1100101b(0x65), and 8bit address for the writing register mode is 11001010b(0xCA), the reading register mode is 11001011b(0xCB). To avoid I^{2}C hang-ups, a timer (TI2CRESET) runs during I^{2}C transactions. If the transaction takes longer than TI2CRESET, any additional commands are ignored and the I^{2}C engine is reset. The timeout is reset with START and repeated START conditions and stops when a valid STOP condition is sent.

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I²C Writing Command Register Interface Protocol (continuous)：
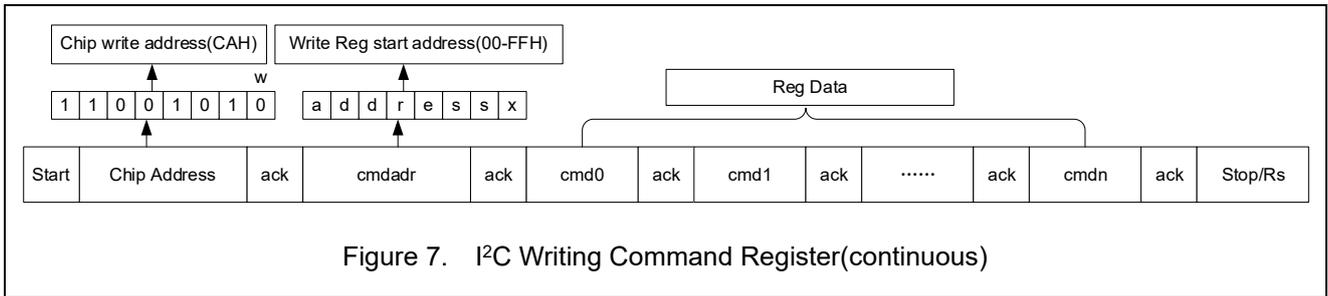
Figure 7.   I²C Writing Command Register(continuous)

- Start=Start Conditions

- Chip address=Write register address =1100101+0(w)b

- ack=Acknowledge from ET95967

- Write Reg start address byte = cmdadr(REG's 8bit addressx)

- ack=Acknowledge from ET95967

- Reg data 0 = cmd0(Command data0)

- ack=Acknowledge from ET95967

- ……………

- Reg data n =cmdn(Command datan)

- ack=Acknowledge from ET95967

- Stop/Rs=Stop Condition/Restart Condition

I²C Writing Command Register Interface Protocol (single)：
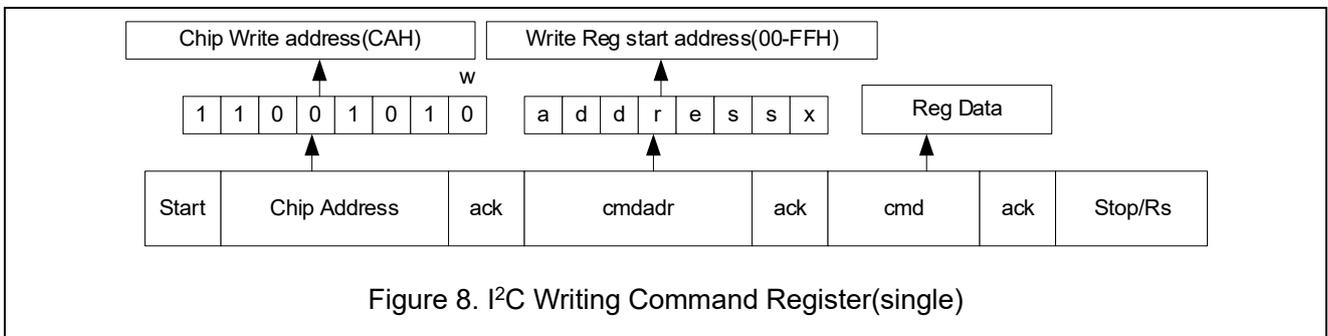
Figure 8. I²C Writing Command Register(single)

- Start=Start Conditions

- Chip address =Write register address=1100101+0(w)b

- ack=Acknowledge from ET95967

- Write Reg start address byte = cmdadr(REG's 8bit addressx)

- ack=Acknowledge from ET95967

- Reg data= cmd(Command data)

- ack=Acknowledge from ET95967

- Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol(continuous)

Figure 9. I²C Reading Command Register(continuous)

- Start=Start Conditions
- Chip address =Write register address=1100101+0(w)b
- ack=Acknowledge from ET95967
- Write Reg start address byte = cmdadr(REG's 8bit addressx)
- ack=Acknowledge from ET95967
- Restart=Restart condition
- Chip address Read register address=1100101+1(r)b
- ack=Acknowledge from ET95967
- Dataout0=Register data output 0
- ack=Acknowledge from Host
- ……………
- Dataoutn=Register data output n
- nack=No Acknowledge from Host
- Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol(single)

Figure 10.   I²C Reading Command Register(single)
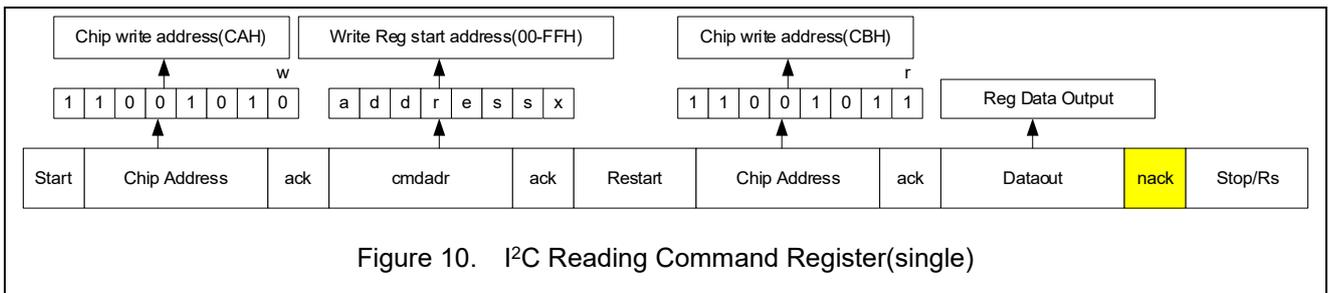
- Start=Start Conditions
- Chip address =Write register address=1100101+0(w)b
- ack=Acknowledge from ET95967
- Write Reg start address byte = cmdadr(REG's 8bit addressx)
- ack=Acknowledge from ET95967
- Restart=Restart condition
- Chip address Read register address=1100101+1(r)b
- ack=Acknowledge from ET95967
- Dataout=Register data output
- nack=No Acknowledge from Host
- Stop/Rs=Stop Condition/Restart Condition

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Register Map

Addr	Name	RST	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	CONTROL1	0x00	REG_RST	MODE [2:0]			WTD_DIS	WTD [2:0]		
0x01	CONTROL2	0x40	PSW_SET [2:0]			DITHER [1:0]		Reserved		
0x02	CONTROL3	0x3C or 0xBC	CFLY_DIAG_EN	Reserved	VBUS_ERR_LOW_EN	VBUS_ERR_HI_EN	VBUS_ERR_LOW_REF [1:0]		VBUS_ERR_HI_REF [1:0]	
0x03	DEV_INFO	0x00	DEVICE_VER [3:0]				DEVICE ID [3:0]			
0x04	VAC_OVP	0x38	Reserved		VAC_OVP_BLOCK_EN	VAC_OVP_EN	VAC_OVP [3:0]			
0x05	VDROP_OVP	0x05	VAC_PD_EN	VBUS_PD_EN	Reserved	VDROP_OVP_DGL	Reserved	VDROP_OVP [2:0]		
0x06	VBUS_OVP	0xCB	VBUS_OVP_EN	VBUS_OVP [6:0]						
0x07	IBUS_OCP	0xB9	IBUS_UCP_EN	IBUS_UCP_THRS	IBUS_OCP_EN	IBUS_OCP [4:0]				
0x08	VBAT_OVP	0x8E	VBAT_OVP_EN	Reserved	VBAT_OVP [5:0]					
0x09	IBAT_OCP	0xBF	IBAT_OCP_EN	Reserved	IBAT_OCP [5:0]					
0x0A	REGULATION	0x24	Reserved		IBATREG_EN	IBATREG [1:0]		VBATREG_EN	VBATREG [1:0]	
0x0B	FLT_FLAG1	0x00	VAC_OVP_FLAG	VAC_PD_FLAG	VBUS_PD_FLAG	VDROP_OVP_FLAG	VBUS_OVP_FLAG	IBUS_OCP_FLAG	IBUS_UCP_RISE_FLAG	IBUS_UCP_FALL_FLAG
0x0C	FLT_INT_MASK1	0x00	VAC_OVP_MASK	VAC_PD_MASK	VBUS_PD_MASK	VDROP_OVP_MASK	VBUS_OVP_MASK	IBUS_OCP_MASK	IBUS_UCP_RISE_MASK	IBUS_UCP_FALL_MASK
0x0D	FLT_FLAG2	0x00	VBAT_OVP_FLAG	IBAT_OCP_FLAG	VBAT_REG_FLAG	IBAT_REG_FLAG	TDIE_OTP_FLAG	VBUS_ERR_LOW_FLAG	VBUS_ERR_HIGH_FLAG	CONV_OCP_FLAG
0x0E	FLT_INT_MASK2	0x00	VBAT_OVP_MASK	IBAT_OCP_MASK	VBAT_REG_MASK	IBAT_REG_MASK	TDIE_OTP_MASK	VBUS_ERR_LOW_MASK	VBUS_ERR_HIGH_MASK	CONV_OCP_MASK
0x0F	FLT_FLAG3	0x00	VBUS_PRES_FLAG	VBAT_PRES_FLAG	WTD_TO_FLAG	VAC_UVLO_FLAG	VBUS_UVLO_FLAG	IBUS_UCP_TO_FLAG	ADC_DONE_FLAG	CFLY_SHORT_FLAG
0x10	FLT_INT_MASK3	0x00	VBUS_PRES_MASK	VBAT_PRES_MASK	WTD_TO_MASK	VAC_UVLO_MASK	VBUS_UVLO_MASK	IBUS_UCP_TO_MASK	ADC_DONE_MASK	CFLY_SHORT_MASK
0x11	ADC_CTRL	0x00	ADC_EN	ADC_RATE	VBUS_ADC_DIS	IBUS_ADC_DIS	VBAT_ADC_DIS	IBAT_ADC_DIS	TDIE_ADC_DIS	Reserved
0x12	VBUS_ADC1	0x00	Reserved				VBUS_ADC [11:8]			
0x13	VBUS_ADC0	0x00	VBUS_ADC [7:0]							
0x14	IBUS_ADC1	0x00	Reserved				IBUS_ADC [11:8]			
0x15	IBUS_ADC0	0x00	IBUS_ADC [7:0]							
0x16	VBAT_ADC1	0x00	Reserved				VBAT_ADC [11:8]			
0x17	VBAT_ADC0	0x00	VBAT_ADC [7:0]							
0x18	IBAT_ADC1	0x00	Reserved				IBAT_ADC [11:8]			
0x19	IBAT_ADC0	0x00	IBAT_ADC [7:0]							
0x1A	TDIE_ADC	0x00	TDIE_ADC [7:0]							
0x40	UFCS_CTRL1	0x00	PROTOCOL_EN [1:0]		EN_UFCS_HDSK	BAUD_RATE [1]	BAUD_RATE [0]	SNDCMD	Cable_HDRST	Source_HDRST
0x41	UFCS_CTRL2	0x00	Reserved						Device Address ID	DM_HIZ_EN

0x42	UFCS_ISR1	0x00	UFCS_HDSK_FAIL_FLAG	UFCS_HDSK_SUCC_FLAG	BAUD_RATE_ERR_FLAG	CRC_ERR_FLAG	SENT_PKT_CMP_FLAG	DATA_RDY_FLAG	HD_RST_FLAG	ACK_RX_TO_FLAG
0x43	UFCS_ISR2	0x00	Reserved	RX_RUF_OVER FLOW_FLAG	RX_LENGTH_ERR_FLAG	BAUD_RATE_CHG_FLAG	FARME_RX_TO_FLAG	RX_BUFF_BUSY_FLAG	MSG_TRANS_FAIL_FLAG	TRAIN_BYTE_ERR_FLAG
0x44	UFCS_MASK1	0x00	UFCS_HDSK_FAIL_MASK	UFCS_HDSK_SUCC_MASK	BAUD_RATE_ERR_MASK	CRC_ERR_MASK	SENT_PKT_CMP_MASK	DATA_RDY_MASK	HD_RST_MASK	ACK_RX_TO_MASK
0x45	UFCS_MASK2	0x00	Reserved	RX_RUF_OVER FLOW_MASK	RX_LENGTH_ERR_MASK	BAUD_RATE_CHG_MASK	FARME_RX_TO_MASK	RX_BUFF_BUSY_MASK	MSG_TRANS_FAIL_MASK	TRAIN_BYTE_ERR_MASK
0x46	DURPBIT	0x00	DUR_BIT [7:0]							
0x47	TX_LENGTH	0x00	TX_LENGTH [7:0]							
0x48	TX_BUFFER0	0x00	TX_BUFFER0							
0x49 ⋮ 0x6A	TX_BUFFER1 ~ TX_BUFFER34	0x00	TX_BUFFER1 ~ 34							
0x6B	TX_BUFFER35	0x00	TX_BUFFER35							
0x6C	RX_LENGTH	0x00	RX_LENGTH [7:0]							
0x6D	RX_BUFFER0	0x00	RX_BUFFER0							
0x6E ⋮ 0xE8	RX_BUFFER1 ~ RXBUFFER123	0x00	RX_BUFFER1 ~123							
0xE9	RX_BUFFER124	0x00	RX_BUFFER124							
0xEC	CONTROL4	0x62 & OTP	VBUS_ERR_OPT	RCP_EN	SCP_EN	VOUT_OVP_EN	RSNS_OPT	OVP_GATE_OPT	BUMP_DIAG_OPT	Reserved
0xED	FLT_FLAG4	0x00	VOUT_SCP Flag	RCP Flag	BUMP_SHORT Flag	VOUT_OVP_flag	Reserved			
0xEE	FLT_INT_FLAG4	0x00	VOUT_SCP_MASK	RCP_MASK	BUMP_SHORT_MASK	VOUT_OVP_MASK	Reserved			
0xF0 ⋮ 0xFF	TEST REG	/	OTP bank for internal use							

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- **0x00 CONTROL1, Default = 0x00**

Bit	Name	Default	Type	Reset Type	Description
7	REG_RST	0	W/C	by REG_RST	0: No register reset 1: Reset register value to default mode
6	MODE [2]	0	R/W	by REG_RST, by Watchdog, by many protection events	Charge mode control 000: Off mode 001: Bypass mode (1:1) 010: Switched cap mode (2:1) 011~111: Off mode
5	MODE [1]	0	R/W		
4	MODE [0]	0	R/W		
3	WTD_DIS	0	R/W	by REG_RST	0: Watchdog is enabled 1: Watchdog is disabled
2	WTD [2]	0	R/W		Watchdog timer setting: 000: 0.5s 001: 1s 010: 2s 011: 5s 100: 10s 101: 20s 110: 40s 111: 80s
1	WTD [1]	0	R/W		
0	WTD [0]	0	R/W		

- **0x01 CONTROL2, Default = 0x40**

Bit	Name	Default	Type	Reset Type	Description
7	FSW_SET [2]	0	R/W	by REG_RST	Set the switching frequency 000: 200kHz 001: 375kHz 010: 500kHz 011: 750kHz 100: 1000kHz 101: 1250kHz 110/111: 1500kHz
6	FSW_SET [1]	1	R/W		
5	FSW_SET [0]	0	R/W		
4	DITHERING [1]	0	R/W		FSW dithering setting: 00/11: Nominal Frequency 01: +10% 10: -10%
3	DITHERING [0]	0	R/W		
2		0	R/W		
1	Reserved	0	R/W		
0		0	R/W		

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- **0x02 CONTROL3, Default = 0x3C or 0xBC**

Bit	Name	Default	Type	Reset Type	Description
7	CFLY_DIAG_EN	**OTP**	R/W	by REG_RST	Flying capacitor short protection enable 0: Disable 1: Enable
6	Reserved	0	R/W		
5	VBUS_ERR_LO W_EN	1	R/W	by REG_RST	VBUS Error Low Voltage check 0: Disable 1: Enable
4	VBUS_ERR_H IG H_EN	1	R/W		VBUS Error High Voltage check 0: Disable 1: Enable
3	VBUS_ERR_LO W_REF [1]	1	R/W		VBUS Error Low Voltage Threshold 00: 1.01 01: 1.02 10: 1.03 11: 1.04
2	VBUS_ERR_LO W_REF [0]	1	R/W		
1	VBUS_ERR_HI_ REF [1]	0	R/W		VBUS Error High Voltage Threshold 00: 1.1 01: 1.15 10: 1.2 11: 1.25
0	VBUS_ERR_HI_ REF [0]	0	R/W		

- **0x03   Dev_INFO, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	DEVICE_VER [3]	0	R	/	
6	DEVICE_VER [2]	0	R		
5	DEVICE_VER [1]	0	R		
4	DEVICE_VER [0]	0	R		
3	DEVICE_ID [3]	0	R		
2	DEVICE_ID [2]	0	R		
1	DEVICE_ID [1]	0	R		
0	DEVICE_ID [0]	0	R		

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- **0x04   VAC_OVP, Default =0x38**

Bit	Name	Default	Type	Reset Type	Description
7	Reserved	0	R/W		
6		0	R/W		
5	VAC_OVP _BLOCK_EN	1	R/W	by REG_RST	VAC OVP Block Enable 0: Disable OVP gate driver 1: Enable OVP gate driver
4	VAC_OVP_EN	1	R/W		VAC OVP enable 0: Disable 1: Enable
3	VAC_OVP [3]	1	R/W		
2	VAC_OVP [2]	0	R/W		VAC_OVP = 4V+VAC_OVP [3:0] x 1V
1	VAC_OVP [1]	0	R/W		
0	VAC_OVP [0]	0	R/W		

- **0x05   VDROP_OVP, Default =0x05**

Bit	Name	Default	Type	Reset Type	Description
7	VAC_PD_EN	0	R/WC	by REG_RST	VAC pull-down enable. 0: Disable 1: Enable It will be back to 0 after 400ms
6	VBUS_PD_EN	0	R/W		VBUS pull-down enable 0: Disable 1: Enable
5	Reserved	0	R/W		
4	VDROP_OVP _DGL	0	R/W		Deglitch time after device reaches VDROP threshold before stop switching 0: 10us 1: 5ms
3	Reserved	0	R/W		
2	VDROP_OVP [2]	1	R/W		VDROP OVP threshold Offset: 50mV VDROP_OVP = 50mV + VDROP_OVP [2:0] * 50mV
1	VDROP_OVP [1]	0	R/W		
0	VDROP_OVP [0]	1	R/W		

- **0x06   VBUS_OVP, Default =0xCB**

Bit	Name	Default	Type	Reset Type	Description
7	VBUS_OVP_EN	1	R/W	by REG_RST	VBUS_OVP enable 0: Disable 1: Enable
6	VBUS_OVP [6]	1	R/W		VBUS over voltage protection Offset: 4000mV VBUS_OVP = 4000mV + VBUS_OVP [6:0] * 100mV When VBUS_OVP [6:0] >=1100100, VBUS_OVP = 14V
5	VBUS_OVP [5]	0	R/W		
4	VBUS_OVP [4]	0	R/W		
3	VBUS_OVP [3]	1	R/W		
2	VBUS_OVP [2]	0	R/W		
1	VBUS_OVP [1]	1	R/W		
0	VBUS_OVP [0]	1	R/W		

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- **0x07   IBUS_OCP, Default =0xB9**

Bit	Name	Default	Type	Reset Type	Description
7	IBUS_UCP _EN	1	R/W	by REG_RST	IBUS UCP enable 0: Disable 1: Enable
6	IBUS_UCP _THRS	0	R/W		IBUS UCP threshold: 0: 300mA rising, 150mA falling 1: 500mA rising, 250mA falling
5	IBUS_OCP _EN	1	R/W		IBUS OCP enable 0: Disable 1: Enable
4	IBUS_OCP [4]	1	R/W		SC mode: IBUS_OCP = 500mA + IBUS_OCP [4:0] * 100mA Bypass mode IBUS_OCP = 2500mA + IBUS_OCP [4:0] * 100mA
3	IBUS_OCP [3]	1	R/W		
2	IBUS_OCP [2]	0	R/W		
1	IBUS_OCP [1]	0	R/W		
0	IBUS_OCP [0]	1	R/W		

- **0x08   VBAT_OVP, Default =0x8E**

Bit	Name	Default	Type	Reset Type	Description
7	VBAT_OVP _EN	1	R/W	by REG_RST	VBAT_OVP Enable 0: Disable 1: Enable
6	Reserved	0	R/W		
5	VBAT_OVP [5]	0	R/W	by REG_RST	VBAT OVP threshold setting Offset: 4000mV VBAT_OVP = 4000mV + VBAT_ OVP [5:0] * 25mV
4	VBAT_OVP [4]	0	R/W		
3	VBAT_OVP [3]	1	R/W		
2	VBAT_OVP [2]	1	R/W		
1	VBAT_OVP [1]	1	R/W		
0	VBAT_OVP [0]	0	R/W		

- **0x09   IBAT_OCP, Default =0xBF**

Bit	Name	Default	Type	Reset Type	Description
7	EN_IBAT _OCP	1	R/W	by REG_RST	Enable IBAT_OCP 0: Disable 1: Enable
6	Reserved	0	R/W		
5	IBAT_OCP [5]	1	R/W	by REG_RST	IBAT_OCP Setting IBAT_OCP = 2000mA + REG [5:0] * 100mA Default = 8300mA
4	IBAT_OCP [4]	1	R/W		
3	IBAT_OCP [3]	1	R/W		
2	IBAT_OCP [2]	1	R/W		
1	IBAT_OCP [1]	1	R/W		
0	IBAT_OCP [0]	1	R/W		

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■ **0x0A Regulation, Default =0x24**

Bit	Name	Default	Type	Reset Type	Description
7	Reserved	0	RW		
6	Reserved	0	R/W		
5	IBATREG_EN	1	R/W	by REG_RST	Enable IBAT Regulation 0: Disable 1: Enable
4	IBATREG [1]	0	R/W		IBAT regulation setting 00: 200mA below IBATOCP setting 01: 300mA below IBATOCP setting 10: 400mA below IBATOCP setting 11: 500mA below IBATOCP setting
3	IBATREG [0]	0	R/W		
2	VBATREG_EN	1	R/W		Enable VBAT Regulation 0: Disable 1: Enable
1	VBATREG [1]	0	R/W		VBAT Regulation Setting 00: 50mV below VBATOVP setting 01: 100mV below VBATOVP setting 10: 150mV below VBATOVP setting 11: 200mV below VBATOVP setting
0	VBATREG [0]	0	R/W		

■ **0x0B FLT_FLAG1, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	VAC_OVP _FLA G	0	RC		This bit is set when VAC_OVP has been active. 0: No VAC_OVP 1: VAC_OVP has occurred
6	VAC_PD _FLAG	0	RC		This bit is set when VAC pull-down has been active. 0: No VAC pull-down 1: VAC pull-down has occurred
5	VBUS_PD_FL A G	0	RC		This bit is set when VBUS pull-down has been active. 0: No VBUS pull-down 1: VBUS pull-down has occurred
4	VDROP_OVP _ FLAG	0	RC		This bit is set when VDROP_OVP has been active. 0: No VDROP_OVP 1: VDROP_OVP has occurred

3	VBUS_OVP_F L AG	0	RC		This bit is set when VBUS_OVP has been active. 0: No VBUS_OVP 1: VBUS_OVP has occurred
2	IBUS_OCP_F L AG	0	RC		Indicates a BUS Over-Current Event has occurred 0: No IBUS_OCP 1: IBUS_OCP has occurred.
1	IBUS_UCP_RI SE_FLAG	0	RC		Bus Under-Current threshold rising flag. An INT is sent when this occurs, and is cleared upon read 0: No IBUS_UCP_RISE 1: IBUS_UCP_RISE event has occurred
0	IBUS_UCP_F A LL_FLAG	0	RC		Bus Under-Current threshold falling flag. An INT is sent when this occurs, and is cleared upon read. 0: No IBUS_UCP_FALL 1: IBUS_UCP_FALL event has occurred--- **this is IBUS_UCP fault**

- **0x0C   FLT_INT_MASK1, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	VAC_OVP _MA SK	0	R/W	by REG_RST	Masks VAC Over-voltage Event INT 0 = Not masked 1 = Masked
6	VAC_PD _MAS K	0	R/W		VAC pull-down event INT 0 = Not Masked 1 = Masked
5	VBUS_PD _MA SK	0	R/W		VBUS pull-down event INT 0 = Not Masked 1 = Masked
4	VDROP_OVP _ MASK	0	R/W		VDROP_OVP INT 0 = Not Masked 1 = Masked
3	VBUS_OVP _M ASK	0	R/W		VBUS Over-voltage event INT 0 = Not Masked 1 = Masked
2	IBUS_OCP _MA SK	0	R/W		Masks IBUS Over-Current INT 0 = Not Masked 1 = Masked
1	IBUS_UCP _RI SE_MASK	0	R/W		Bus Under Current Rising INT 0 = Not Masked 1 = Masked
0	IBUS_UCP _FA LL_MASK	0	R/W		Bus Under Current Falling INT 0 = Not Masked 1 = Masked

- **0x0D   FLT_FLAG2, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	VBAT_OVP _FL AG	0	RC		This bit is set when VBAT_OVP has been active. 0: No VBAT_OVP 1: VBAT_OVP has occurred
6	IBAT_OCP _FL AG	0	RC		This bit is set when IBAT_OCP has been active. 0: No IBAT_OCP 1: IBAT_OCP has occurred
5	VBAT_REG _FL AG	0	RC		This bit is set when VBAT_REG has been active. While VBATREG_EN=1 (REG0A [2]) 0: No VBAT_REG 1: VBAT_REG has occurred
4	IBAT_REG _FL AG	0	RC		This bit is set when IBAT_REG has been active. While IBATREG_EN=1 (REG0A [5]) 0: No IBAT_REG 1: IBAT_REG has occurred
3	TDIE_OTP _FL AG	0	RC		This bit is set when TDIE_OTP has been active. 0: No TDIE_OTP 1: TDIE_OTP has occurred
2	VBUS_ERR _L OW_FLAG	0	RC		This bit is set when VBUS Low Voltage error has been active 0: No VBUS_ERR_LOW fault. 1: VBUS_ERR_LOW fault has occurred.
1	VBUS_ERR _HI GH_FLAG	0	RC		This bit is set when VBUS High Voltage error has been active 0: No VBUS_ERR_HIGH fault. 1: VBUS_ERR_HIGH fault has occurred.
0	CONV_OCP _F LAG	0	RC		This bit set when converter OCP has occurred. 0: No CONV_OCP 1: CONV_OCP has occurred

- **0x0E   FLT_INT_MASK2, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	VBAT_OVP_M ASK	0	R/W	by REG_RST	Masks VBAT Over-voltage Event INT 0 = Not masked. 1 = Masked
6	IBAT_OCP_MA SK	0	R/W		Masks IBAT Over-current Event INT 0 = Not masked. 1 = Masked
5	VBAT_REG_M ASK	0	R/W		Masks VBAT regulation Event INT 0 = Not masked. 1 = Masked
4	IBAT_REG_MA SK	0	R/W		Masks IBAT regulation Event INT 0 = Not masked. 1 = Masked
3	TDIE_OTP_MA SK	0	R/W		Masks TDIE Over-temperature INT 0 = Not masked. 1 = Masked
2	VBUS_ERR_L OW_MASK	0	R/W		Masks VBUS low voltage INT 0 = Not masked. 1 = Masked
1	VBUS_ERR_HIGH_MASK	0	R/W		Masks VBUS high voltage INT 0 = Not masked. 1 = Masked
0	CONV_OCP_M ASK	0	R/W		Masks Converter Over Current INT 0 = Not masked. 1 = Masked

- **0x0F   FLT_FLAG3, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	VBUS_PRES_ FLAG	0	RC		VBUS present Flag 0: VBUS is not present yet 1: VBUS has been present
6	VBAT_PRES_F LAG	0	RC		VBAT present Flag 0: VBAT is not present yet 1: VBAT has been present
5	WTD_TO_FLA G	0	RC		WTD Timer Out Flag 0: Watchdog is not time out 1: Watchdog has been time out
4	VAC_UVLO_FL AG	0	RC		VAC UVLO Flag 0: VAC_UVLO has not occurred. 1: VAC_UVLO has occurred.
3	VBUS_UVLO_ FLAG	0	RC		VBUS UVLO Flag 0: VBUS_UVLO has not occurred. 1: VBUS_UVLO has occurred.
2	IBUS_UCP_TO FLAG	0	RC		IBUS UCP Time out Flag 0: No time out 1: Time out, doesn't rise over UCP rising

					threshold in set time.
1	ADC_DONE _F LAG	0	RC		ADC_DONE flag, need this flag in one-shot mode 0: No ADC_DONE 1: ADC_DONE
0	CFLY_SHORT _ FLAG	0	RC		Flying capacitor short protection has occurred 0: No flying capacitor short 1: Flying capacitor short has occurred.

■   **0x10   FLT_MASK3, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	VBUS_PRES _ MASK	0	R/W	by REG_RST	VBUS voltage has been present and above the VBUS UVLO threshold event INT mask 0: Not Masked 1: Masked
6	VBAT_PRES _MASK	0	R/W		VBAT voltage has been present and above the VBAT UVLO threshold event INT mask 0: Not Masked 1: Masked
5	WTD_TO _MAS K	0	R/W		Watchdog Timeout Flag Event INT Mask 0: Not Masked 1: Masked
4	VAC_UVLO _M ASK	0	R/W		VAC UVLO INT mask 0: Not Masked 1: Masked
3	VBUS_UVLO _ MASK	0	R/W		VBUS UVLO INT mask 0: Not Masked 1: Masked
2	IBUS_UCP _TO	0	R/W		IBUS_UCP Timer out FLAG INT mask 0: Not Masked 1: Masked
1	ADC_DONE _M ASK	0	R/W		ADC_DONE Flag INT mask 0: Not Masked 1: Masked
0	CFLY_SHORT _ MASK	0	R/W		Flying cap short event INT mask 0: Not Masked 1: Masked

■   **0x11   ADC_CTRL, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	ADC_EN	0	R/W	by REG_RST, by Watchdog	Enable ADC 0 = Disabled 1 = Enabled
6	ADC_RATE	0	R/W	by REG_RST	0 = Continuous Conversion 1 = One-shot
5	VBUS_ADC _DIS	0	R/W		VBUS channel disable 0: Enable 1: Disable
4	IBUS_ADC _DIS	0	R/W		IBUS channel disable 0: Enable 1: Disable
3	VBAT_ADC	0	R/W		VBAT channel disable 0: Enable 1: Disable

	_DIS				
2	IBAT_ADC _DIS	0	R/W		IBAT channel disable 0: Enable 1: Disable
1	TDIE_ADC _DIS	0	R/W		TDIE channel disable 0: Enable 1: Disable
0	Reserved	0	R/W		

- **0x12~0x13   VBUS_ADC1-ADC0, Default =0x0000**

Bit	Name	Default	Type	Reset Type	Description
7	Reserved	0	R		
6	Reserved	0	R		
5	Reserved	0	R		
4	Reserved	0	R		
3	VBUS_ADC [11]	0	R		
2	VBUS_ADC [10]	0	R		
1	VBUS_ADC [9]	0	R		
0	VBUS_ADC [8]	0	R		
7	VBUS_ADC [7]	0	R		
6	VBUS_ADC [6]	0	R	by REG_RST	VBUS_ADC = VBUS_ADC [11:0] x 4mV
5	VBUS_ADC [5]	0	R		
4	VBUS_ADC [4]	0	R		
3	VBUS_ADC [3]	0	R		
2	VBUS_ADC [2]	0	R		
1	VBUS_ADC [1]	0	R		
0	VBUS_ADC [0]	0	R		

- **0x14~0x15   IBUS_ADC1-ADC0, Default =0x0000**

Bit	Name	Default	Type	Reset Type	Description
7	Reserved	0	R		
6	Reserved	0	R		
5	Reserved	0	R		
4	Reserved	0	R		
3	IBUS_ADC [11]	0	R		
2	IBUS_ADC [10]	0	R	by REG_RST	IBUS_ADC = IBUS_ADC [11:0] x 2mA
1	IBUS_ADC [9]	0	R		
0	IBUS_ADC [8]	0	R		

7	IBUS_ADC [7]	0	R		
6	IBUS_ADC [6]	0	R		
5	IBUS_ADC [5]	0	R		
4	IBUS_ADC [4]	0	R		
3	IBUS_ADC [3]	0	R		
2	IBUS_ADC [2]	0	R		
1	IBUS_ADC [1]	0	R		
0	IBUS_ADC [0]	0	R		

- **0x16~0x17   VBAT_ADC1-ADC0, Default =0x0000**

Bit	Name	Default	Type	Reset Type	Description
7	Reserved	0	R		
6	Reserved	0	R		
5	Reserved	0	R		
4	Reserved	0	R		
3	VBAT_ADC [11]	0	R	by REG_RST	VBAT_ADC = VBAT_ADC [11:0] x 2mV
2	VBAT_ADC [10]	0	R		
1	VBAT_ADC [9]	0	R		
0	VBAT_ADC [8]	0	R		
7	VBAT_ADC [7]	0	R		
6	VBAT_ADC [6]	0	R		
5	VBAT_ADC [5]	0	R		
4	VBAT_ADC [4]	0	R		
3	VBAT_ADC [3]	0	R		
2	VBAT_ADC [2]	0	R		
1	VBAT_ADC [1]	0	R		
0	VBAT_ADC [0]	0	R		

- **0x18~0x19   IBAT_ADC1-ADC0, Default =0x0000**

Bit	Name	Default	Type	Reset Type	Description
7	Reserved	0	R		
6	Reserved	0	R		
5	Reserved	0	R		
4	Reserved	0	R		

3	IBAT_ADC [11]	0	R		
2	IBAT_ADC [10]	0	R		
1	IBAT_ADC [9]	0	R		
0	IBAT_ADC [8]	0	R		
7	IBAT_ADC [7]	0	R		
6	IBAT_ADC [6]	0	R	by REG_RST	IBAT_ADC = IBAT_ADC [11:0] x 2mV
5	IBAT_ADC [5]	0	R		
4	IBAT_ADC [4]	0	R		
3	IBAT_ADC [3]	0	R		
2	IBAT_ADC [2]	0	R		
1	IBAT_ADC [1]	0	R		
0	IBAT_ADC [0]	0	R		

- **0x1A   TDIE_ADC, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	TDIE [7]	0	R		
6	TDIE [6]	0	R		
5	TDIE [5]	0	R		
4	TDIE [4]	0	R	by REG_RST	TDIE_ADC=TDIE [7:0]-40°C
3	TDIE [3]	0	R		
2	TDIE [2]	0	R		
1	TDIE [1]	0	R		
0	TDIE [0]	0	R		

- **0x40   UFCS_CTRL1, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	PROTOCOL_EN [1]	0	R/W		01: Reserved
6	PROTOCOL_EN [0]	0	R/W	by REG_RST, by Watchdog, by PROTOCOL_EN falling edge	10: Enable UFCS 00/11: Disable UFCS
5	EN_UFCS_HDSK	0	R/W		UFCS Handshake Enable 0: Disable UFCS handshake 1: Enable UFCS handshake
4	BAUD_RATE [1]	0	R/W		00: 115200bps 01: 57600bps
3	BAUD_RATE [0]	0	R/W		10: 38400bps 11: 19200bps

2	SNDCMD	0	R/WC		Transition start 0: Not transition 1: Start transition
1	Cable _HDRST	0	R/WC		Sent HardresetCable 0: Not sent HardresetCable 1: Sent HardresetCable
0	Source _HDRST	0	R/WC		Sent_HardresetSource 0: Not sent HardresetSource 1: Sent HardsresetSource

- **0x41   UFCS_CTRL2, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	Reserved	0	R/W		
6	Reserved	0	R/W		
5	Reserved	0	R/W		
4	Reserved	0	R/W		
3	Reserved	0	R/W		
2	Reserved	0	R/W		
1	Device Address ID	0	R/W	by REG_RST, by Watchdog, by PROTOCOL_EN falling edge	0: Source 1: Cable
0	DM_HIZ_EN	0	R/W		Set DM_HIZ 0: Disable DM_HIZ 1: Enable DM_HIZ

- **0x42   UFCS_ISR1, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	UFCS_HDSK_FAIL_FLAG	0	RC		0: UFCS handshake not completed or succeed 1: UFCS handshake failed
6	UFCS_HDSK_SUCC_FLAG	0	RC		0: UFCS handshake not completed or failed 1: UFCS handshake succeed
5	BAUD_RATE_ERR_FLAG	0	RC		0: Baud rate check OK 1: Baud rate error
4	CRC_ERR_FLAG	0	RC		0: CRC check OK 1: CRC error
3	SENT_PKT_CMP_FLAG	0	RC		0: Sent packet not completed or failed 1: Sent packet completed

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2	DATA_RDY_FL AG	0	RC		0: Not ready 1: Ready
1	HD_RST_FLA G	0	RC		UFCS receive Hard_Reset command 0: UFCS do NOT receive Hard_Reset 1: UFCS receive Hard_Reset
0	ACK_RX_TO_F LAG	0	RC		0: No ACK receive timeout event 1: ACK receive timeout

■ **0x43   UFCS_ISR2, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	Reserved	0	RC		
6	RX_BUFF_OVERFLOW_FLAG	0	RC		0: RX buffer not overflow 1: RX buffer overflow
5	RX_LENGTH_E RR_FLAG	0	RC		0: RX length is not error. 1: RX length is error.
4	BAUD_RATE_CHG_FLAG	0	RC		0: Baud rate don't change 1: Baud rate changed after RX ping message with different baud rate.
3	FRAME_RX_TO_FLAG	0	RC		0: Frame receive timer is not out 1: Frame receive timer is out.
2	RX_BUFF_BUSY FLAG	0	RC		0: The RX buffer data is empty when receives message 1: The last RX buffer data has not been read
1	MSG_TRANS_FAIL_FLAG	0	RC		0: Message transfer not fail 1: Message transfer fails
0	TRAIN_BYTE_ERR_FLAG	0	RC		0: Training byte is right. 1: Training byte is error.

■ **0x44   UFCS_MASK1, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	UFCS_HDSK_FAIL_MASK	0	R/W	by REG_RST	0: Not masked. 1: Masked
6	UFCS_HDSK_SUCC_MASK	0	R/W		0: Not masked. 1: Masked
5	BAUD_RATE_ERR_MASK	0	R/W		0: Not masked. 1: Masked
4	CRC_ERR_MASK	0	R/W		0: Not masked. 1: Masked
3	SENT_PKT	0	R/W		0: Not masked.

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Bit	Name	Default	Type	Reset Type	Description
	_CMP_MASK				1: Masked
2	DATA_RDY _MASK	0	R/W		0: Not masked. 1: Masked
1	HD_RST _MASK	0	R/W		0: Not masked. 1: Masked
0	ACK_RX_TO _MASK	0	R/W		0: Not masked. 1: Masked

- **0x45   UFCS_MASK2, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	RX_BUFF _OVERFLOW _MASK	0	R/W		0: Not masked. 1: Masked
6	RX_LENGTH _ERR_MASK	0	R/W		0: Not masked. 1: Masked
5	BAUD_RATE _CHG_MASK	0	R/W		0: Not masked. 1: Masked
4	FRAME_RX _TO_MASK	0	R/W	by REG_RST	0: Not masked. 1: Masked
3	RX_BUFF _BUSY_MASK	0	R/W		0: Not masked. 1: Masked
2	MSG_TRANS _FAIL_MASK	0	R/W		0: Not masked. 1: Masked
1	TRAIN_BYTE _ERR_MASK	0	R/W		0: Not masked. 1: Masked
0	RX_BUFF _OVERFLOW _MASK	0	R/W		0: Not masked. 1: Masked

- **0x46   Duration_Bit, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	DUR_BIT [7]	0	R		
6	DUR_BIT [6]	0	R		
5	DUR_BIT [5]	0	R		
4	DUR_BIT [4]	0	R	PROTOCOL _EN falling edge	LSB: 250ns
3	DUR_BIT [3]	0	R		
2	DUR_BIT [2]	0	R		
1	DUR_BIT [1]	0	R		
0	DUR_BIT [0]	0	R		

- **0x47   TX_LENGTH, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	TX_LENGTH [7]	0	R/W		
6	TX_LENGTH [6]	0	R/W		
5	TX_LENGTH [5]	0	R/W	by REG_RST,	TX data length, except
4	TX_LENGTH [4]	0	R/W	by Watchdog,	training byte and CRC byte
3	TX_LENGTH [3]	0	R/W	by PROTOCOL	LSB: 1
2	TX_LENGTH [2]	0	R/W	_EN falling edge	
1	TX_LENGTH [1]	0	R/W		
0	TX_LENGTH [0]	0	R/W		

- **0x48   TX_ BUFFER0, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	TX_BUFFER0 [7]	0	R/W		
6	TX_BUFFER0 [6]	0	R/W		
5	TX_BUFFER0 [5]	0	R/W	by REG_RST,	
4	TX_BUFFER0 [4]	0	R/W	by Watchdog,	
3	TX_BUFFER0 [3]	0	R/W	by PROTOCOL	
2	TX_BUFFER0 [2]	0	R/W	_EN falling edge	
1	TX_BUFFER0 [1]	0	R/W		
0	TX_BUFFER0 [0]	0	R/W		

- **0x49~0x6A   TX_ BUFFER1~34, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	TX_BUFFERn [7]	0	R/W		
6	TX_BUFFERn [6]	0	R/W		
5	TX_BUFFERn [5]	0	R/W	by REG_RST,	
4	TX_BUFFERn [4]	0	R/W	by Watchdog,	
3	TX_BUFFERn [3]	0	R/W	by PROTOCOL	
2	TX_BUFFERn [2]	0	R/W	_EN falling edge	
1	TX_BUFFERn [1]	0	R/W		
0	TX_BUFFERn [0]	0	R/W		

- **0x6B   TX_ BUFFER35, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	TX_BUFFER35 [7]	0	R/W		
6	TX_BUFFER35 [6]	0	R/W	by REG_RST,	
5	TX_BUFFER35 [5]	0	R/W	by Watchdog,	
4	TX_BUFFER35 [4]	0	R/W	by PROTOCOL	
3	TX_BUFFER35 [3]	0	R/W	_EN falling edge	
2	TX_BUFFER35 [2]	0	R/W		

Bit	Name	Default	Type
1	TX_BUFFER35 [1]	0	R/W
0	TX_BUFFER35 [0]	0	R/W

■ **0x6C   RX_LENGTH, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	RX_LENGTH [7]	0	R		
6	RX_LENGTH [6]	0	R		
5	RX_LENGTH [5]	0	R		
4	RX_LENGTH [4]	0	R		RX data length, except training byte and CRC byte
3	RX_LENGTH [3]	0	R		LSB: 1
2	RX_LENGTH [2]	0	R		
1	RX_LENGTH [1]	0	R		
0	RX_LENGTH [0]	0	R		

■ **0x6D   RX_BUFFER0, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	RX_BUFFER0 [7]	0	R		
6	RX_BUFFER0 [6]	0	R		
5	RX_BUFFER0 [5]	0	R		
4	RX_BUFFER0 [4]	0	R		
3	RX_BUFFER0 [3]	0	R		
2	RX_BUFFER0 [2]	0	R		
1	RX_BUFFER0 [1]	0	R		
0	RX_BUFFER0 [0]	0	R		

■ **0x6E~0xE8   RX_BUFFER1~123, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	RX_BUFFERn [7]	0	R		
6	RX_BUFFERn [6]	0	R		
5	RX_BUFFERn [5]	0	R		
4	RX_BUFFERn [4]	0	R		
3	RX_BUFFERn [3]	0	R		
2	RX_BUFFERn [2]	0	R		
1	RX_BUFFERn [1]	0	R		
0	RX_BUFFERn [0]	0	R		

■ **0xE9   CONTROL4, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	RX_BUFFER124 [7]	0	R		
6	RX_BUFFER124 [6]	0	R		
5	RX_BUFFER124 [5]	0	R		

Bit	Name	Default	Type
4	RX_BUFFER124 [4]	0	R
3	RX_BUFFER124 [3]	0	R
2	RX_BUFFER124 [2]	0	R
1	RX_BUFFER124 [1]	0	R
0	RX_BUFFER124 [0]	0	R

- **0xEC   RX_BUFFER124, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	VBUS_ERR_OPT	0	R/W	by REG_RST	This bit set whether VBUS_ERR check still works after switching starts. 0: VBUS_ERR will be disabled after switching starts. (Only works before switching starts) 1: VBUS_ERR will be always active.
6	RCP_EN	**OTP**	R/W		Reverse Current Protection enable 0: Disable 1: Enable (need OTP to change default)
5	SCP_EN	**OTP**	R/W		Output short circuit protection. 0: Disable 1: Enable (need OTP to change default)
4	VOUT_OVP_EN	0	R/W		Output overvoltage protection. 0: Disable 1: Enable
3	RSNS_OPT	0	R/W		Sense resistor option 0: 5mΩ (default) 1: 2mΩ
2	OVP_GATE_OPT	0	R/W	by REG_RST, by Watchdog	OVP Driver Output Voltage 0: 5V (default) 1: 10V
1	BUMP_DIAG_OPT	**OTP**	R/W	by REG_RST	Bump short diagnostic enable 0: Disable 1: Enable (need OTP to change default)
0	Reserved	0	R/W		

- **0xED   FLT_FLAG4, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	VOUT_SCP FLAG	0	RC		0: VOUT_SCP has not occurred. 1: VOUT_SCP has occurred.
6	RCP FLAG	0	RC		0: RCP has not occurred. 1: RCP has occurred
5	BUMP_SHORT _ FLAG	0	RC		0: BUMP_SHORT is not detected 1: BUMP_SHORT is detected.
4	VOUT_OVP_FLA G	0	RC		0: VOUT_OVP has not occurred. 1: VOUT_OVP has occurred.

3	Reserved	0			
2	Reserved	0			
1	Reserved	0			
0	Reserved	0			

- **0xEE   FLT_INT_MASK4, Default =0x00**

Bit	Name	Default	Type	Reset Type	Description
7	VOUT_SCP_MA SK	0	R/W	by REG_RST	0: VOUT_SCP INT is not masked. 1: VOUT_SCP INT is masked.
6	RCP_MASK	0	R/W		0: RCP INT is not masked. 1: RCP is masked.
5	BUMP_SHORT_ MASK	0	R/W		0: BUMP_SHORT INT is not masked. 1: BUMP_SHORT is masked.
4	VOUT_OVP_MA SK	0	R/W		0: VOUT_OVP INT is not masked. 1: VOUT_OVP INT is masked.
3	Reserved	0			
2	Reserved	0			
1	Reserved	0			
0	Reserved	0			

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Absolute Maximum Ratings[1]

Symbol	Parameters (Items)	Value	Unit
V_{AC}	VAC power input voltage	-0.3 to 40	V
V_{BUS}, V_{PMID}	VBUS, PMID Pins voltage	-0.3 to 22	
V_{CFH1}, V_{CFH2}, V_{CFL1}, V_{CFL2}	CFH1, CFH2, CFL1, CFL2 Pins voltage	-0.3 to 22	
$V_{GATE-VBUS}$	GATE to VBUS voltage	-0.3V to 14	
$V_{BST1-CFH1}$, $V_{BST2-CFH2}$	BST1 to CFH1, BST2 to CFH2 voltage	-0.3V to 6	
$V_{PMID-CFH1}$, $V_{PMID-CFH2}$	PMID to CFH1, CFH2 voltage	-0.3V to 6	
$V_{CFH1-VOUT}$, $V_{CFH2-VOUT}$	CFH1, CFH2 to VOUT voltage	-0.3V to 6	
V_{CFL1}, V_{CFL2}, V_{OUT}, V_{BATP}, V_{BATN}, V_{REGN}, V_{DP}, V_{DM}	CFL1, CFL2, VOUT, BATP, BATN, REGN, DP, DM Pins voltage	-0.3V to 6	
V_{SRN}, V_{SRP}	SRN, SRP Pins voltage	-0.3V to 1.8	
$V_{SRP-SRN}$	SRP to SRN voltage	-0.5V to 0.5	
$V_{CONTROL}$	SDA, SCL Pins Voltage	-0.3 to 6	
V_{INT}	$\overline{INT}$ Pin Voltage	-0.3 to 6	
P_D	Maximum Power Consumption, T_A=25°C	**TBD**	mW
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, T_A=25°C	**TBD**	°C/W
T_J[2]	Operating Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-65 to 150	
T_{SOLD}	Lead Temperature (Soldering, 10 sec)	260	
V_{ESD}	HBM	±2000	V
	CDM	±250	

Note (1): Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): This device series incorporates ESD protection and is tested by the following methods:

HBM tested per EIA/JESD22-A114
CDM tested per EIA/JESD22-C101

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Recommended Operating Conditions

Symbol	Parameters	Rating	Unit
V$_{VAC}$	Supply Input Voltage	3.3 to 18	V
V$_{VBUS}$	VBUS Input Voltage	3.3 to 12	
V$_{VOUT}$	Output Voltage	3 to 5.5	
V$_{CFH1-VOUT}$, V$_{CFL1}$, V$_{CFH2-VOUT}$, V$_{CFL2}$	CFH1 to VOUT Voltage, CFL1 Voltage CFH2 to VOUT Voltage, CFL2 Voltage	0 to 5.5	
V$_{BST1-CFH1}$, V$_{BST2-CFH2}$	BST1 to CFH1, BST2 to CFH2 Voltage	0 to 5.5	
V$_{BATP}$, V$_{BATN}$	BATP, BATN Input Voltage	0 to 5.5	
V$_{SRP-SRN}$	SRP to SRN Voltage	-0.03 to 0.03	
V$_{SRN}$	SRN Voltage	-0.1 to 1.8	
V$_{SDA}$, V$_{SCL}$, V$_{INT}$	SDA, SCL, INT Voltage	0 to 5.5	
V$_{DM}$, V$_{DP}$	SDA, SCL, INT Voltage	0 to 5.5	
T$_J$	Operating Junction Temperature	-40 to 125	ºC
T$_A$	Operating Ambient Temperature	-40 to 85	
C$_{VAC}$	Effective Input Ceramic Capacitor Value	10	uF
C$_{VBUS}$	Effective Input Ceramic Capacitor Value	1	
C$_{PMID}$	Effective Input Ceramic Capacitor Value	10	
C$_{FLY1}$	Effective switch Capacitor Value	2*22	
C$_{FLY2}$	Effective switch Capacitor Value	2*22	
C$_{VOUT}$	Effective Output Ceramic Capacitor Value	10	
C$_{BST1}$/C$_{BST2}$	Effective BST Ceramic Capacitor Value	100	nF
C$_{REGN}$	Effective LDO Output Ceramic Capacitor Value	4.7	uF
R$_{SNS}$	Sense resistance value	5 or 2	mΩ
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

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Electrical Characteristics

(Unless otherwise noted, -40ºC≤T_J≤85ºC, typical values are at T_A = 25ºC, with respect to GND)

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
INTERNAL THRESHOLD							
V_{AC_UVLO}	VAC Under-voltage Lockout	VAC Rising		2.2	2.23	2.262	V
$V_{AC\_UVLO\_HYS}$		Falling Hysteresis			200		mV
V_{AC_PRES}	VAC Present	VAC_PRES Rising			3.224		V
$V_{AC\_PRES\_HYS}$		Falling Hysteresis			100		mV
V_{BUS_PRES}	VBUS Present	VBUS_PRES Rising			3.094		V
$V_{BUS\_PRES\_HYS}$		Falling Hysteresis			100		mV
V_{BAT_PRES}	VBAT Present	VBAT Rising			2.838		V
$V_{BAT\_PRES\_HYS}$		Falling Hysteresis			120		mV
SUPPLY CURRENT							
I_{Q_AC}	VAC Quiescent Current	V_{AC_OVP} Hiz, V_{AC}=12V, V_{BUS}=0V			944		μA
I_{Q_BAT}	VBAT Quiescent Current	No VBUS, V_{BAT}=4.2V	ADC Disabled		7		
			ADC Enabled		833		
RESISTANCES							
R_{QRB_ON}	Reverse Block-FET On resistance				9.6		mΩ
R_{QCH1_ON}	On resistance of QCH1				17.8		
R_{QDH1_ON}	On resistance of QDH1				9.8		
R_{QCL1_ON}	On resistance of QCL1				15.6		
R_{QDL1_ON}	On resistance of QDL1				11.3		
R_{QCH2_ON}	On resistance of QCH2				17.8		
R_{QDH2_ON}	On resistance of QDH2				9.8		
R_{QCL2_ON}	On resistance of QCL2				15.6		
R_{QDL2_ON}	On resistance of QDL2				11.3		
VAC OVER-VOLTAGE PROTECTION							
$V_{OVPGATE}$	OVPGATE Voltage	REGEC Bit [2] =0			10		V
		REGEC Bit [2] =1		4.7	5.0	5.3	V
V_{VAC_OVP}	VAC OVP Range			4		19	V
	VAC OVP Accuracy	VAC_OVP =12V		2		2	%
t_{VAC_OVP}	VAC OVP Response Time	Qg = 20nC				200	ns
V_{VAC_OK}	VAC OVP Immunity Time	From VAC_PRES to turn on the OVP FET			20		ms

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Electrical Characteristics (Continued)

(Unless otherwise noted, -40ºC≤T_J≤85ºC, typical values are at T_A = 25ºC, with respect to GND)

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
PROTECTION							
V_{VBUS_OVP}	VBUS OVP Range			4		14	V
	VBUS OVP Accuracy			-2		2	%
V_{VBAT_OVP}	VBAT OVP Range			4		5	V
	VBAT OVP Accuracy	T_A = 0~85°C		-0.5		0.5	%
V_{VOUT_OVP}	VOUT OVP			4.94	4.96	4.99	V
I_{IBUS_OCP}	IBUS OCP Range	SC Mode		0.5		3.6	A
		Bypass Mode		2.5		5.6	
	IBUS OCP Accuracy	2A		-5		5	%
I_{IBUS_UCP}	IBUS UCP Rising Threshold	REG07, Bit6=1			484		mA
		REG07, Bit6=0			276		
	IBUS UCP Falling Threshold	REG07, Bit6=1			214		
		REG07, Bit6=0			109		
I_{IBAT_OCP}	IBAT OCP Range			2		8.3	A
	IBAT OCP Accuracy	2A		-5		5	%
V_{VDROP_OVP}	VDROP OVP	REG05h=02		143	150	169	mV
		REG05h=04		238	250	280	
		REG05h=06		335	350	393	
t_{DIE}	TDIE Over Temperature Threshold				150		°C
VBUS IN-RANGE-CHECK							
$V_{VBUS\_Err\_HI\_TH}$	VBUS Error High Voltage Rising Threshold	0.5*VIN: VOUT in SC mode; VIN: VOUT in Bypass mode	REG02 [1:0] =00		1.122		Rate
			REG02 [1:0] =01		1.173		
			REG02 [1:0] =10		1.224		
			REG02 [1:0] =11		1.275		
$V_{VBUS\_Err\_LW\_TH}$	VBUS Error Low Voltage Falling Threshold		REG02 [3:2] =00		0.997		
			REG02 [3:2] =01		1.017		
			REG02 [3:2] =10		1.027		
			REG02 [3:2] =11		1.038		
PULL DOWN							
R_{VAC_PD}	VAC Pull-down Resistor				128		Ω
R_{VBUS_PD}	VBUS Pull-down Resistor				0.9		kΩ
REGN LDO							
V_{OUT_REG}	REGN LDO Output Voltage			3.139	3.273	3.322	V
I_{OUT_REG}	REGN LDO Output Current Limit			30			mA

Electrical Characteristics (Continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
TIMING SPECIFICATIONS						
V$_{VAC\_Present}$	VAC Present Deglitch Time	From VAC_PRES to generate the flag		30		ms
V$_{VBUS\_Present}$	VBUS Present Deglitch Time	From VBUS present to generate the flag		1		
V$_{VBAT\_Present}$	VBAT Present Deglitch Time	From VBAT present to generate the flag		17		us
t$_{VBUS\_OVP}$	VBUS OVP Response Time				200	ns
t$_{VBAT\_OVP}$	VBAT OVP Response Time	VBAT not in regulation			1	µs
		VBAT in regulation			500	
t$_{IBAT\_OCP}$	IBAT OCP Deglitch Time	IBAT not in regulation			50	
		IBAT in regulation			500	
t$_{VOUT\_OVP}$	VOUT OVP Response Time			1	2	
t$_{IBUS\_UCP-F}$	IBUS_UCP Falling Deglitch Time	REGEC Bit7=0			20	
		REGEC Bit7=1		5		ms
t$_{IBUS\_UCP-R}$	IBUS_UCP Rising Deglitch Time			1		
t$_{IBUS\_OCP}$	IBUS_OCP Deglitch Time				50	µs
t$_{VDROP\_OVP}$	VDROP_OVP Deglitch Time	REG05 Bit4=0		10		
t$_{Soft\_start}$	Soft-start Timer				100	s
t$_{CMP\_SLEEP}$	CMP_SLEEP Deglitch Time	CMP rising enter Sleep Mode (no deglitch)			1	us
		CMP falling exit Sleep Mode			10	ms
t$_{VBUS\_In-range\_R}$	VBUS In-range Check Entry Deglitch Time			10		µs
t$_{VBUS\_In-range\_F}$	VBUS In-range Check Exit Deglitch Time			500		
t$_{INT\_DOWN}$	INT Pull-down Duration			256		
t$_{VAC\_DOWN}$	VAC Pull-down Duration			400		ms
t$_{WD}$	Watchdog Timer		0.5		80	s
	Watchdog Timer Accuracy		-5		5	%
FREQUENCY						
Fsw	Switched Frequency Range		200		1500	kHz
	Switched Frequency Accuracy		-10.5		4.4	%

Electrical Characteristics (Continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
ADC						
BITE	Effective Resolution			12		bits
t_{ADC_CON}	Conversion Time Each Measurement			3		ms
$I_{IBUS\_ADC\_RAG}$	IBUS ADC Measurement Range		0		8.19	A
$I_{IBUS\_ADC\_LSB}$	IBUS ADC LSB			2		mA
$I_{IBUS\_ADC\_ACCUR}$	IBUS ADC Measurement Accuracy	$I_{BUS}=2A$, $T_J=0{\sim}85°C$	-5		5	%
$V_{VBUS\_ADC\_RAG}$	VBUS ADC Measurement Range		0		16.38	V
$V_{VBUS\_ADC\_LSB}$	VBUS ADC LSB			4		mV
$V_{VBUS\_ADC\_ACCUR}$	VBUS ADC Measurement Accuracy		-2		2	%
$V_{VBAT\_ADC\_RAG}$	VBAT ADC Measurement Range		0		8.19	V
$V_{VBAT\_ADC\_LSB}$	VBAT ADC LSB			2		mV
$V_{VBAT\_ADC\_ACCUR}$	VBAT ADC Measurement Accuracy	$V_{BAT} = 4.3V$, $T_J = 0{\sim}85°C$	-0.50		0.50	%
$I_{IBAT\_ADC\_RAG}$	IBAT ADC Measurement Range		0		8.19	A
$I_{IBAT\_ADC\_LSB}$	IBAT ADC LSB			2		mA
$I_{IBAT\_ADC\_ACCUR}$	IBAT ADC Measurement Accuracy	$I_{BAT} = 4A$, $R_{SNS} = 5m\Omega$, $T_J=0{\sim}85°C$	-5		5	%
$TDIE_{ADC\_RAG}$	TDIE ADC Measurement Range		-40		150	°C
$TDIE_{ADC\_LSB}$	TDIE ADC LSB			1		°C
$TDIE_{ADC\_ACCUR}$	TDIE ADC Measurement Accuracy		-3		3	°C
I²C Interface (SDA, SCL)						
F_{I2C}	I²C Frequency	may not be 1MHz I²C compliant		400	1000	kHz
V_{IH}	Input High Threshold		1.3			V
V_{IL}	Input Low Threshold				0.455	V
V_{OL}	SDA Output Low Threshold				0.4	V
D+/D- LEVELS (UFCS)						
V_{ILD+}	Input Low Threshold		0.3		0.99	V
V_{IHD+}	Input High Threshold		2.31	3.3	3.6	V
V_{OLD-}	Output Low Voltage	D- = 2mA			0.4	V
V_{OHD-}	Output High Voltage	D- = 2mA	1.44	3.3	3.6	V

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Electrical Characteristics (Continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
UFCS TIMING SPECIFICATION						
$t_{DM\_H\_Duration1}$	DM High Voltage Time of Duration1		1.5	2	2.5	ms
$t_{DM\_H\_Duration2}$	DM Low Voltage Time of Duration2		6	8	10	
$t_{DM\_H\_Duration3}$	DM High Voltage Time of Duration3		1.5	2	2.5	
$t_{DM\_H\_Duration4}$	DM Low Voltage Time of Duration4		6	8	10	
t_{DP_DET}	DP Detection Timer		11		15	
$t_{DP\_DET\_RETRY}$	DP Detection Retry Time		0		10	
t_{UFCS_Delay}	UFCS Mode Delay Time				100	
t_{SEND}	Send Ping Time of Duration				1	
Baud Rate	Baud Rate Option			115200		bps
				57600		
				38400		
	Accuracy of Baud Rate in Transmitter		-10		10	%
	Accuracy of Baud Rate in Transmitter in Data Packet		-1		1	
	Tolerance of Baud Rate in Receiver		-15		15	
t_{TIMER}	Data Frame Receiving Timer		500		700	µs
t_{ACK_REC}	ACK Receiving Window				10	ms
t_{ACK_RES}	ACK Respond Delay		100		1000	µs
t_{MES_RES}	Message Resending Window				500	
t_{MES_REC}	Message Receiving Window				50	ms
$t_{MES\_RES\_DELAY}$	Message Respond Delay				40	
t_{PAT}	Power Adjust Time				550	
t_{CABLE_ACCEPT}	Cable Identification Information Acceptance Window				1200	
$t_{POWERED\_STOP}$	Powered Device Stops Communicating				1100	
t_{CABLE_ACCEPT}	Cable Accepts Information Window				1000	ms

Application Circuits
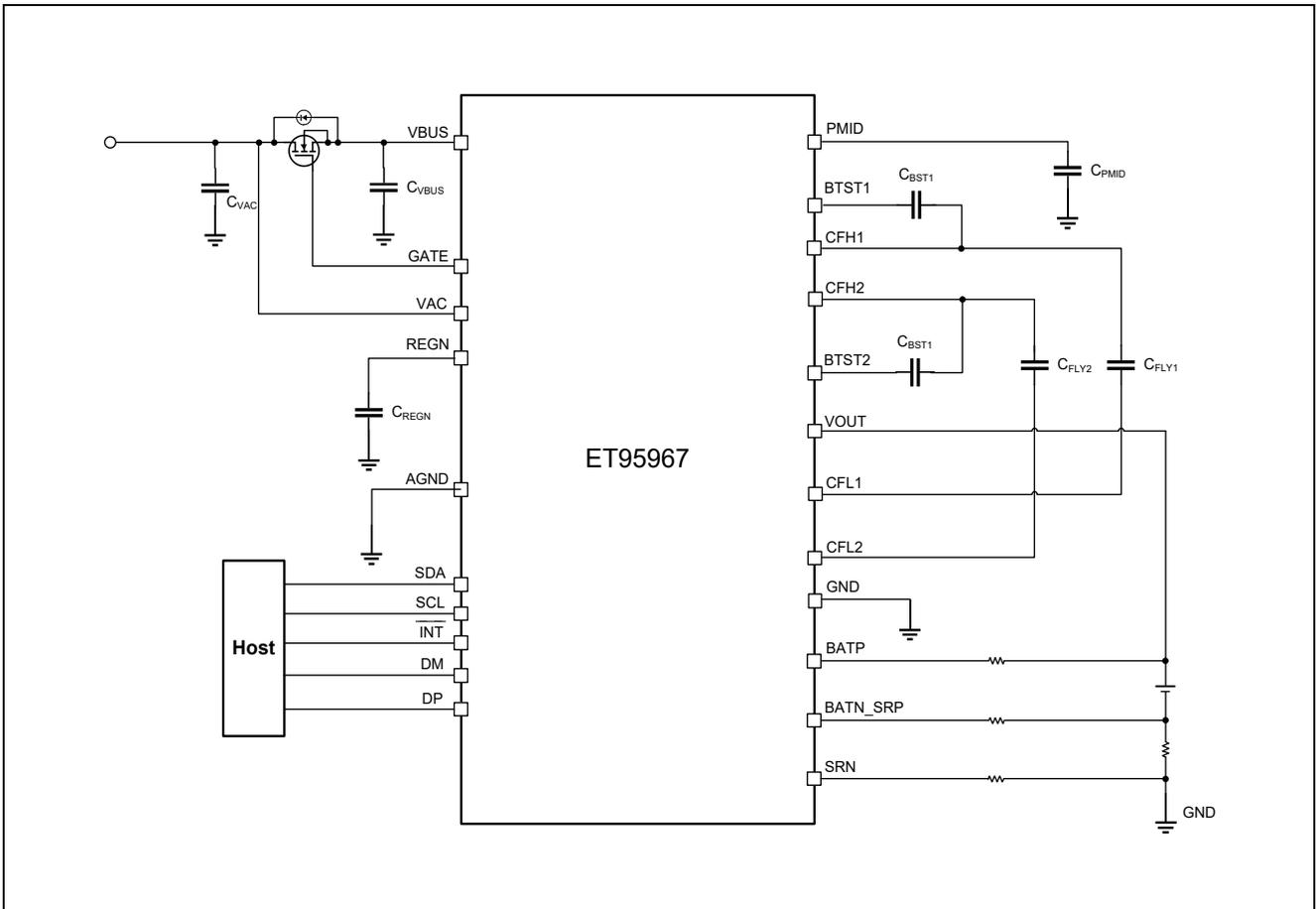
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Package Dimension

BOTTOM VIEW

SIDE VIEW

Unit: mm
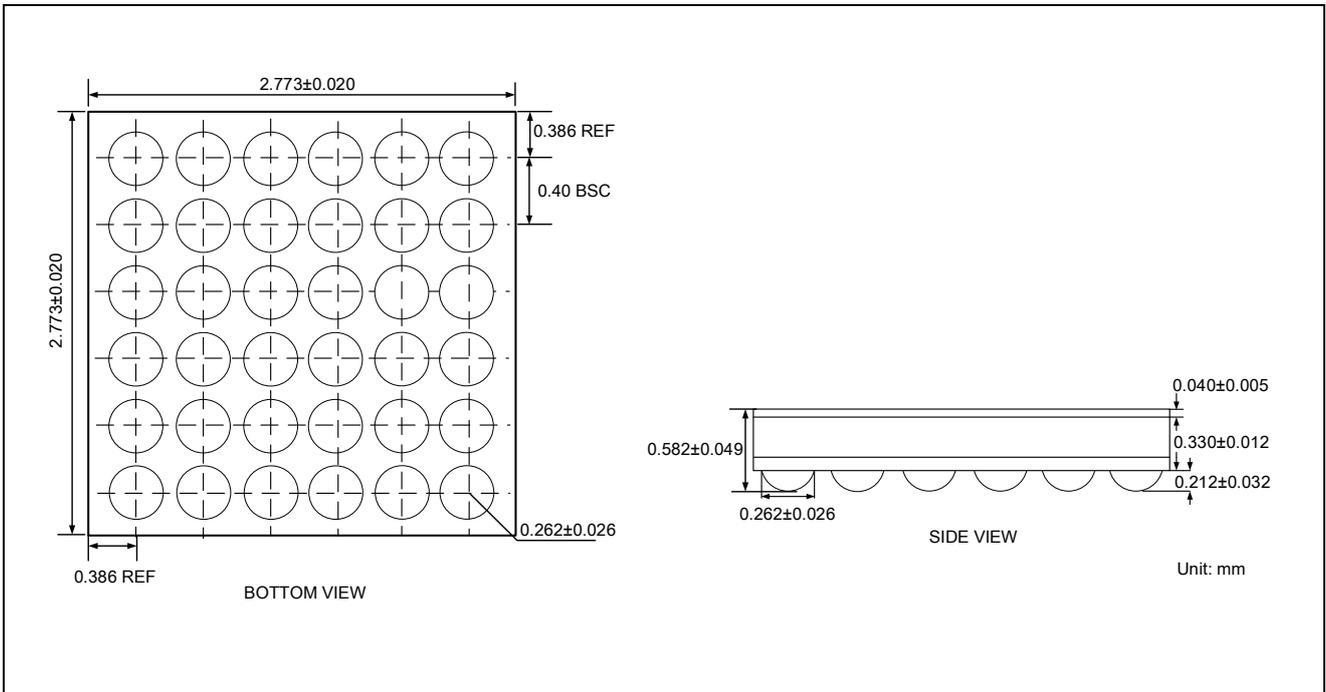
Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2024-08-26	Version 1.0	Yang Xiao Xu	Yang Xiao Xu	Yang Xiao Xu