Integration of 7 Audio Equalizer 16CH RGB LED Constant Current Drive Circuit

General Description

ET6298 is a constant current LED driver circuit with 256 steps linear current control function. Built-in 16 independent low-resistance color LED driver channels, can adjust each channel's current. Through code selection, each channel can provide four current range: 5mA, 10mA, 20mA, 40mA. ET6298 integrate 7 band audio equalizer, subdivide 20Hz~20KHz input audio signal into 7 frequencies by built-in band-pass filters, and through the built-in high resolution ADC converts the average amplitude of each frequency value into corresponding data, control 7 output current channels. In audio synchronization mode, MCU needn't any data operation, only need to set up the corresponding instruction, LED brightness will change along with the music beats.

ET6298 also have half fade function, in this mode, MCU just completed the brightness and darkest time cycle control and send single instruction to set fade direction (fade-in or fade-out), ET6298 will automatically complete fade-in or fade-out cycle control, this will greatly reduce the hardware and software overhead.

Features

- Operate supply voltage：2.4V to 5.5V
- 256 steps linear current adjust
- Provide four current range: 5mA, 10mA, 20mA, 40mA (Default 20mA)
- Use common anode LED
- I^2C BUS interface, can read and write
- Any channel's current can be adjust alone
- Half fade function, send single instruction to set fade direction
- Built-in low voltage reset function
- Built-in 7 band audio equalizers
- Built-in LED brightness will change along with the music beats
- -24~+18dB input audio signal gain adjustment
- Operate temperature range: T_A=-40 to 85°C
- Package: QFN24(4mm × 4mm)

Application

- Mobile Phones
- Smart home applications
- Toy

Pin Configuration

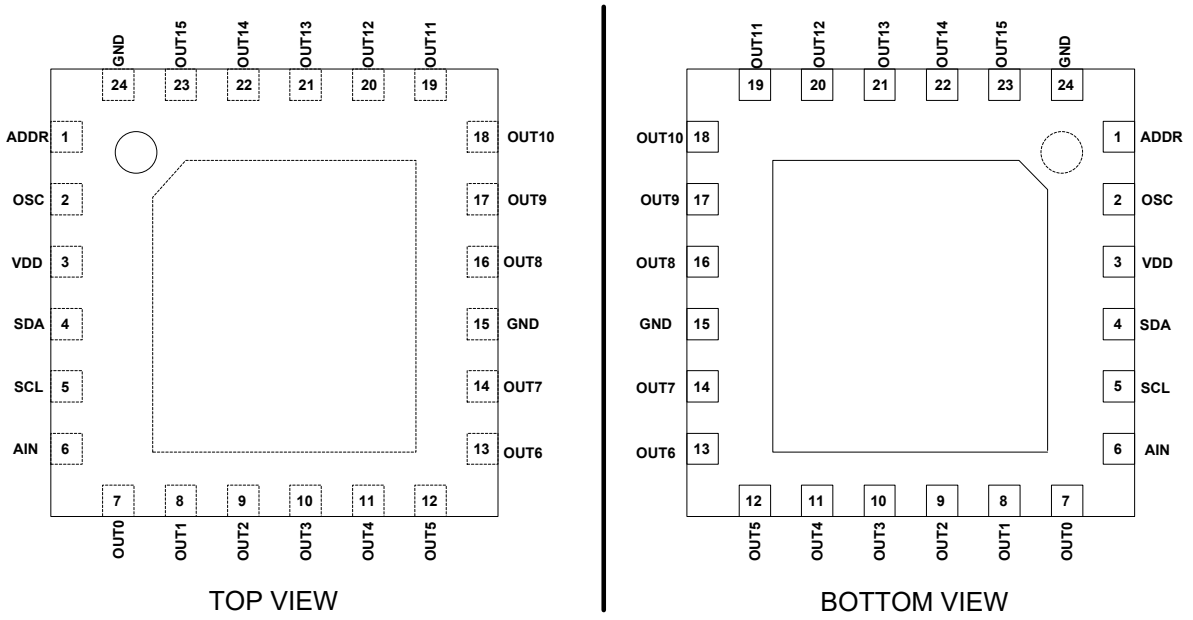


Figure 1. Pin Configuration (QFN24)

Pin Function

Pin No.	Name	Description
1	ADDR	I²C BUS Address Selection.
2	OSC	Oscillation Input, Need a external resistor and a external capacitor to determine frequency.
3	VDD	Supply Voltage.
4	SDA	I²C BUS Data I/O.
5	SCL	I²C BUS Clock Input.
6	AIN	Audio Signal Input.
7~14, 16~23	OUT0~OUT7,OUT8~OUT15	LED Constant Current Output.
15,24	GND	GND.

Block Diagram

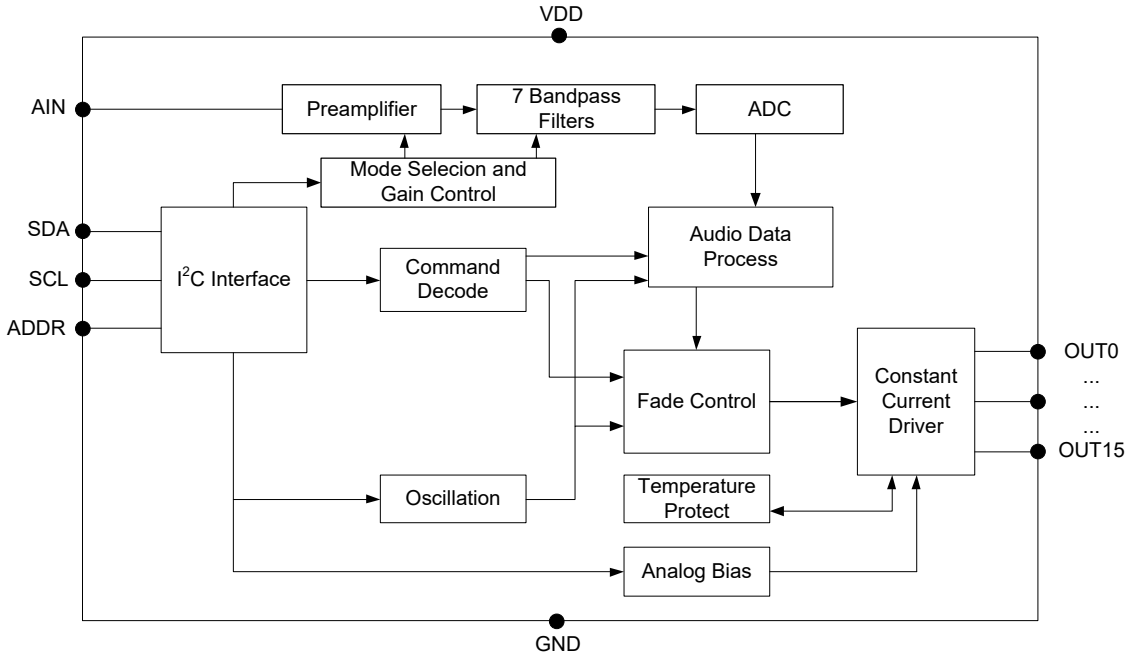


Figure 2. Block Diagram

Function Description

1. RC Selection for OSC

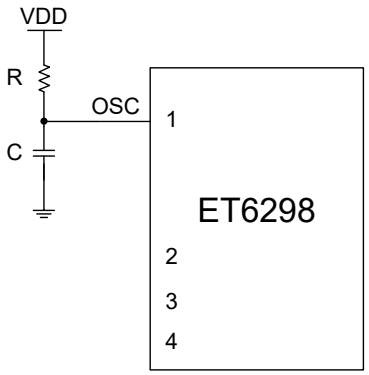


Figure 3. RC Selection for OSC

OSC Frequency	Supply Voltage（V）	Resistor（kΩ）	Capacitor（pf）
2.5MHz	5.0	18	33
	4.2	16	33
	3.3	15	33

2.I²C BUS

BUS Interface

MCU can transmit data with ET6298 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

While SCL signal is high, SDA’s data is effective and stable. While SCL signal is low, MCU can change SDA port’s voltage to high or low.

Start(Restart) and Stop operate condition

While SCL signal is high, SDA signal change from high to low, the interface start or restart; while SCL signal is high, and SDA signal change from low to high ,the interface will stop operating.

Byte Format

Each byte of data has 8 bits, and each byte include a ACK. Transfer the first bit data is MSB.

ACK

During the ACK clock, the MCU make the SDA port at a high level, and in the write mode, ET6298 will send ACK signal and make the SDA port at a low level during the response. In the reading mode, ET6298 will not send the ACK signal and make the SDA port in a high level during the response.

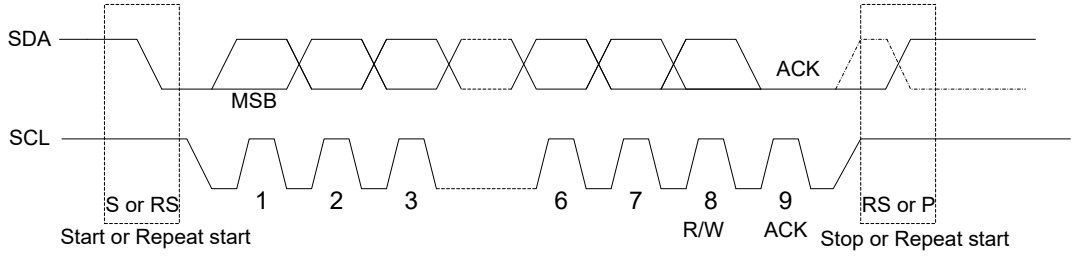


Figure 4. I²C Write mode

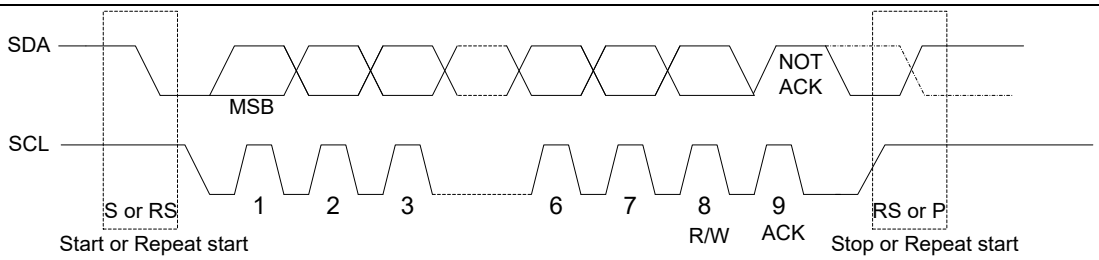


Figure 5. I²C Read mode

- ACK=Acknowledge
- MSB=Most Significant Bit
- S=Start Conditions RS=Restart Conditions P=Stop Conditions
- Fastest Transmission Speed =400KBITS/S
- Restart: SDA-level turnover as expressed by the dashed line waveform

Chip Address

ET6298 has four Chip address

ADDR port connect to the pin	Chip Address
VDD	6EH/6FH(Write/Read)
GND	66H/67H(Write/Read)
SCL	6AH/6BH(Write/Read)
SDA	6CH/6DH(Write/Read)

I²C BUS Protocol

I²C Writing Command Register Interface Protocol (Single):

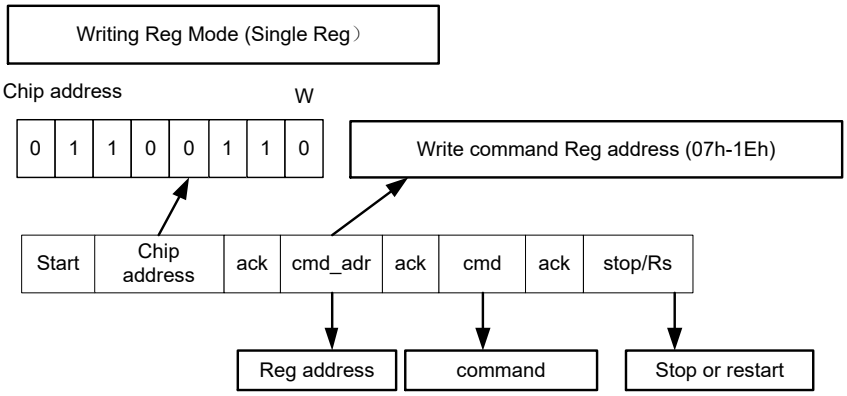


Figure 6. I²C Writing Register Mode(single)

- Start=Start Conditions
- Chip address=Write register chip address =0110011+0(w)b
- ack=Acknowledge
- cmd_adr= (1bit single mode 0b+2bits Don’t care bits xx +5bits command reg address)
- ack=Acknowledge
- command =cmd=Register Data
- ack=Acknowledge
- Stop/Rs=Condition/Restart Condition

Writing Command Register Interface Protocol (continuous)：

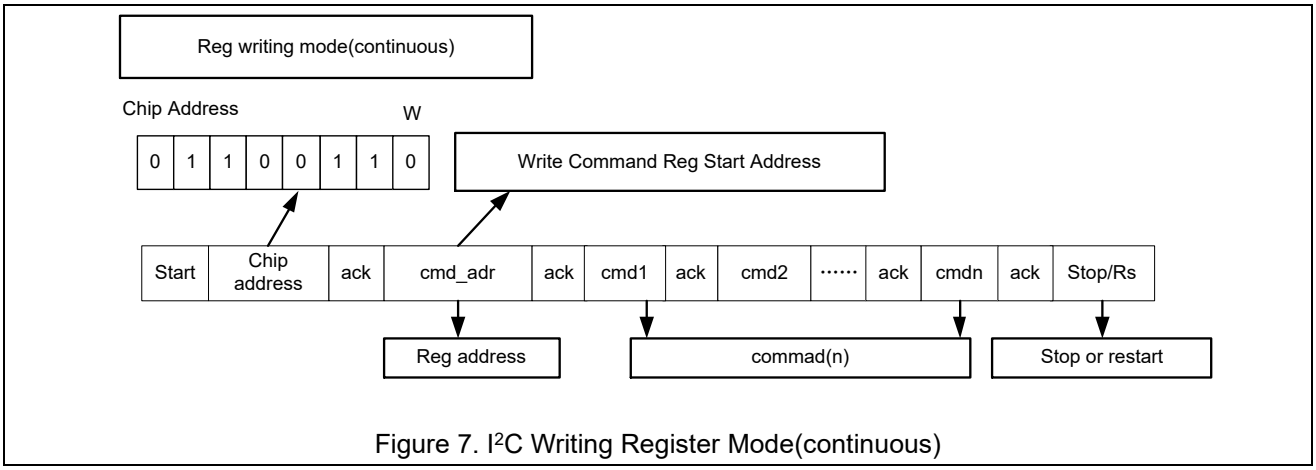


Figure 7. I²C Writing Register Mode(continuous)

- Start=Start Conditions
- Chip address=Write register chip address =0110011+0(w)b
- ack=Acknowledge
- **Reg address =cmd_adr=(1bit continuous mode 1b +2bit Don’t’ care xx +5bits command reg start address)**
- ack=Acknowledge
- Command reg data1=cmd1
- ack=Acknowledge
- ……
- Command reg data n=cmdn
- ack=Acknowledge
- Stop/Rs=Condition/Restart Condition

Reading Command Register Interface Protocol:

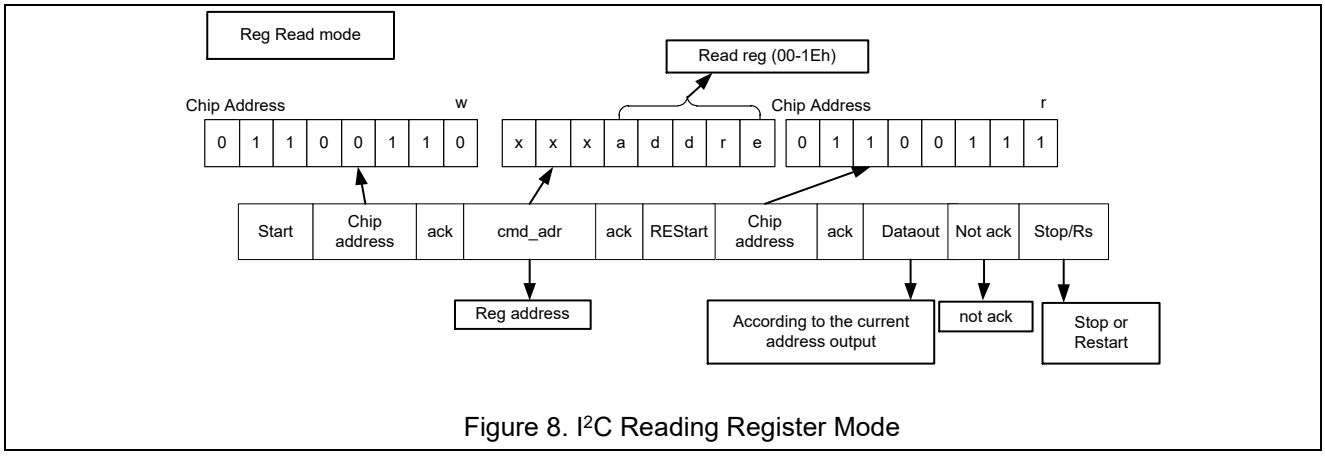


Figure 8. I²C Reading Register Mode

- Start =Start Conditions
- Chip address=Write register chip address =0110011+0(w)b
- ack=Acknowledge
- cmd_adr= (1bits single mode 0b+2bits Don’t care bits xx +5bits command reg address)
- ack=Acknowledge

- REStart=Restart Conditions
- Chip address=Read register chip address =0110011+1(r)b
- ack=Acknowledge
- Dataout=Register Data Output
- Not ack= No Acknowledge(1b)
- Stop/Rs=Condition/Restart Condition

3. Register Definition

Table 1. ADC conversion result Registers

Addr: 00h-06h			Adc_one,Adc_two…Adc_seven Register		
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**
00h	7:0	adc_one	00h	R	63Hz audio data ADC conversion result
01h	7:0	adc_two	00h	R	160Hz audio data ADC conversion result
02h	7:0	adc_three	00h	R	400Hz audio data ADC conversion result
03h	7:0	adc_four	00h	R	1KHz audio data ADC conversion result
04h	7:0	adc_five	00h	R	2.5KHz audio data ADC conversion result
05h	7:0	adc_six	00h	R	6.25KHz audio data ADC conversion result
06h	7:0	adc_seven	00h	R	12KHz audio data ADC conversion result

Table 2. Display Control Registers

Addr: 07h		Display Control Register			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2:0	gc	000b	R/W	Pre-amplifier gain setting	
				000	0db
				001	6db
				010	12db
				011	18db
				100	-6db
				101	-12db
				110	-18db
				111	-24db
3	x	x	x	Don’t Care	
5:4	curtmd	10b	R/W	Maximum linear current I_{max}	
				00	5mA
				01	10mA
				10	20mA
				11	40mA
6	disp_con	0b	R/W	0	Display Close
				1	Display Open
7	shutdown	1b	R/W	0	Normal work
				1	Shutdown

Table 3. Mode Selection Register 1

Addr: 08h		Mode Select Register 1			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	mdsel_chal0	0b	R/W	0	Channel 0 is work in linear current adjust or half fade mode
				1	Channel 0 work in audio mode（63Hz）
1	mdsel_chal1	0b	R/W	0	Channel 1 is work in linear current adjust or half fade mode
				1	Channel 1 work in audio mode（160Hz）
2	mdsel_chal2	0b	R/W	0	Channel 2 is work in linear current adjust or half fade mode
				1	Channel 2 work in audio mode（400Hz）
3	mdsel_chal3	0b	R/W	0	Channel 3 is work in linear current adjust or half fade mode
				1	Channel 3 work in audio mode（1KHz）
4	mdsel_chal4	0b	R/W	0	Channel 4 is work in linear current adjust or half fade mode
				1	Channel 4 work in audio mode（2.5KHz）
5	mdsel_chal5	0b	R/W	0	Channel 5 is work in linear current adjust or half fade mode
				1	Channel 5 work in audio mode（6.25KHz）
6	mdsel_chal6	0b	R/W	0	Channel 6 is work in linear current adjust or half fade mode
				1	Channel 6 work in audio mode（12KHz）
7	adcwork_sel	0b	R/W	0	ADC Disable(mdsel_chalx=0, x=0~13)
				1	ADC enable

Table 4. Mode Selection Register 2

Addr: 09h		Mode Select Register 2			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	mdsel_chal7	0b	R/W	0	Channel 7 is work in linear current adjust or half fade mode
				1	Channel 7 work in audio mode（63Hz）
1	mdsel_chal8	0b	R/W	0	Channel 8 is work in linear current adjust or half fade mode
				1	Channel 8 work in audio mode（160Hz）
2	mdsel_chal9	0b	R/W	0	Channel 9 is work in linear current adjust or half fade mode
				1	Channel 9 work in audio mode（400Hz）
3	mdsel_chal10	0b	R/W	0	Channel 10 is work in linear current adjust or half fade mode
				1	Channel 10 work in audio mode（1KHz）

4	mdsel_chal11	0b	R/W	0	Channel 11 is work in linear current adjust or half fade mode
				1	Channel 11 work in audio mode（2.5KHz）
5	mdsel_chal12	0b	R/W	0	Channel 12 is work in linear current adjust or half fade mode
				1	Channel 12 work in audio mode（6.25KHz）
6	mdsel_chal13	0b	R/W	0	Channel 13 is work in linear current adjust or half fade mode
				1	Channel 13 work in audio mode（12KHz）
7	x	x	x	x	Don't Care

Notes:

(1) {(|mdsel_chalx),adcwork_sel}, |mdsel_chalx→(mdsel_chal0 | mdsel_chal1|⋯| mdsel_chal13)=00, each channel data is from Linear Current Regulating Registers (I^2C control) or half fade mode(internal counter control)；

(2) {(|mdsel_chalx),adcwork_sel}, |mdsel_chalx→(mdsel_chal0 | mdsel_chal1|⋯| mdsel_chal13)=10/11, each channel data is from the ADC, namely LED breath according to music frequency；

(3) {(|mdsel_chalx),adcwork_sel}, |mdsel_chalx→(mdsel_chal0 | mdsel_chal1|⋯| mdsel_chal13)=01, The user can read the current ADC data(00~06H register) through I^2C, and each channel data is from Linear Current Regulating Registers (I^2C control) or half fade mode(internal counter control).

(4) if use the audio mode, recommend V_{DD}≥3.3V

Table 5. Bias Register 1

Addr: 0Ah		**Mode Select Register**			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	bias_one	40H	R/W	Music mode gradually dark trailing low brightness threshold value	
				00H	threshold value is 00H（All LED light）
				…	……
				40H	Low brightness range of 00H to 40H

Notes：

(1) Bias_one minimum value is greater than 20H, it can ensure that LED lights are not lighting in the case of no music state.

(2) Bias_one according to real-time volume to write the right values, to ensure that the LED lights gorgeous respiratory effects under different volume.

Table 6. Bias Register 2

Addr: 0Bh		Mode Select Register			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	bias_two	7FH	R/W	Music mode gradually dark trailing high brightness threshold value	
				7FH	High brightness range of 7FH to FFH
				…	……..
				FFH	High brightness range of FFH to FFH

Note： bias_two is larger than bias_one

Table 7. Brightness Jump Rank Set Register

Addr: 0Ch		Brightness Jump Rank Set Register			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:6	brit_jump_rank_hr	11b	R/W	Diminishing high brightness dimming level for audio mode	
				00	The fading for decreasing level is 3H
				01	The fading for decreasing level is 7H
				10	The fading for decreasing level is BH
				11	The fading for decreasing level is FH
5:3	brit_jump_rank_m	100b	R/W	Diminishing middle brightness dimming level for audio mode	
				000	The fading for decreasing level is 0H
				…	……
				111	The fading for decreasing level is 7H
2:0	brit_jump_rank_l	100b	R/W	Diminishing low brightness dimming level for audio mode	
				000	The fading for decreasing level is 0H
				…	……
				111	The fading for decreasing level is 7H

Notes：

(1) brit_jump_rank_h is the actual high brightness level for diminishing,and brit_jump_rank_h= { brit_jump_rank_hr, 2'b11}，namely, brit_jump_rank_hr=11b，then brit_jump_rank_h=1111b=FH

(2) Figure 9 is the audio synchronization breath rendering diagram, and the parameter shown as the figure is set by these registers.

In BIAS_TWO diminishing FFH interval value to use brit_jump_rank_h, maximum value is FH;

In BIAS_ONE diminishing BIAS_TWO interval value to use brit_jump_rank_m, maximum is 7H;

In 00 h to diminishing BIAS_ONE interval value brit_jump_rank_l, maximum is 7H

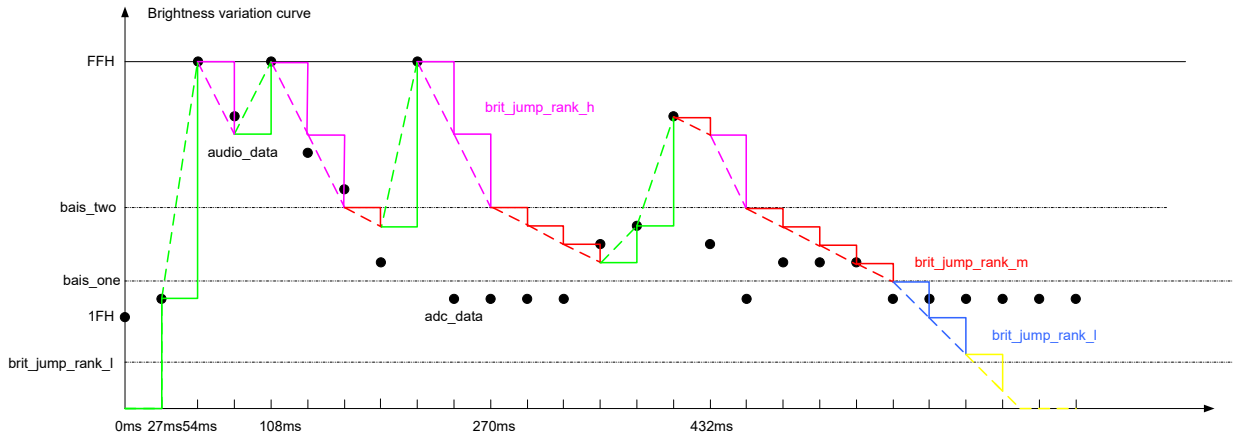


Figure 9. Audio synchronization breath rendering

Table 8. Linear Current Regulating Registers

Addr: 0Dh-1CH		Linear Current Modulation Register			
Addr	**Register Name**	**Default**	**Access**	**Description**	
0DH	curt_step_chal0	00h	R/W	0 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	…… …
				FFh	255/255I_{max}
0EH	curt_step_chal1	00h	R/W	1 Channel Current Value	
				00H	0
				01h	1/255I_{max}
				…	…… …
				FFH	255/255I_{max}
0FH	curt_step_chal2	00h	R/W	2 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	…… …
				FFh	255/255I_{max}
10H	curt_step_chal3	00h	R/W	3 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	…… …
				FFh	255/255I_{max}

11H	curt_step_chal4	00h	R/W	4 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	……
				FFh	255/255I_{max}
12H	curt_step_chal5	00h	R/W	5 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	……
				FFh	255/255I_{max}
13H	curt_step_chal6	00h	R/W	6 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	……
				FFh	255/255I_{max}
14H	curt_step_chal7	00h	R/W	7 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	……
				FFh	255/255I_{max}
15H	curt_step_chal8	00h	R/W	8 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	……
				FFh	255/255I_{max}
16H	curt_step_chal9	00h	R/W	9 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	……
				FFh	255/255I_{max}
17H	curt_step_chal10	00h	R/W	10 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	……
				FFh	255/255I_{max}

18H	curt_step_chal11	00h	R/W	11 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	……
				FFh	255/255 I_{max}
19H	curt_step_chal12	00h	R/W	12 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	……
				FFh	255/255I_{max}
1AH	curt_step_chal13	00h	R/W	13 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	……
				FFh	255/255I_{max}
1BH	curt_step_chal14	00h	R/W	14 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	……
				FFh	255/255I_{max}
1CH	curt_step_chal15	00h	R/W	15 Channel Current Value	
				00h	0
				01h	1/255I_{max}
				…	……
				FFh	255/255I_{max}

Note： I_{max} is shown as Table 2

Table 9. Semi-Autonomous Breath Parameters Register

Addr: 1Dh		**Half-Independent Breath Parameter Register**			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2:0	breath_rise	000b	R/W	Fade-in cycle	
				000b	0.1s
				001b	0.2s
				010b	0.4s
				011b	0.8s
				100b	1.6s
				101b	3.3s

				110b	6.5s
				111b	13.1s
4:3	xx	xx	xx	Don't Care	
7:5	breath_fall	000b	R/W	Fade-out cycle	
				000b	0.1s
				001b	0.2s
				010b	0.4s
				011b	0.8s
				100b	1.6s
				101b	3.3s
				110b	6.5s
				111b	13.1s

Note： For example, breath_rise=000b, breath_fall=001b, breath_dir =0/1b, fade-in and fade-out is shown as figure 10.

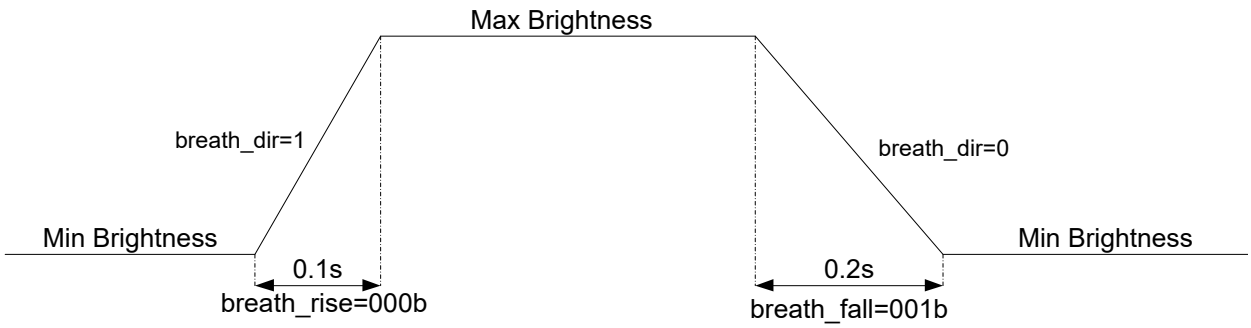


Figure 10. Fade-in and Fade-out Cycle

Table 10 Semi-Autonomous Breath Control Register

Addr: 1Eh		Half-Independent Breath Control Register			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	breath_dir	0b	R/W	Fade-in and Fade-out Direction Control	
				0b	From the brightest faded to the dark
				1b	From the dark faded to the brightest
3:1	x	xxx	x	Don't Care	
4	bre_con_7	0b	R/W	Semi-auto Breath Mode Select for 0-6 channel	
				0b	Audio Synchronization or Linear Current Regulation
				1b	Semi-auto Breath Mode
5	bre_con_3l	0b	R/W	Semi-auto Breath Mode Select for 7-9 channel	
				0b	Audio Synchronization or Linear Current Regulation
				1b	Semi-auto Breath Mode

6	bre_con_3m	0b	R/W	Semi-auto Breath Mode Select for 10-12 channel	
				0b	Audio Synchronization or Linear Current Regulation
				1b	Semi-auto Breath Mode
7	bre_con_3h	0b	R/W	Semi-auto Breath Mode Select for 13-15 channel	
				0b	Audio Synchronization or Linear Current Regulation
				1b	Semi-auto Breath Mode

Absolute Maximum Ratings

Characteristic	Symbol	Range	Unit
Supply Voltage	V_{DD}	6.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Storage Temperature	T_{STG}	-65~150	°C
Junction Temperature	T_J	-40~150	°C
Operating Temperature	T_A	-40~85	°C

Electrical Characteristic (Unless otherwise specified, V_{DD}=5V, T_A=-40~85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	-	2.4	5	5.5	V
Supply Current	I_{DD1}	ADC Work, Max liner current bit=10b	3	5	7	mA
Supply Current	I_{DD2}	ADC don't work, Max liner current bit=10b	1.5	3	4.5	mA
Shutdown Current	I_{SD}	-			5	uA
Output Current	I_{OUT5mA}	Max liner current bit=00b V_{DD}=5V, T_A=25°C@V_{DS}=1V	4.5	5	5.5	mA
	$I_{OUT10mA}$	Max liner current bit=01b V_{DD}=5V, T_A=25°C@V_{DS}=1V	9	10	11	mA
	$I_{OUT20mA}$	Max liner current bit=10b V_{DD}=5V, T_A=25°C@V_{DS}=1V	18	20	22	mA
	$I_{OUT40mA}$	Max liner current bit=11b V_{DD}=5V, T_A=25°C@V_{DS}=1V	36	40	44	mA
Output channels current matching	I_{SINK}	Max liner current bit=10， All CurrentData=FFh,	-9		9	%
Output Dropout Voltage	V_{DPO}	Max liner current bit=11b All CurrentData=FFh, (V_{DD}=5V, T_A=25°C 90% Of current@V_{DS}=1V)		250	450	mV
Low Voltage Reset	V_{LVRF}	T_A=25°C	1.5	1.8	2.1	V
	V_{LVRR}	T_A=25°C	1.6	1.9	2.2	V

Input Low Voltage	$V_{IN(0)}$	-			0.3	V
Input High Voltage	$V_{IN(1)}$	-	1.6			V
Input Low Current	$I_{IN(0)}$	-		5	200	nA
Input High Current	$I_{IN(1)}$	-		5	200	nA

I²C Mode Timing Parameter

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCL}	SCL Clock Frequency	0	-	400	KHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	1.3	-	-	μs
$t_{HD:STA}$	Hold Time(Repeated) START Condition	0.6	-	-	μs
t_{LOW}	Low Period of SCL Clock	1.3	-	-	μs
t_{HIGH}	HIGH Period of SCL Cloc	0.6	-	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	0.6	-	-	μs
$t_{HD:DAT}$	Data Hold Time	-	-	0.9	μs
$t_{SU:DAT}$	Data Setup Time	100	-	-	ns
t_R	Data Hold Time2	20+0.1Cb(1)	-	300	ns
t_F	Data Hold Time2	20+0.1Cb(1)	-	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	0.6	-	-	μs

Note1: Cb=total capacitance of one bus line in PF.

I²C Mode Timing

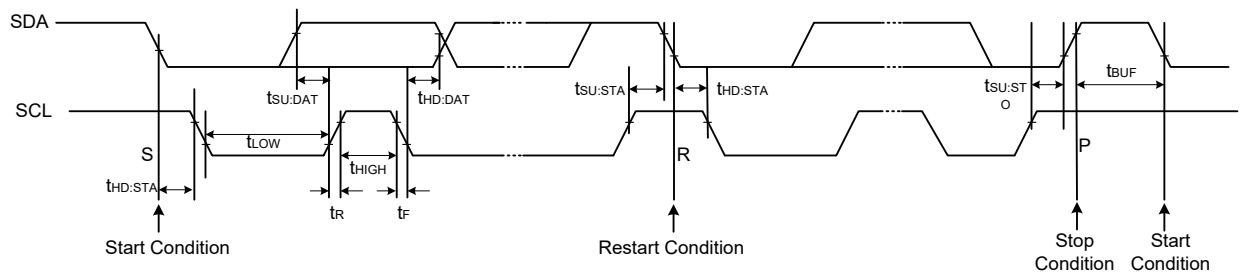


Figure 11.

Typical Application Diagram

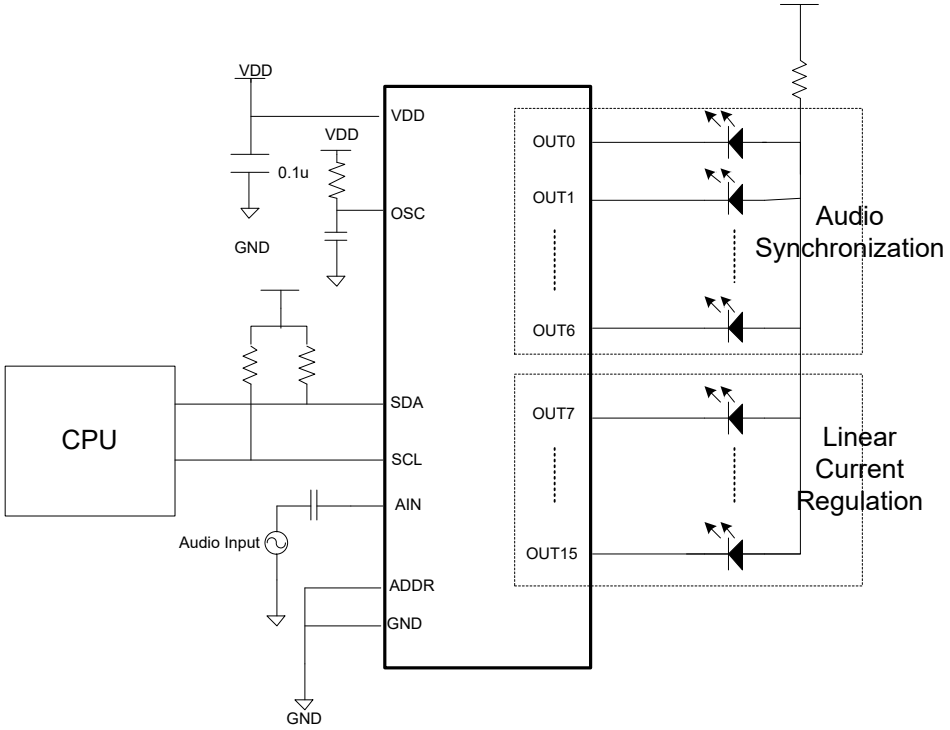


Figure 12. Typical application Diagram 1 (7 Audio Synchronization + Linear Current Regulation)

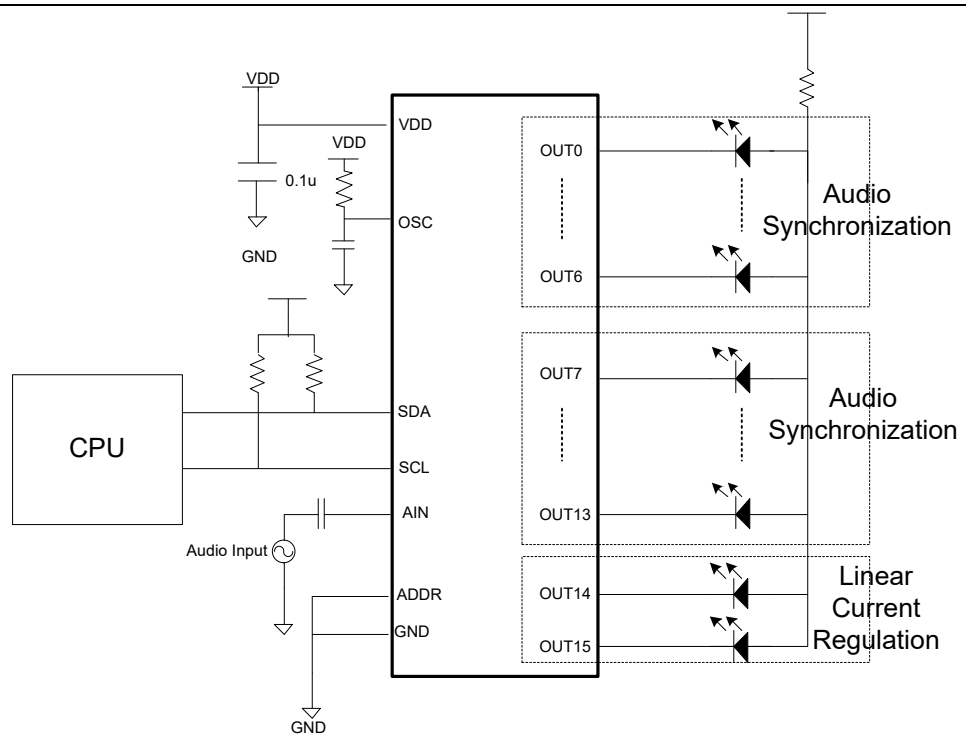


Figure 13. Typical application Diagram 2 (14 audio synchronization + linear current regulation)

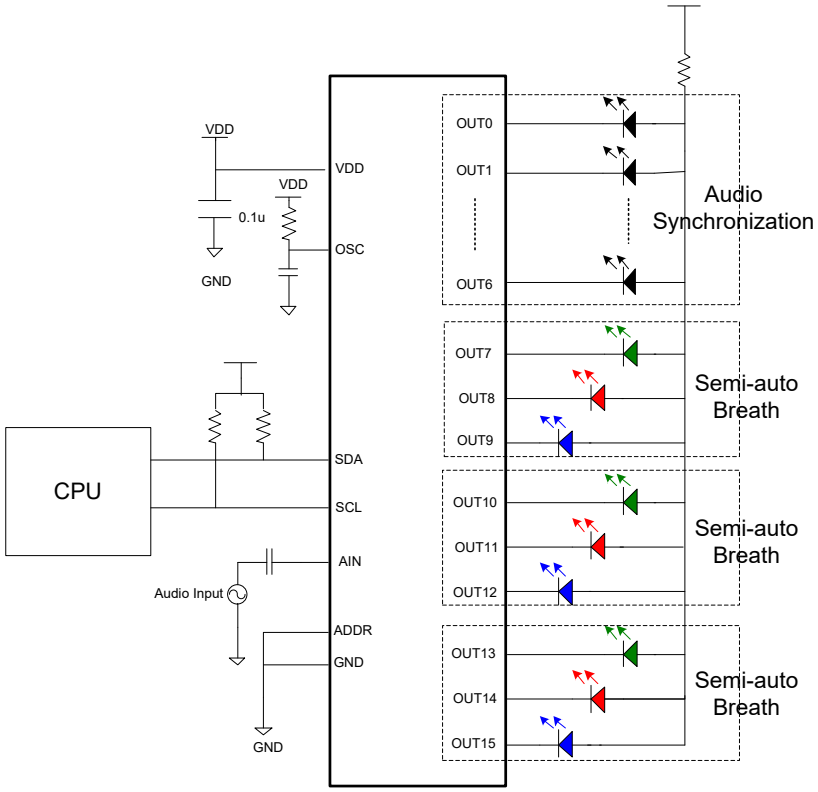


Figure 14. Typical application Diagram 3 (7 Audio Synchronization +Semi-auto Breath)

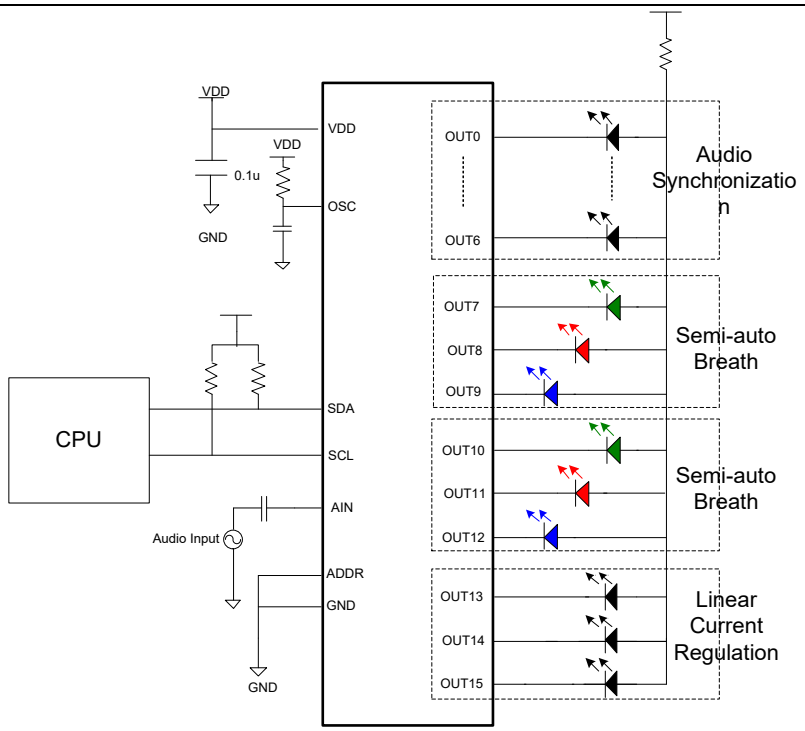
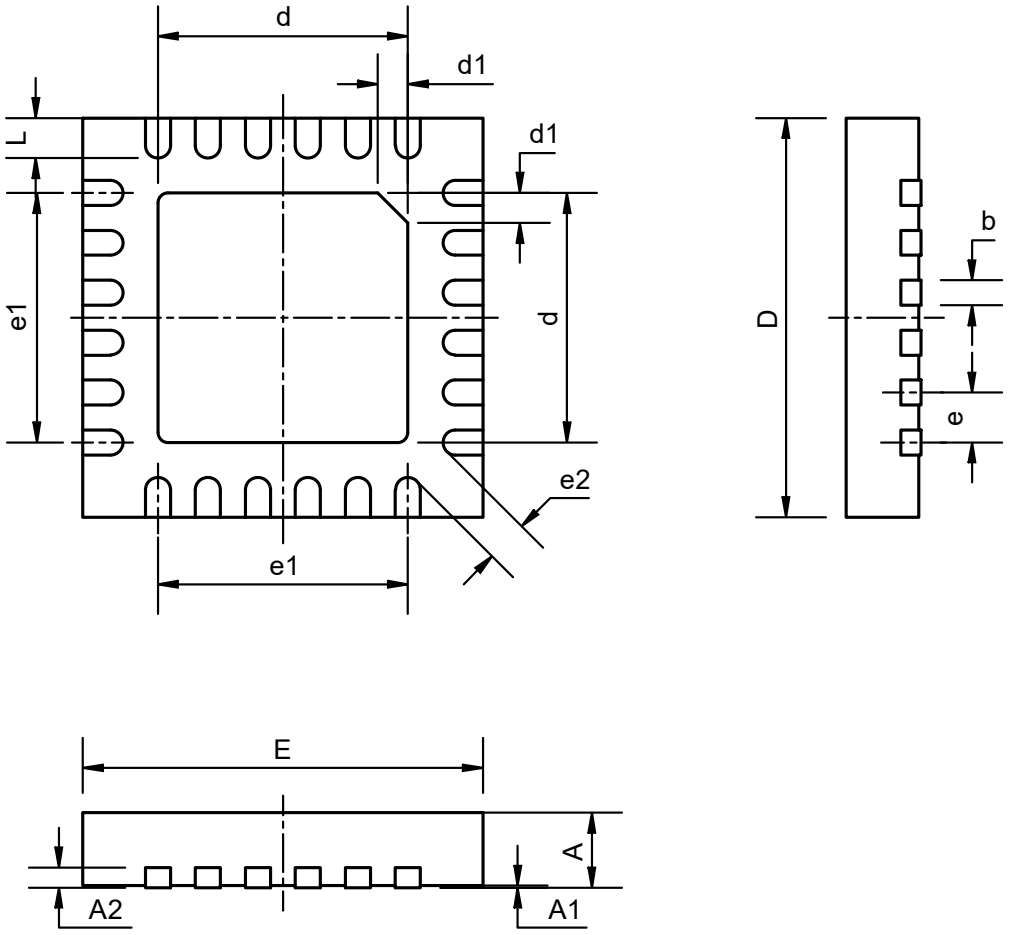


Figure 15. Typical application Diagram 4 (Mixed mode)

*：Above circuit is only for reference.

Package

QFN24



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.18	0.20	0.25
b	0.18	0.25	0.30
D	3.90	4.00	4.10
d	2.40	2.60	2.80
d1	0.30	0.35	0.40
E	3.90	4.00	4.10
e		0.50	
e1	2.40	2.60	2.80
e2	0.40	0.45	0.50
L	0.35	0.40	0.45