ET6220 - Dot Matrix LED Driver

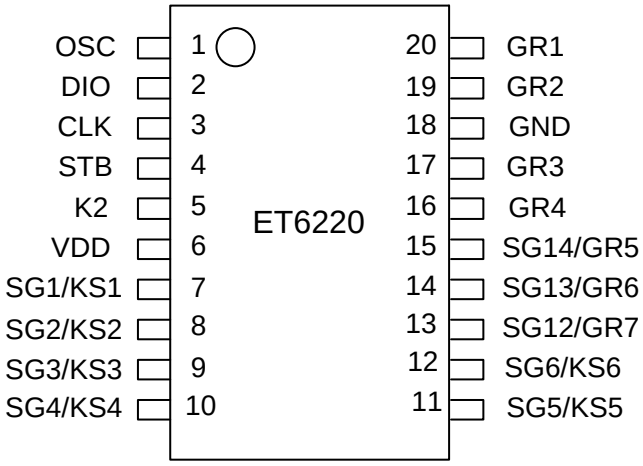
General Description

ET6220 is a high reliability matrix LED driver IC with 6 segments output (SEG), 4 commons output (GRID), 3 segments/commons output (SEG/GRID), display memory, control circuit, key scan circuit , using 3-line serial interface communication.

Features

- High performance CMOS process, low power consumption
- Display Mode: 6 Segs × 7 Grids ~ 9 Segs × 4 Grids ,Max support 42 LED matrix
- Keyboard scanning: 1 × 6 matrix
- Dimming adjustment: 8 step
- 3-Line serial interface
- Package: TSSOP20

Pin Assignments

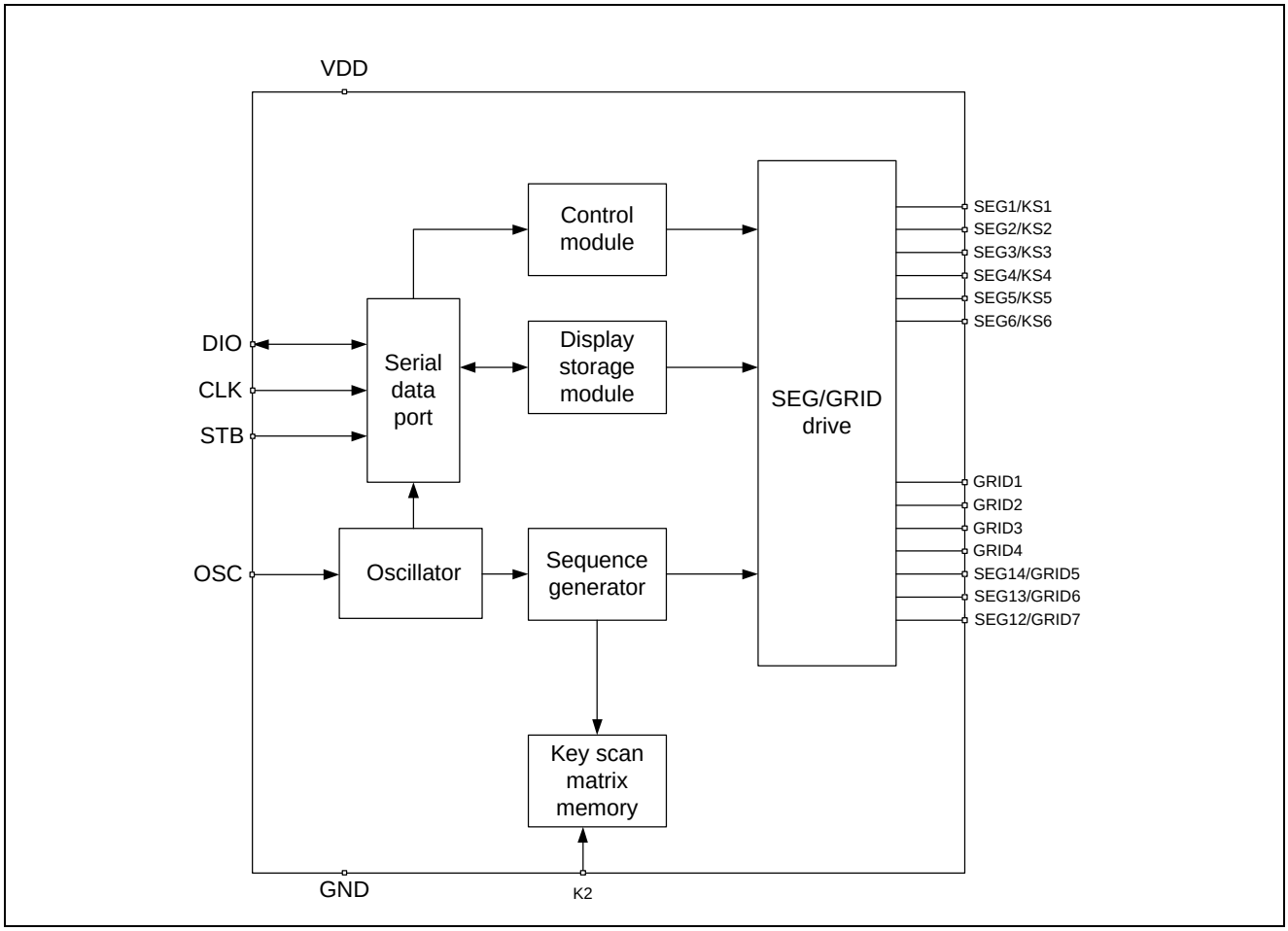


Top View

Pin. Function

Pin No.	Symbol	I/O	Description
1	OSC	-	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency
2	DIO	I/O	Serial data input/output port. (open-drain output structure)
3	CLK	I	Serial clock input port.
4	STB	I	Serial data strobe port.
5	K2	I	Key data input port.
6	VDD	—	power Input
7～12	SG1/KS6～SG7/KS6	O	Segment output port (Connected LED positive pole)/Key scan output
13～15	SG12/GR7～SG14/GR5	O	Segment/Grid output port, select segment or grid output through registers.
18	GND	—	Ground
16，17，19，20	GR4～GR1	O	Grid output port, Connected LED negative pole

Function Diagram



Functions Description

Command

After the STB port status changes from high to low, input command bytes through the DIO port.If the STB port is set to high for some reason while the data or command is being transmitted, the serial communication is initialized and the data/command being entered is considered invalid.

Command 1: display mode setting command

The display mode setting command determines the number of segments (4~7 grids, 9~6 segments) used.A display command must be executed to continue the display.If the same mode is selected, the command is not executed.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B1	Function	Description
0	0	NC, Set to 0 please				0	0	Display segment and grid setting	9 Segs×4 Grids
0	0					0	1		8 Segs×5 Grids
0	0					1	0		7 Segs×6 Grids
0	0					1	1		6 Segs×7 Grids

Command2：Data Command Setting

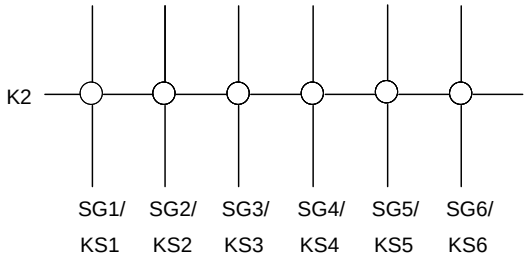
Data setup commands perform write display data or read keys.When the power supply is powered on, bits 4 to 1 (B3 to B0) should be set to 0.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
0	1	NC, Set to 0 please		0				Mode setting	Normal mode
				1					Test mode
					0			Address mode	Automatic address increase
					1				Fixed address
						0	0	Data write/read	Display data input mode
						1	0		Read Key Data

Key scan matrix

The key scan matrix is composed of 1×6 array：



Key scan data storage RAM

The input data is stored as follows: the READ command is used to READ from the highest bit.

	B0	B1	B2	B3	B4	B5	B6	B7	READING SEQUENCE
BYTE1	×	SG1/KS1	×	×	SG2/KS2	×			↓
BYTE2	×	SG3/KS3	×	×	SG4/KS4	×			
BYTE3	×	SG5/KS5	×	×	SG6/KS6	×			
		K2			K2				

Note： B0、B2、B3、B5～B7 undefined.

Command3：Display Address Setting

The address setting command is used to set the display memory address.If the address ranges from 00H to 0DH, the address is valid.If the address is 0EH or higher, the data is invalid unless the correct address is set again.When the power supply is powered on, the address is 00H.

MSB **LSB**

B7	B6	B5	B4	B3	B2	B1	B0	Description
1	1	NC, fill in 0		0	0	0	0	Display address 00H
1	1			0	0	0	1	Display address 01H
1	1			0	0	1	0	Display address 02H
1	1			0	0	1	1	Display address 03H
1	1			0	1	0	0	Display address 04H
1	1			0	1	0	1	Display address 05H
1	1			0	1	1	0	Display address 06H
1	1			0	1	1	1	Display address 07H
1	1			1	0	0	0	Display address 08H
1	1			1	0	0	1	Display address 09H
1	1			1	0	1	0	Display address 0AH
1	1			1	0	1	1	Display address 0BH
1	1			1	1	0	0	Display address 0CH
1	1			1	1	0	1	Display address 0DH

Address assignment：

SG1……SG4	SG5…SG6	SG12	SG13…SG14	Matrix Address
$00H_L$	$00H_U$	$01H_L$	$01H_U$	GR1
$02H_L$	$02H_U$	$03H_L$	$03H_U$	GR2
$04H_L$	$04H_U$	$05H_L$	$05H_U$	GR3
$06H_L$	$06H_U$	$07H_L$	$07H_U$	GR4
$08H_L$	$08H_U$	$09H_L$	$09H_U$	GR5
$0AH_L$	$0AH_U$	$0BH_L$	$0BH_U$	GR6
$0CH_L$	$0CH_U$	$0DH_L$	$0DH_U$	GR7

B0	B1	B2	B3	B4	B5	B6	B7
××H_L				××H_U			
Low 4bits				High 4bits			

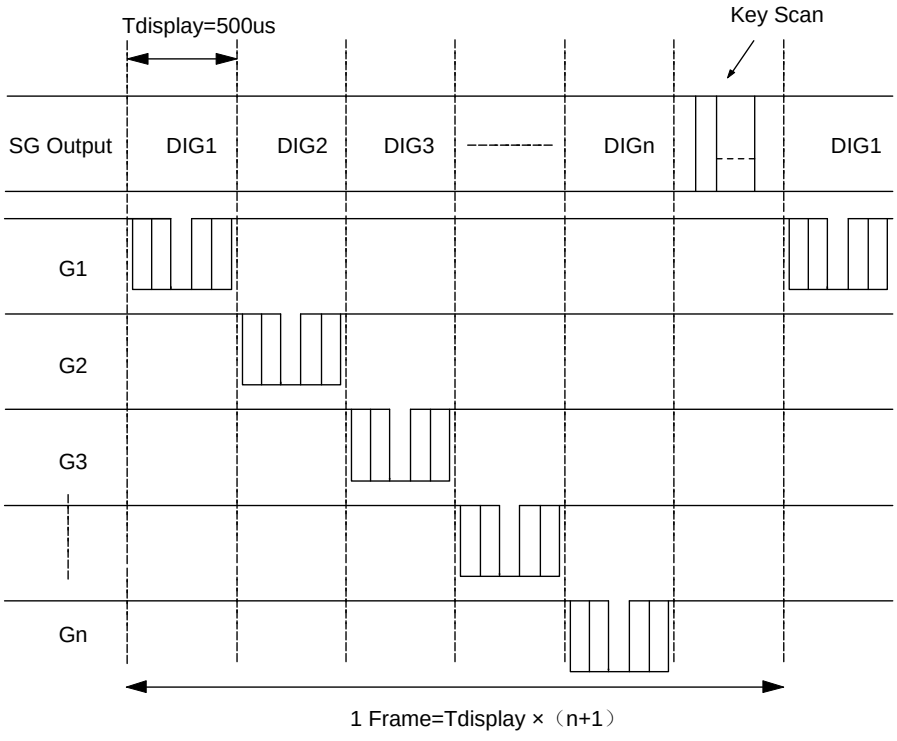
Command4：Display Control Setting

MSB **LSB**

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
1	0	NC, fill in 0			0	0	0	Display duty cycle setting	Duty cycle is 1/16
1	0				0	0	1		Duty cycle is 2/16
1	0				0	1	0		Duty cycle is 4/16
1	0				0	1	1		Duty cycle is 10/16
1	0				1	0	0		Duty cycle is 11/16
1	0				1	0	1		Duty cycle is 12/16
1	0				1	1	0		Duty cycle is 13/16
1	0				1	1	1		Duty cycle is 14/16
1	0			0				Display ON / OFF setting	Display OFF
1	0			1					Display ON

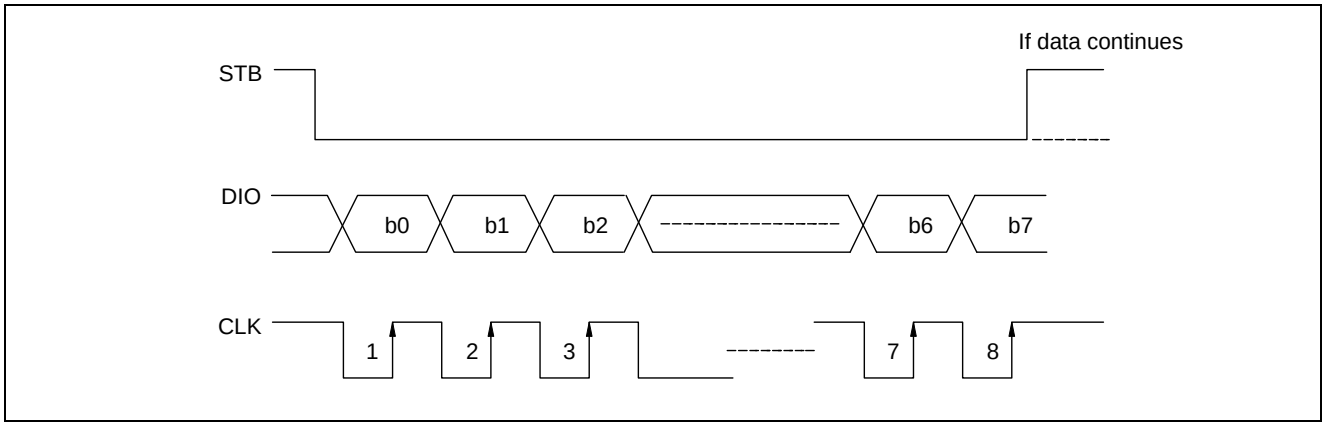
Scan and display timing

Key scan and display sequence diagram as shown below.A cycle of key scanning consists of 2 frames.The data of the 6 x 1 matrix is stored in RAM.

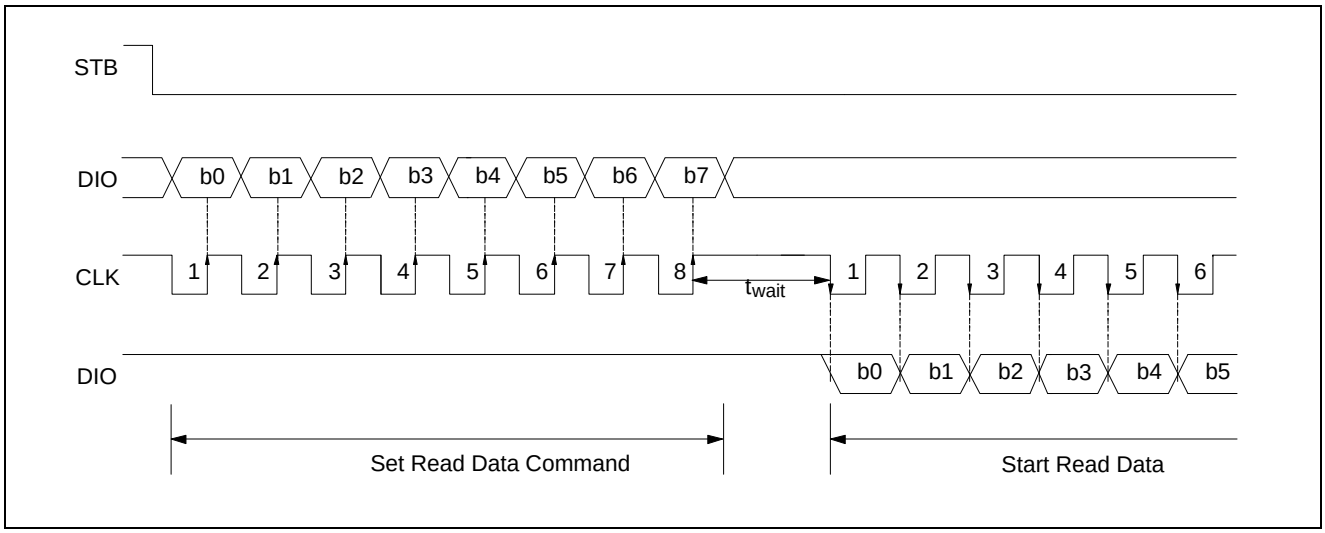


Serial Communication Format

The following figure shows the serial communication format of ET6220. It is recommended to connect a pull-up resistor (1K ~ 10K) to the DIO port.



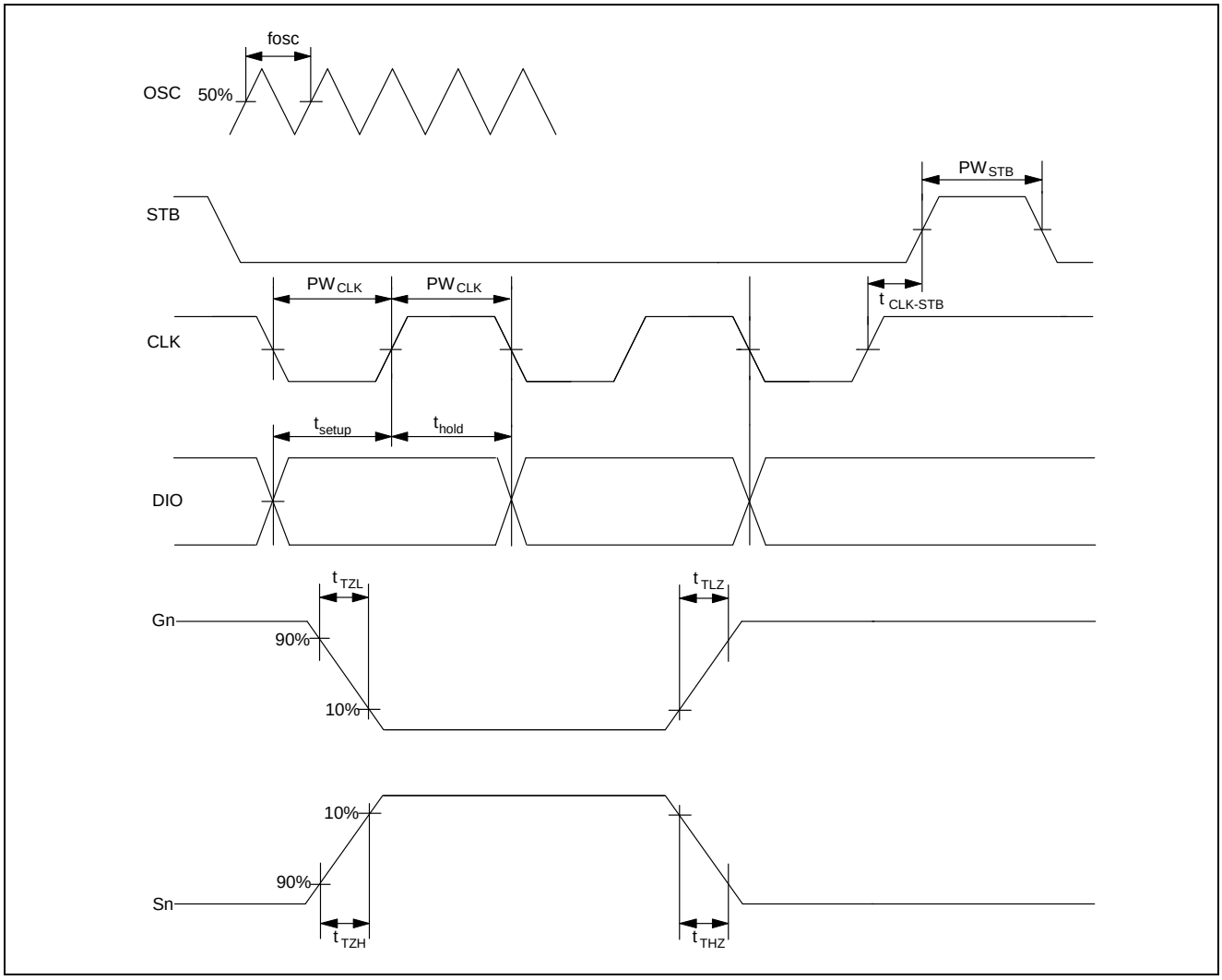
Data transmission（Data read）



Note: T_{wait}（waiting time）≥1μs.

It should be noted that when reading data, the rising edge is the eighth clock of the instruction to the falling edge of the first clock of the subsequent data reading must be longer than or equal to 1us waiting time(T_{wait}).

Conversion Characteristic Waveform



Transformation Characteristic

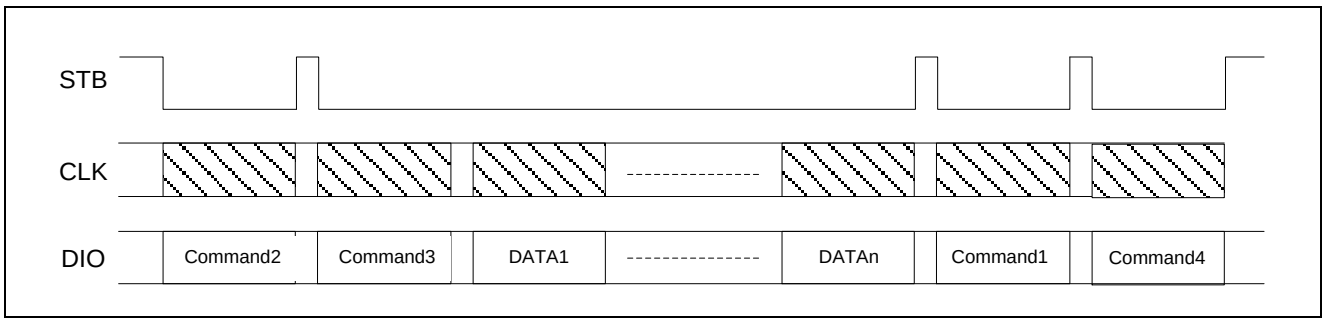
Symbol	Descripiton	Range	Units
PW_{CLK}	CLK pulse width	≥400	ns
PW_{STB}	STB pulse width	≥1	us
t_{setup}	Data setup time	≥100	ns
t_{hold}	Date hold time	≥100	ns
$t_{CLK-STB}$	CLK-STB time	≥1	us
t_{THZ}	Falling time	≤10	us
t_{TZH}	Rising time	≤1	us
t_{TZL}		<1	us
t_{TLZ}		<10	us

Note: The test conditions are as follows:

t_{THZ} (pull-down resistance = 10kΩ, loading capacitance =300pF), t_{TLZ} (pull-up resistance = 10kΩ, loading capacitance =300pF)

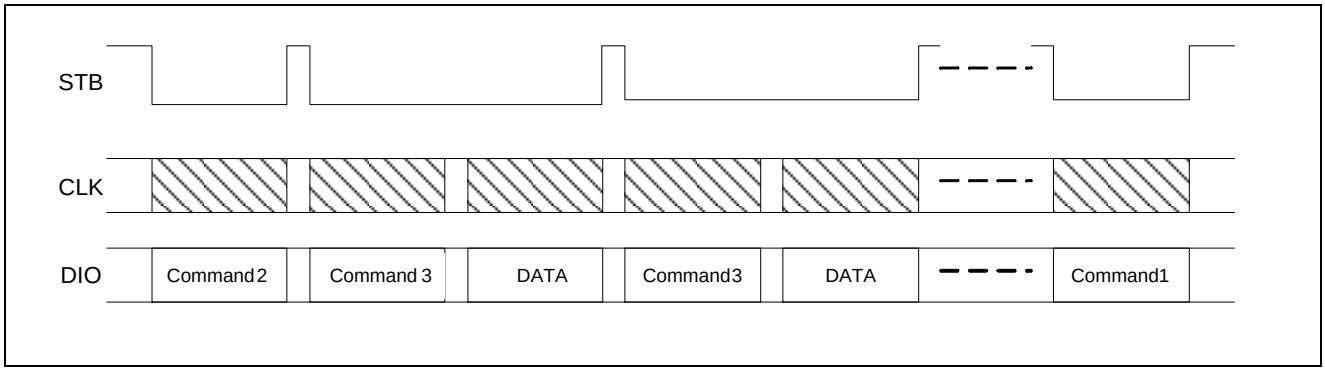
Communication application time series

Continuous display data writing (Automatic address increase)



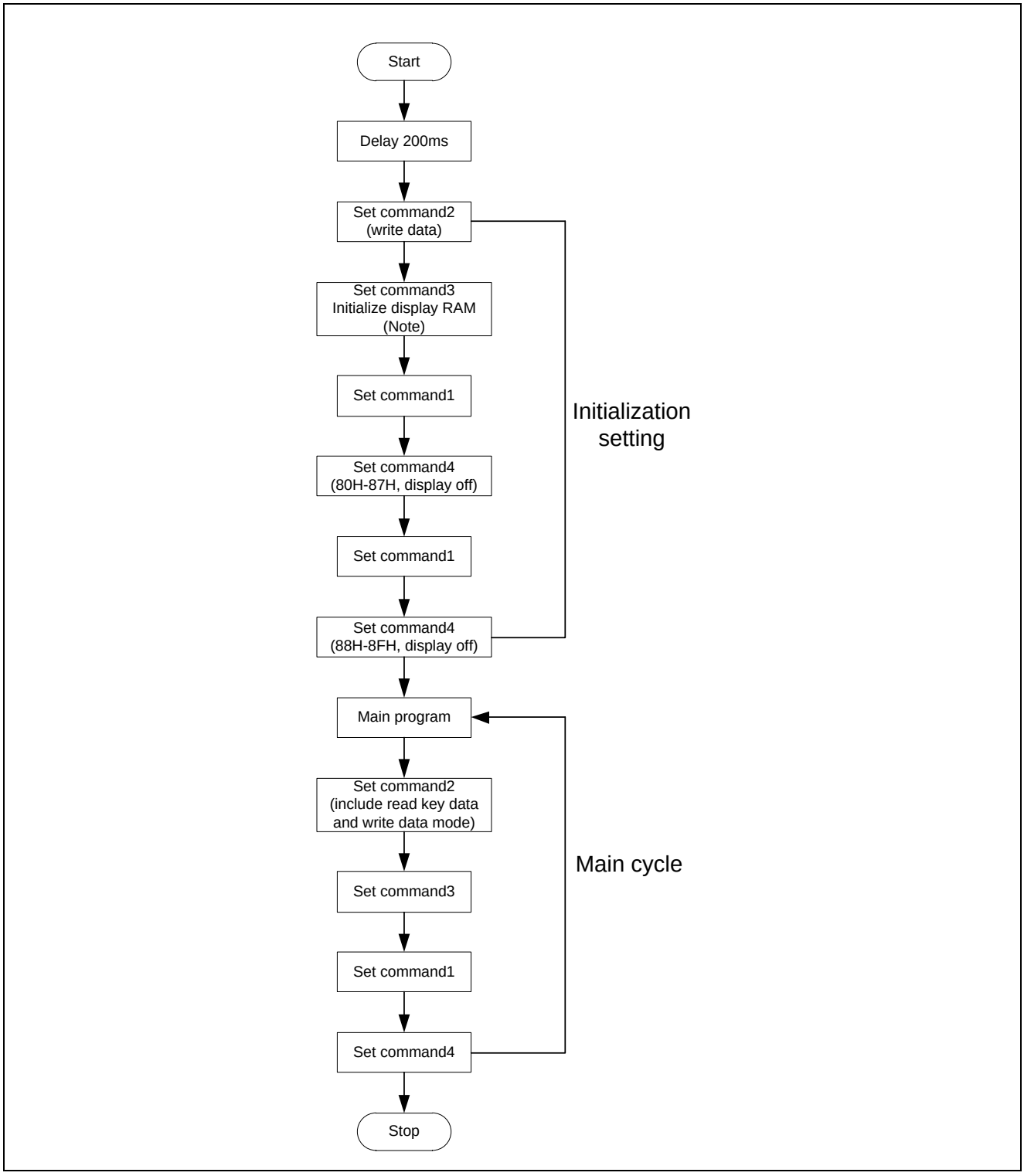
- Command1：Display mode setting
- Command2：Data command setting
- Command3：Address command setting
- DATA1～n： Display data(MAX 14 bytes)
- Command4：Display control command

Single display data writing (fixed address mode)



- Command1：Display mode setting
- Command2：Data command setting
- Command3：Address command setting
- DATA：Display data

Software flow chart



Notes：

- Command1：Display mode setting
- Command2：Data command setting
- Command3：Address command setting
- Command4：Display control command

When the IC is powered on for the first time, the contents of the display RAM are not defined, so be sure to clear the contents of the display RAM in the initialization setting.

Absolute Maximum Ratings

(Unless otherwise noted ,T_A=25°C)

Characteristic	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.5～+7	V
Logic Input Voltage	V_I	-0.5～V_{DD}+0.5	V
Driver Output Current	I_{OLGR}	+250	mA
	I_{OHSG}	-50	mA
Max Output Driver current	I_{TOTAL}	250	mA
Operating Junction Temperature	T_J	-40～+150	°C
Storage Temperature	T_{STG}	-65～+150	°C

Recommended Operating Conditions

(Unless otherwise noted ,T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	5.0	5.5	V
Dynamic current	I_{DD_DYN} *	—	—	5	mA
High Level Input Voltage	V_{IH}	0.8V_{DD}	—	V_{DD}	V
Low Level Input Voltage	V_{IL}	0	—	0.25V_{DD}	V
Operating Temperature	T_A	-40		85	°C

Note*: Test condition Set display mode command = 80H (display off & no load).

Electrical Characteristics

(Unless otherwise noted, V_{DD}=5V ,T_A=25°C)

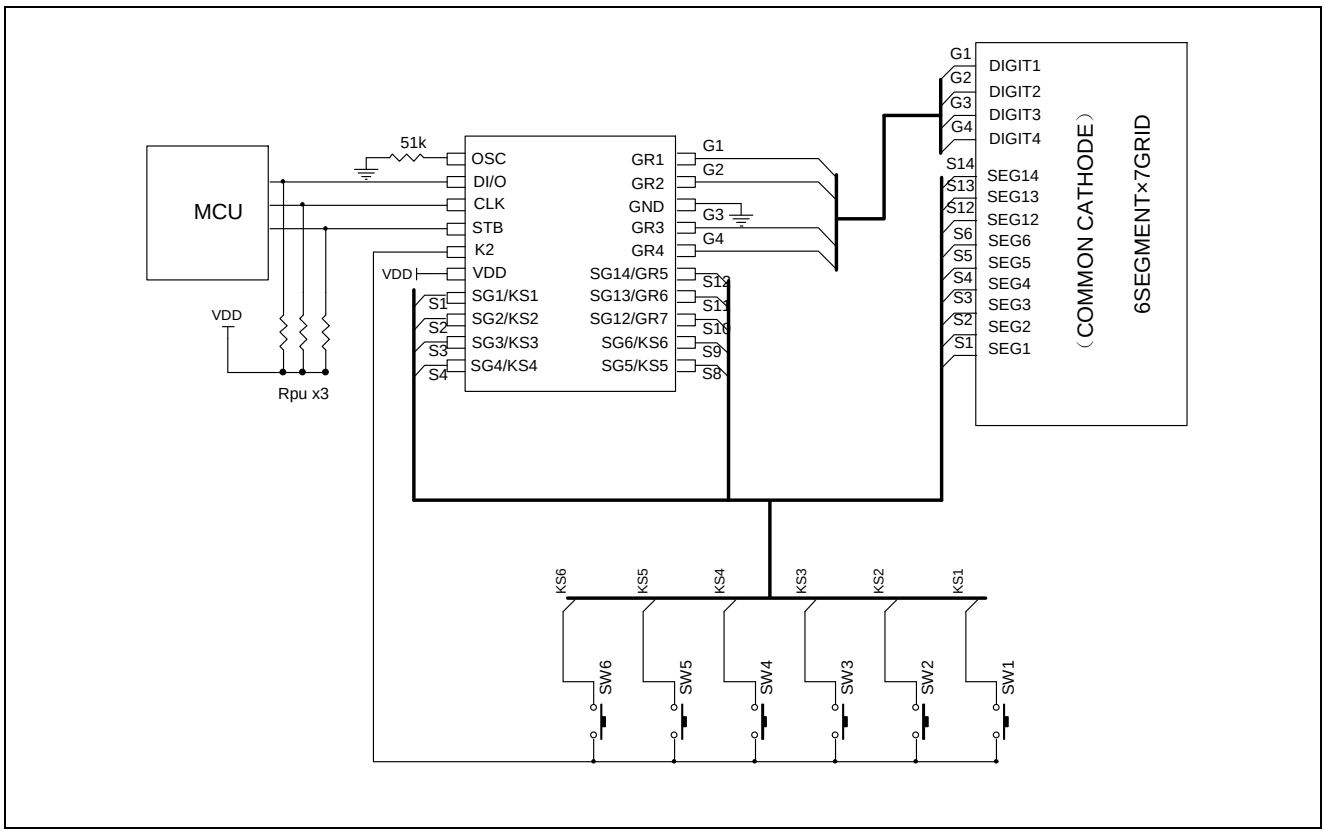
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Output Current	I_{OHSG1}	V_O=V_{DD} -2V，SG1～SG6, SG12/GR7～SG14/GR5	-20	-25	-40	mA
	I_{OHSG2}	V_O=V_{DD} -3V，SG1～SG6, SG12/GR7～SG14/GR5	-25	-30	-50	mA
Low Level Output Current	I_{OLGR}	V_O=0.3V，GR1～GR4, SG12/GR7～SG14/GR5	100	140	—	mA
Low Level Output Current (DIO Pin)	I_{OLDOUT}	V_O=0.4V	4	—	—	mA
Percentage of high level output current at segment	I_{TOLSG}	V_O=V_{DD}-3V，SG1～SG6, SG12GR7～SG14/GR5	—	—	+5	%
High Level Input Voltage	V_{IH}	—	0.6V_{DD}	—	V_{DD}	V
Low Level Input Voltage	V_{IL}	—	0	—	0.3V_{DD}	V
Oscillation Frequency	F_{OSC}	R = 51k	350	500	650	kHz
K2 Pull-down Resistance	R_{KN}	K2	40	—	100	kΩ

Electrical Characteristics

(Unless otherwise noted, V_{DD}=3.3V ,T_A=25°C)

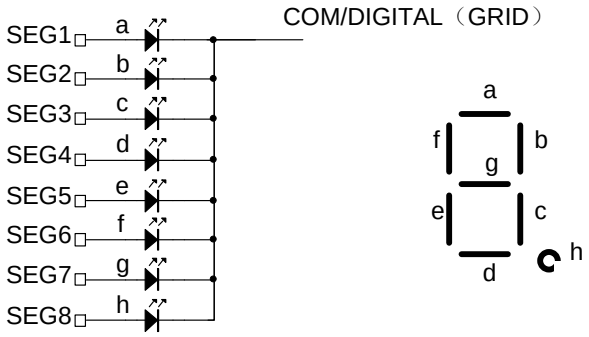
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Output Current	I_{OHSG1}	V_O = V_{DD} - 2V，SG1～SG6, SG12～SG14	-15	-20	-35	mA
Low Level Output Current	I_{OLGR}	V_O =0.3V，GR1～GR7,	85	110	—	mA
Low Level Output Current (DIO Pin)	I_{OLDOUT}	V_O=0.4V	4	—	—	mA
High Level Input Voltage	V_{IH}	—	0.8V_{DD}	—	3.3	V
Low Level Input Voltage	V_{IL}	—	0	—	0.3V_{DD}	V
Oscillation Frequency	F_{OSC}	R = 51k	300	420	580	kHz
K2 Pull-down Resistance	R_{KN}	K2	40	—	100	kΩ

Application circuit



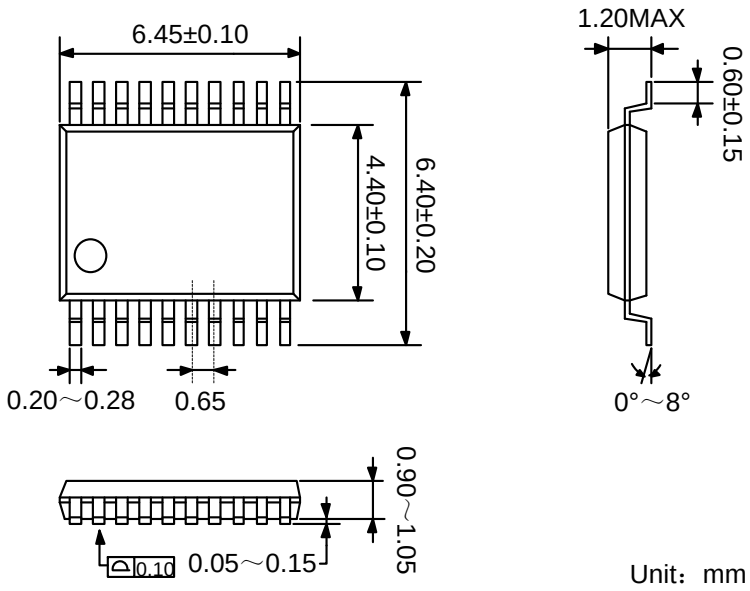
Note： This application circuit is only for reference, and the filter capacitor(recommended ≥1uF) should be placed as close as possible to the VDD. R_{PU} recommended 3.3K to 10KΩ.

Common cathode LED connection

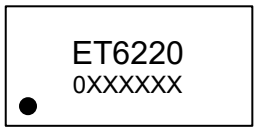


Package

TSSOP20



Marking



ET6220 - Part Number
0XXXXXX - Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2018-01-19		Shilj	Shilj	Zhujl
1.4	2023-2-19	Update Typeset	Shibo	Shilj	Zhujl