High Input, Ultra-low Noise, Low IQ 500mA LDO

General Description

The ET55HS24 is a low-dropout linear regulator (LDO) designed for 2.5V to 20V power supplies, delivering a maximum output current of 500mA. Featuring high power rejection ratio and low noise characteristics, making it ideal for powering high-performance analog and mixed-signal circuits. The device employs an advanced circuit architecture and unique processing technology, with both C_{IN} and C_{OUT} requiring only a compact 2.2uF ceramic output capacitor to achieve excellent transient response performance for both lines and loads.

The ET55HS24's output voltage can be adjusted above the initial set point using an external feedback divider.

Features

- Input voltage range: 2.5V to 20V
- Adjust output voltage range: 1.2V to V_{IN}-1V
- Fixed output voltage versions: 3.3V (only ET55HS24Y-33) and 5V (only ET55HS24Y-50)
- Low static current: 50uA (typical)
- Low turn-off current: 1.2uA
- Ultra-low noise: 10uVrms (typical) @10mA
- High power supply rejection ratio (PSRR)
  -- 91dB @ 10kHz
  -- 70dB @ 100kHz
  -- 60dB @ 1MHz
- Output current: 500mA
- Output voltage accuracy: ±1%
- Low dropout voltage:
  -- 20mV @ 10mA
  -- 250mV @ 200mA
  -- 700mV @ 500mA
- Internal soft start
- Precision-enable control
- Reverse input protection
- Available in various packages including SOP8, DFN6 (2×2), and SOT23-5

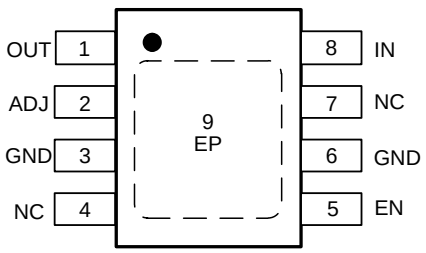
Application

- Suitable for noise-sensitive applications such as ADCs, DACs, and precision amplifiers.
- Communications and infrastructure
- Health care
- Industry and instrumentation

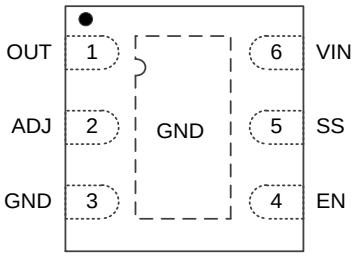
Device Information

Part No.	Package	Packing Option	MSL
ET55HS24M	SOP8	Tape and Reel, 4K	Level 3
ET55HS24Y	DFN6 (2mm×2mm)	Tape and Reel, 3K	Level 1
ET55HS24Y1	DFN6 (2mm×2mm)	Tape and Reel, 3K	Level 1
ET55HS24	SOT23-5	Tape and Reel, 3K	Level 3
ET55HS24T	SOT23-5	Tape and Reel, 3K	Level 3

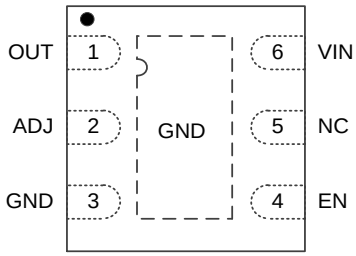
Pin Configuration



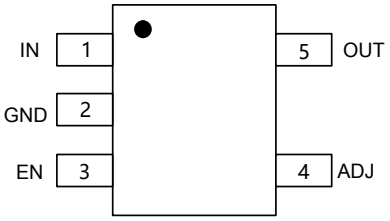
ET55HS24M (SOP8)



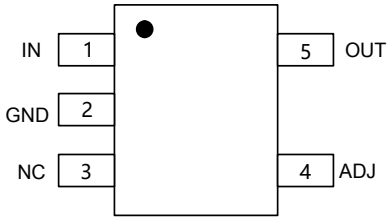
ET55HS24Y(DFN6)



ET55HS24Y1(DFN6)



ET55HS24 (SOT23-5)



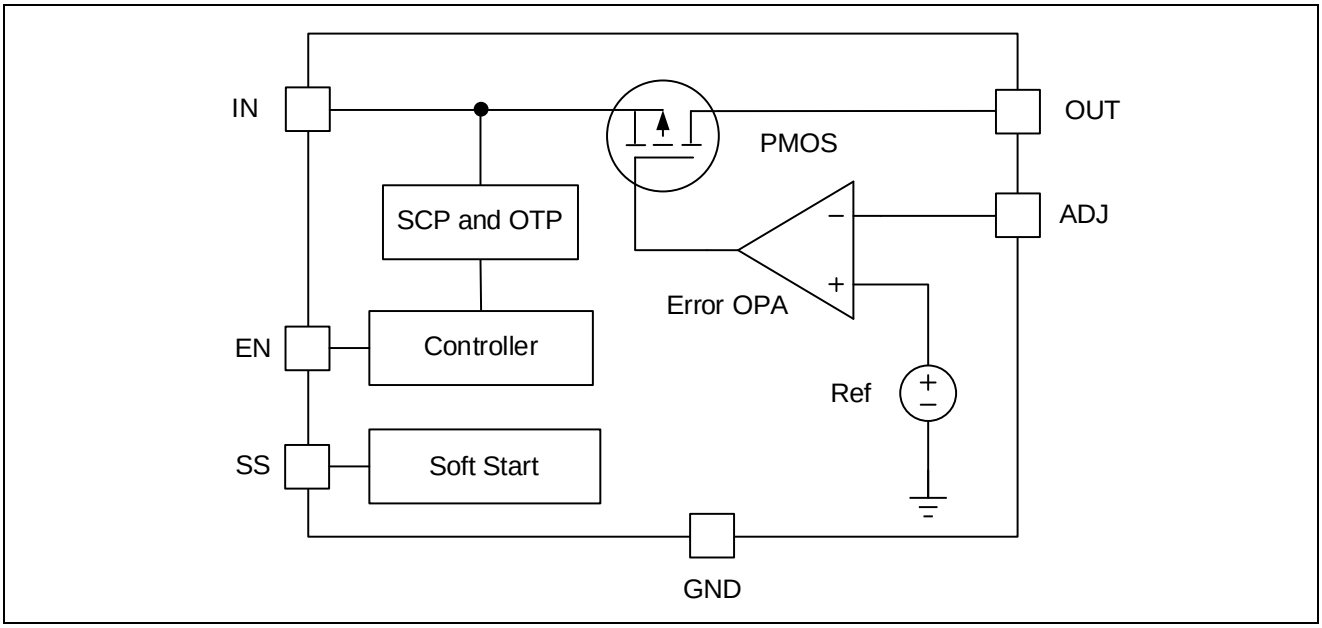
ET55HS24T(SOT23-5)

Top View

Pin Function

SOP8	DFN6		SOT23-5		Pin Name	Pin description
	Y	Y1	/	T		
1	1	1	5	5	OUT	Output voltage port pin, requires a bypass capacitor of 2.2μF or larger to connect OUT to GND.
2	2	2	4	4	ADJ	Detect input pin, connect to the load side, and use an external resistor divider to set the output voltage higher than the fixed output voltage
3,6	3	3	2	2	GND	Ground Pin.
5	4	4	3	/	EN	Enable the pin: Set EN high to activate the voltage regulator, set EN low to deactivate it, and connect EN to IN for automatic startup.
8	6	6	1	1	IN	The voltage regulator's input power pin, should be bypassed to GND using a 2.2μF or larger capacitor.
4,7	5	/	/	/	SS	Soft start time adjustment pin. External capacitors with different capacitance values can adjust the soft start time.
/	/	5	/	3	NC	No connect
9					EP	Heat dissipation pin. Since EP pads are electrically connected to the internal GND, it is recommended to connect to the GND layer.

Block Diagram



Functional Description

Input Bypass capacitor

The input capacitor should be at least 2.2uF and placed as close to the chip as possible to minimize PCB traces' impact on the circuit. If the output capacitor exceeds 2.2uF, increase the input capacitor value accordingly.

Output capacitance

The ESR of the output capacitor impacts the stability of the LDO control loop. To ensure stable chip operation, a 2.2uF output capacitor with ESR below 0.3 Ω and ESL under 2nH is recommended. Additionally, the output capacitor affects the transient response to load current variations. For applications requiring high transient response or significant load current fluctuations, using a larger capacitance value is advised to enhance the transient response of the ET55HS24.

Input and output capacitance characteristics

Input/output capacitors must maintain proper operation within the specified temperature range and under DC bias conditions. X5R or X7R dielectric capacitors are recommended. Y5V and Z5U dielectric capacitors have poor temperature and current bias characteristics and are not recommended.

Current limit and Over-thermal protection

The chip incorporates current limiting and thermal overload protection circuits to prevent damage caused by excessive power consumption. When the output current exceeds 630mA (typical value), the chip enters current limiting protection mode, reducing the output voltage. If the junction temperature surpasses 150°C, the chip activates its overheat protection function, temporarily shutting down the output. When the junction temperature drops below 130°C, the overheat protection is deactivated, and the chip resumes output. Notably, a short circuit causes intense heat generation, triggering the overheat protection when junction temperature exceeds 150°C. If the short circuit issue isn't resolved promptly, the chip will re-enter current limiting protection mode and activate overheat protection again upon temperature recovery, creating a recurring cycle until the fault is cleared. To ensure stable operation, external power consumption must be controlled to keep junction temperature below 150°C.

Soft Start

The ET55HS24 features a voltage-controlled soft-start function with an external capacitor (SS pin). This capability is crucial for eliminating power-on initialization issues in scenarios where the device drives FPGAs, DSPs, or other processors. By controlling the output voltage ramp, the peak inrush current during startup is reduced, thereby minimizing transient effects on the input power bus. The soft-start ramp time depends on the soft-start current (I_{SS}) and soft-start capacitor (C_{SS}), which can be calculated using Equation 1:

$$T_{SS} = 500\mu s + (C_{SS}pF / I_{SS}\mu A) \quad (1)$$

The I_{SS} is the soft-start charging current, which is 0.787uA.

The 500us in Equation 1 represents the initial soft-start time without ADJ mode. When using ADJ mode to adjust the output voltage, this initial time should be recalibrated based on actual measured values. The C_{SS} must be a low-leakage current capacitor, preferably made of X7R, X5R, or C0G dielectric materials. When this feature is disabled, the SS pin remains floating, resulting in an initial soft-start time of approximately

442us for the output voltage.

Enable and disable operations

Under normal operating conditions, the ET55HS24 uses the EN pin to enable or disable the output voltage. When EN is high, VOUT is activated; when EN is low, VOUT is deactivated. For automatic startup, connect EN to IN.

Output voltage adjustment principle

The adjustable output voltage version allows voltage adjustment through external voltage divider resistors (the maximum output voltage is limited by device characteristics). The voltage adjustment principle is shown in Equation 2, where R1 and R2 are the resistors in the output voltage divider, and V_{REF}=1.2V。

$$\mathbf{V_{OUT} = V_{REF} \times (1 + R1 / R2)} \quad \mathbf{(2)}$$

Adjustable output voltage device applications

The ET55HS24 model list includes the ADJ variant, which uses 1.2V as its reference voltage for ADJ adjustment. For higher output voltage requirements in practical applications, simply select an appropriate voltage divider resistor. For example, to achieve 6V output voltage, use V_{REF} =1.2V as specified in Equation 2.

If R1 is 200K, R2 can be set to 50K.

The calculation is as follows: V_{OUT}=1.2 × (1 + 200K / 50K) = 6V

Fixed output voltage device applications

The ET55HS24 model list includes devices with fixed output voltage. Refer to the model selection list.

If you need to adjust the fixed output voltage in practical applications, simply refer to Equation 1. Here is a calculation example:

For fixed 5V output, to achieve 6V output voltage, use 5V reference voltage (V_{REF}) according to Equation 2. Select 40kΩ resistor (R1) and 200kΩ resistor (R2).

V_{OUT}= V_{REF}×(1 + R1/R2)

=5V×(1+40K/200K)

=6V

Recommendations for R1 and R2 component selection: It is recommended to keep R2 below 200kΩ to minimize output voltage errors caused by ADJ pin input current. Additionally, connecting a 100nF feedforward capacitor (C_{FF}) in parallel with R1 helps reduce output voltage noise and PSRR in ADJ mode. For example, when both R1 and R2 are 200kΩ and the default output voltage is 1.2V, the adjustable output voltage can reach 2.4V. Assuming a typical ADJ pin input current of 2nA at 25°C, the output voltage error caused by this current is 0.2mV (0.016%).

Absolute Maximum Ratings

Symbol	Parameters	Range	Unit
V_{IN}	Input voltage	-20 to +20	V
V_{OUT}	Output voltage	-0.3 to V_{IN}	V
V_{EN}	Enable pin voltage	-0.3 to V_{IN}	V
V_{ADJ}	ADJ pin voltage	-0.3 to +5.5	V
T_{JMAX}	Maximum junction temperature range	+150	°C
T_{STG}	storage temperature	-50 to +150	°C

Note : Exceeding the specified absolute maximum rated values may cause permanent damage to the product. These values represent nominal limits only. The product's operational capability under these conditions or any other specifications beyond those outlined in the technical specifications' operating section cannot be guaranteed. Prolonged operation beyond the maximum rated values will compromise the product's reliability.

Thermal Performance

Thermal Resistance	SOP8	DFN6	SOT23-5	Unit
$R_{\theta JA}$	113.9	100.0	182.0	°C /W
$R_{\theta JC}$	54.7	77.0	70.0	°C /W

The PCB's layered structure, copper foil thickness, device thermal pads, and the number and diameter of vias near components all influence thermal characteristics. These factors should be evaluated based on actual application requirements.

The thermal resistance coefficient of SOP8 shown in the table is based on a PCB with dimensions of 115×76cm (length × width), a thickness of 1.6mm, a 4-layer board, and a copper ratio of 20%,100%,100%, and 5% for L1 to L4 respectively, with a copper thickness of 1 ounce for each layer.

Recommended Operating Conditions

Symbol	Parameters	Range	Unit
V_{IN}	input voltage	2.5 to 20	V
I_{OUT}	Output voltage	0 to 500	mA
T_J	Operating Junction Temperature Range	-40 to +125	°C
C_{IN}	Enter the effective capacitance of the ceramic capacitor	>1.5	μF
C_{OUT}	Output the effective capacitance of the ceramic capacitor	>1.5	μF
ESR	Equivalent Series Resistance of input/output capacitors	5 to 100	mΩ

Electrical Characteristics

Unless otherwise noted, (V_{IN} =V_{OUT} +1V) or 5V, V_{OUT} = 3.3V, I_{OUT} = 10mA, C_{IN} =C_{OUT} =2.2μF, T_A=25°C

Symbol	Parameter	Test Conditions[6]	Min	Typ	Max	Unit
V_{IN}	Input Voltage Operation Range		2.5		20	V
I_{Q_ON}	DC Supply Quiescent Current	I_{OUT} = 0mA		50		μA
I_{GND}	GND Current	I_{OUT} = 10mA		140		μA
		I_{OUT} = 500mA		2		mA
I_{Q_OFF}	DC Supply Shutdown Current	EN = GND		1.2		μA
V_{OUT}	Regulated Output Voltage		-1		1	%
I_{OUT}	Output Current			200		mA
$Line_{REG}$	Output Voltage Line Regulation	V_{IN} = (V_{OUT}+1V) to 20V		0.002		%/V
$Load_{REG}$	Output Voltage Load Regulation[2]	I_{OUT} = 100μA to 500mA		0.002		%/mA
V_{DROP}	Dropout Voltage[3]	I_{OUT} = 10mA		20		mV
		I_{OUT} = 200mA		250		mV
		I_{OUT} = 500mA		700		mV
t_{ON}	Soft-start Time[4]	From V_{EN} > V_{ENH} to V_{OUT} = 90% of $V_{OUT(NOM)}$		356		μs
I_{LIMIT}	Current Limit[5]			630		mA
V_{UVLO_R}	Under-Voltage Lockout, Rise			2.5		V
V_{UVLO_F}	Under-Voltage Lockout, Fall			2.2		V
V_{UVLO_HYS}	Under-voltage Threshold Hysteresis			300		mV
V_{ENH}	EN Input Logic Low Voltage	2.5V ≤ V_{IN} ≤ 20V		1.2	1.3	V
V_{ENL}	EN Input Logic High Voltage	2.5V ≤ V_{IN} ≤ 20V		1.1		V
$V_{EN\text{-}HYS}$	EN Input Logic Threshold Hysteresis	2.5V ≤ V_{IN} ≤ 20V		120		mV
t_{DON}	EN Input Delay Time	From V_{EN} > 0V to V_{OUT} = 10% of $V_{OUT(NOM)}$		80		μs
e_N	Output Noise Voltage	f = 10Hz to 100KHz		10		μV_{RMS}

PSRR	Power Supply Rejection Ratio	I_{OUT} = 10mA, f = 10kHz, V_{IN} = 5V, V_{OUT} = 3.3V		90		dB
		I_{OUT} = 10mA, f = 100kHz, V_{IN} = 5V, V_{OUT} = 3.3V		70		dB
		I_{OUT} = 10mA, f = 1MHz, V_{IN} = 5V, V_{OUT} = 3.3V		60		dB
t_{SS}	Soft Start	C_{SS} float, I_{SS}=0.787μA t_{SS} = (500μs)+(C_{SS} pF)/(I_{SS} μA) From V_{EN} > V_{ENH} to V_{OUT} = 90% of $V_{OUT(NOM)}$		442		μs
T_{SD}	Over-temperature Shutdown Threshold	T_J Rising		150		°C
T_{HYS}	Over-temperature Shutdown Hysteresis	T_J Falling from Shutdown		15		°C

Note (2). Calculated based on the endpoint using 100uA and 500mA load.

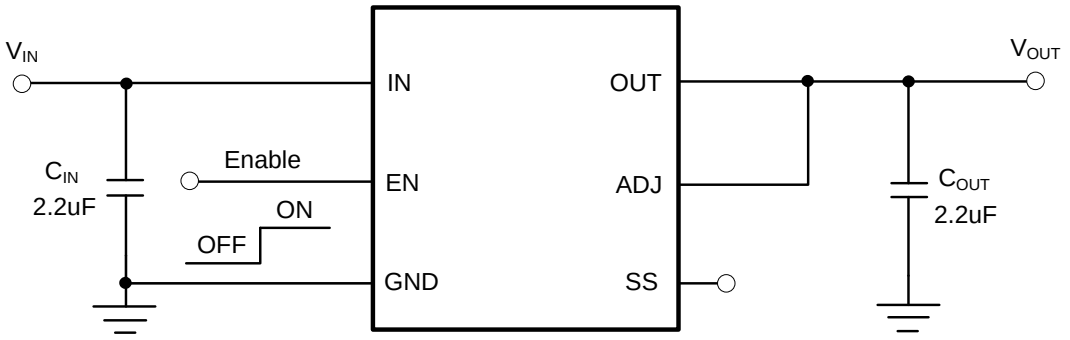
Note (3). The voltage difference is defined as the voltage difference between the input and output when the input voltage is set to the nominal output voltage. The voltage difference is only applicable to output voltages above 2.5V.

Note (4). The start time is defined as the duration from the rising edge of EN to when OUT reaches 90% of its nominal value.

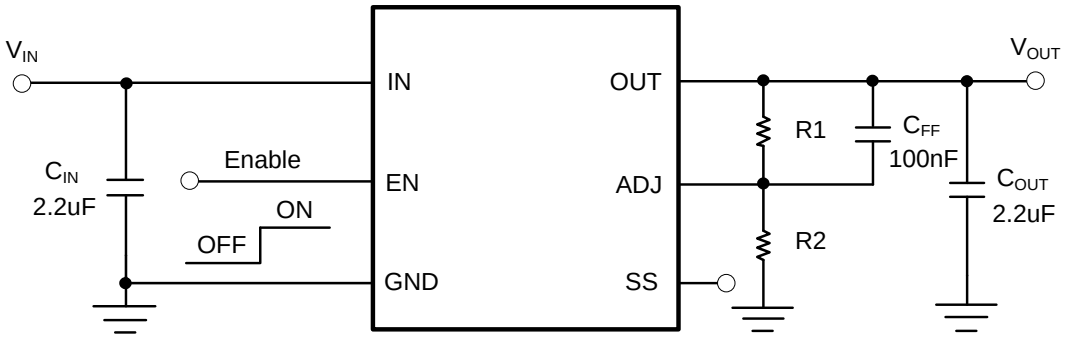
Note (5). The current limit threshold is defined as the current at which the output voltage drops to 90% of the rated typical value. For example, the current limit for a 5.0V output voltage is defined as the current that causes the output voltage to drop to 90% of 5.0V, or 4.5V.

Note (6). Under all operating conditions, input and output capacitors must be at least 1.5uF. When selecting components, consider all application conditions to ensure minimum capacitance requirements. For any LDO, use X7R/X5R capacitors instead of Y5V/Z5U capacitors.

Application Circuits



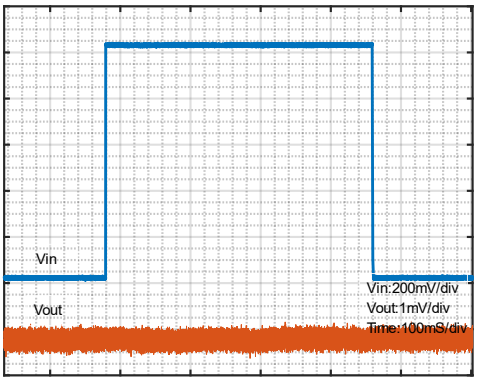
ET55HS24Y with fixed output voltage circuit



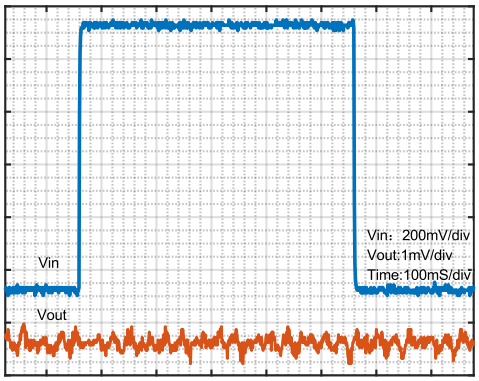
ET55HS24 with adjustable output voltage circuit

Typical Characteristics

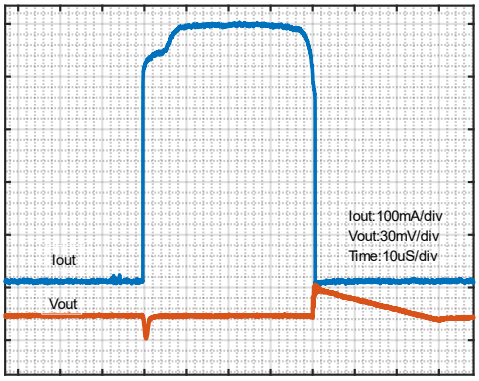
V_{IN} = (V_{OUT} + 1V) or 2.5V(the higher value), V_{REF} = V_{IN}, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 2.2μF, T_A = +25°C, temperature curve test based on T_J ,unless otherwise specified



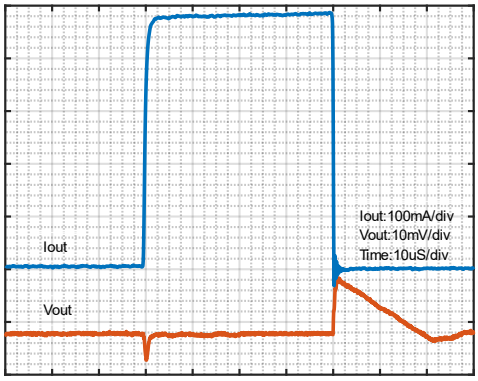
Line Transient
(V_{IN}=3.7~4.7V,V_{OUT}=1.2V, I_{OUT}=500mA)



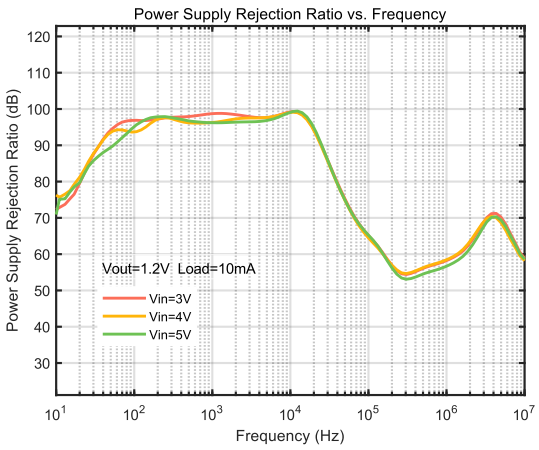
Line Transient
(V_{IN}=4~5V,V_{OUT}=3V, I_{OUT}=500mA)



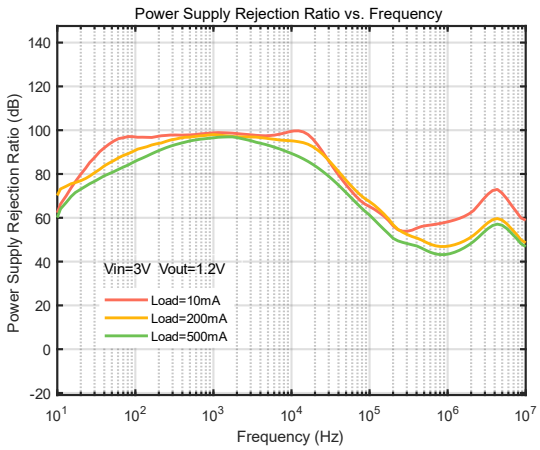
Load Transient
(V_{OUT}=1.2V I_{OUT}=10~500mA)



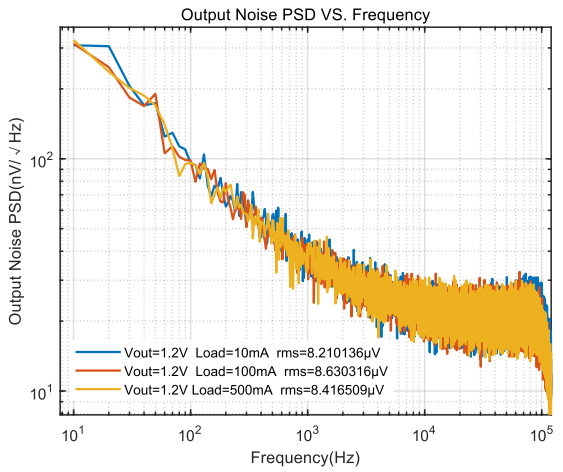
Load Transient
(V_{OUT}=3V I_{OUT}=10~500mA)



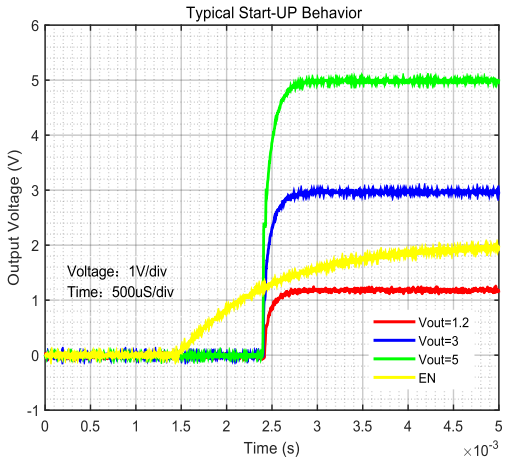
PSRR(I_{OUT}=10mA)



PSRR(V_{IN}=3V)



Output Noise PSD



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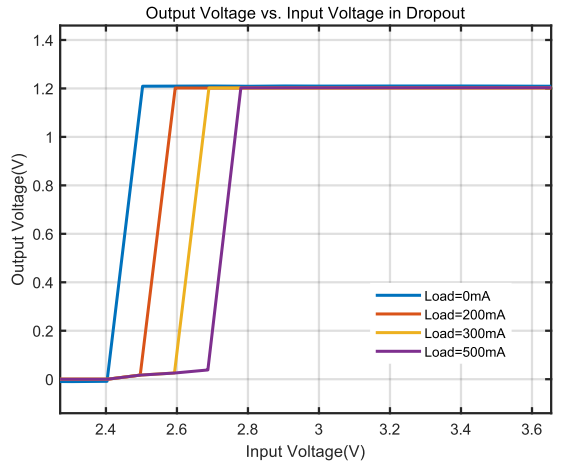
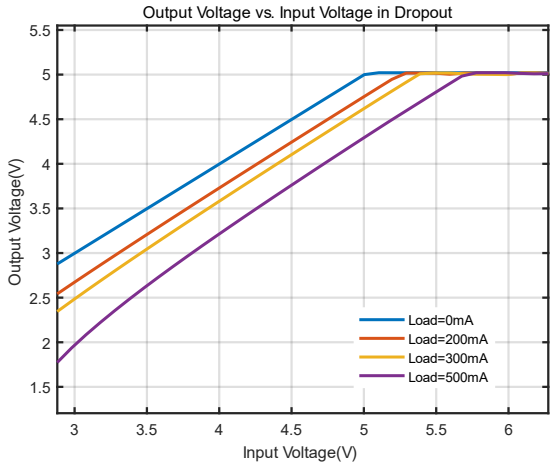
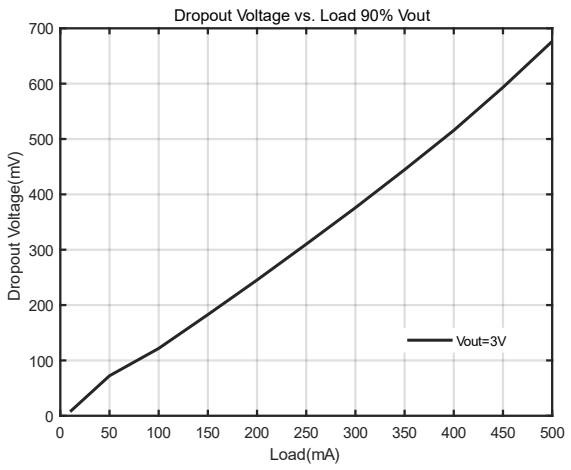
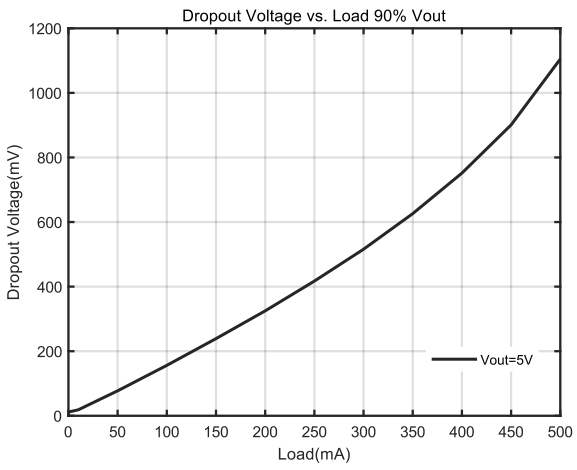
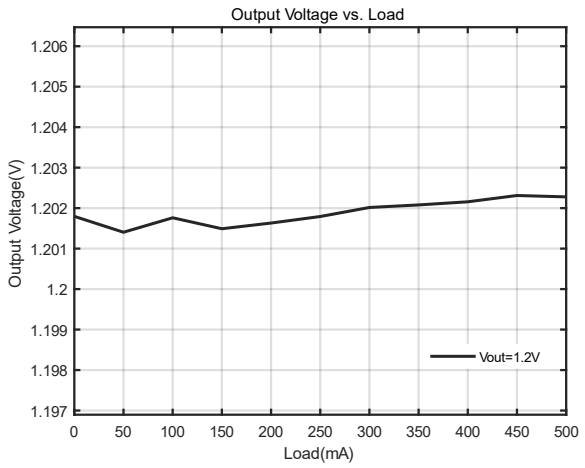
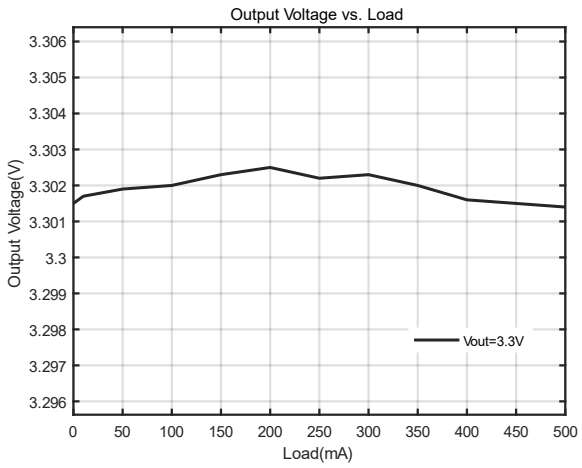


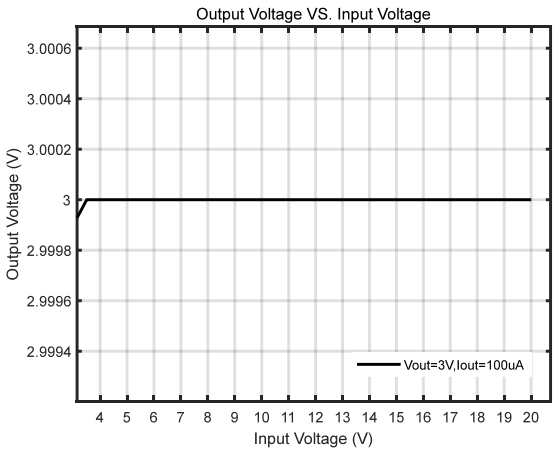


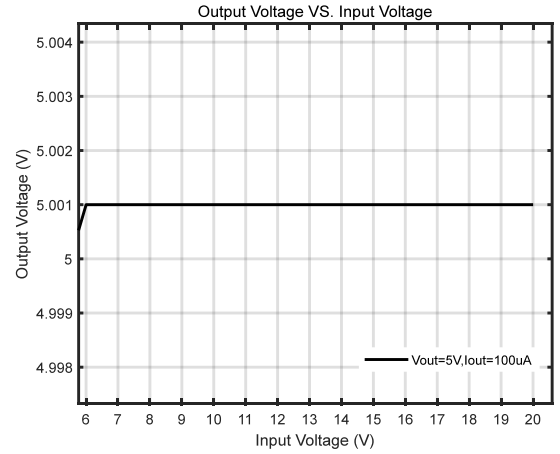


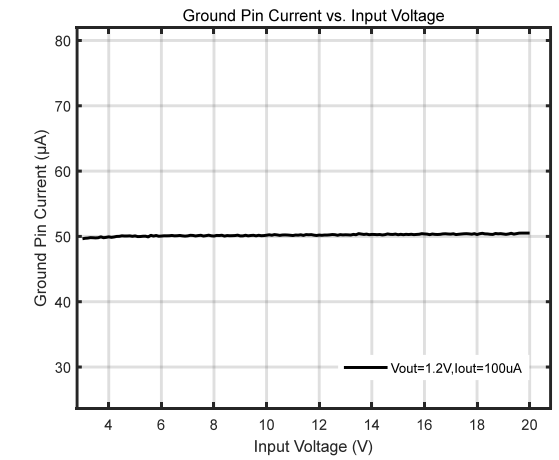


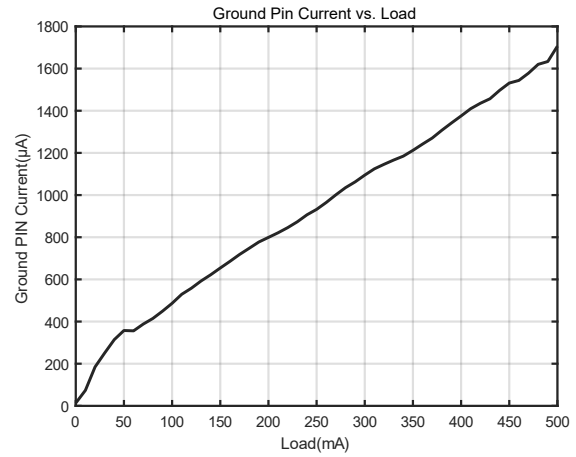

Output Voltage vs. Load
Output Voltage(V)
Load(mA)
Vout=1.2V

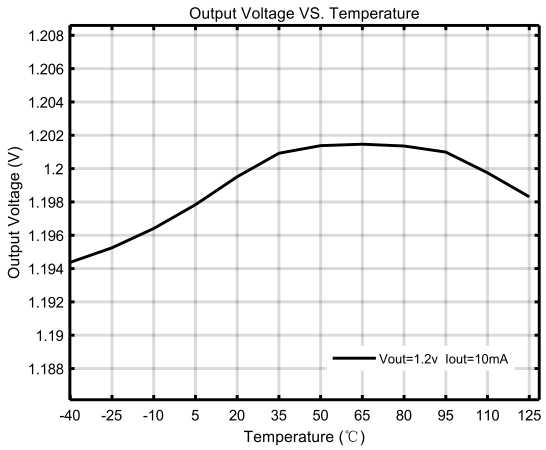

Output Voltage vs. Load
Output Voltage(V)
Load(mA)
Vout=3.3V

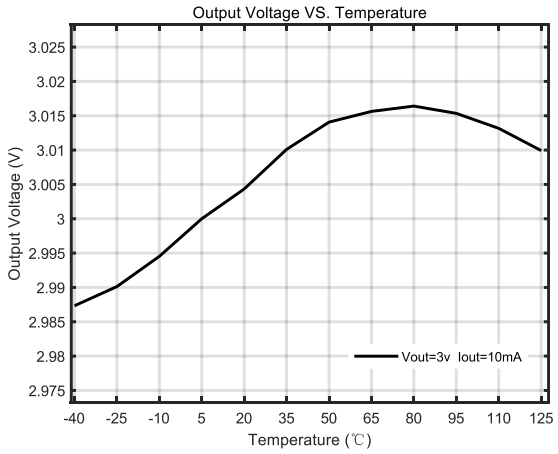

Output Voltage VS. Input Voltage
Output Voltage (V)
Input Voltage (V)
Vout=3V,Iout=100uA

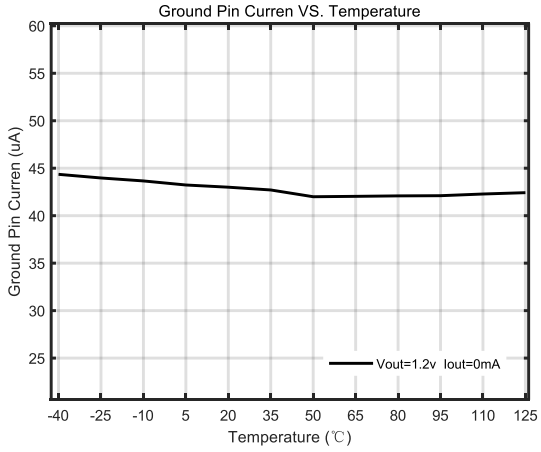

Output Voltage VS. Input Voltage
Output Voltage (V)
Input Voltage (V)
Vout=5V,Iout=100uA

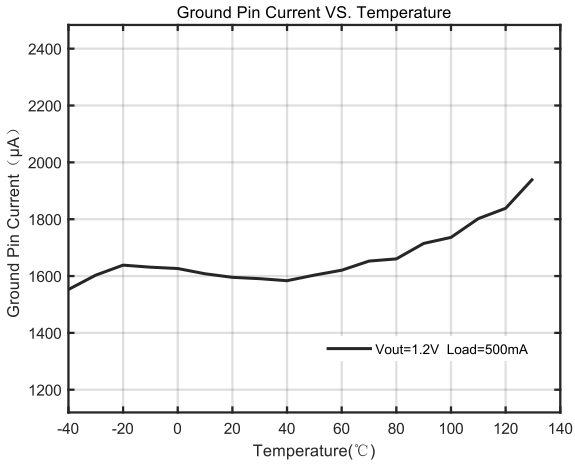

Ground Pin Current vs. Input Voltage
Ground Pin Current (µA)
Input Voltage (V)
Vout=1.2V,Iout=100uA

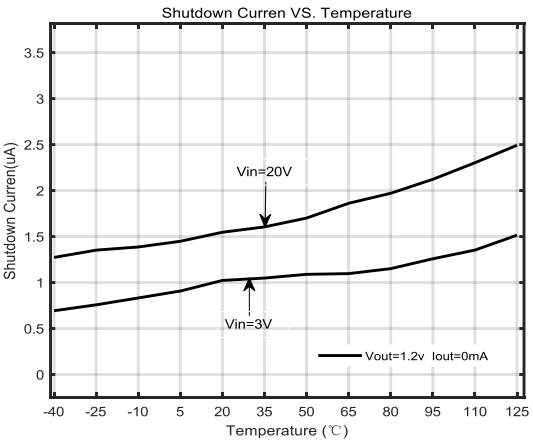

Ground Pin Current vs. Load
Ground PIN Current(µA)
Load(mA)

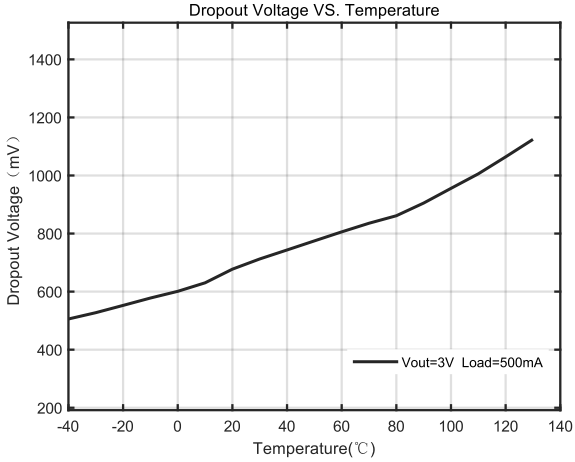

Output Voltage VS. Temperature
Output Voltage (V)
Temperature (℃)
Vout=1.2v Iout=10mA


Output Voltage VS. Temperature
Output Voltage (V)
Temperature (℃)
Vout=3v Iout=10mA


Ground Pin Curren VS. Temperature
Ground Pin Curren (uA)
Temperature (℃)
Vout=1.2v Iout=0mA

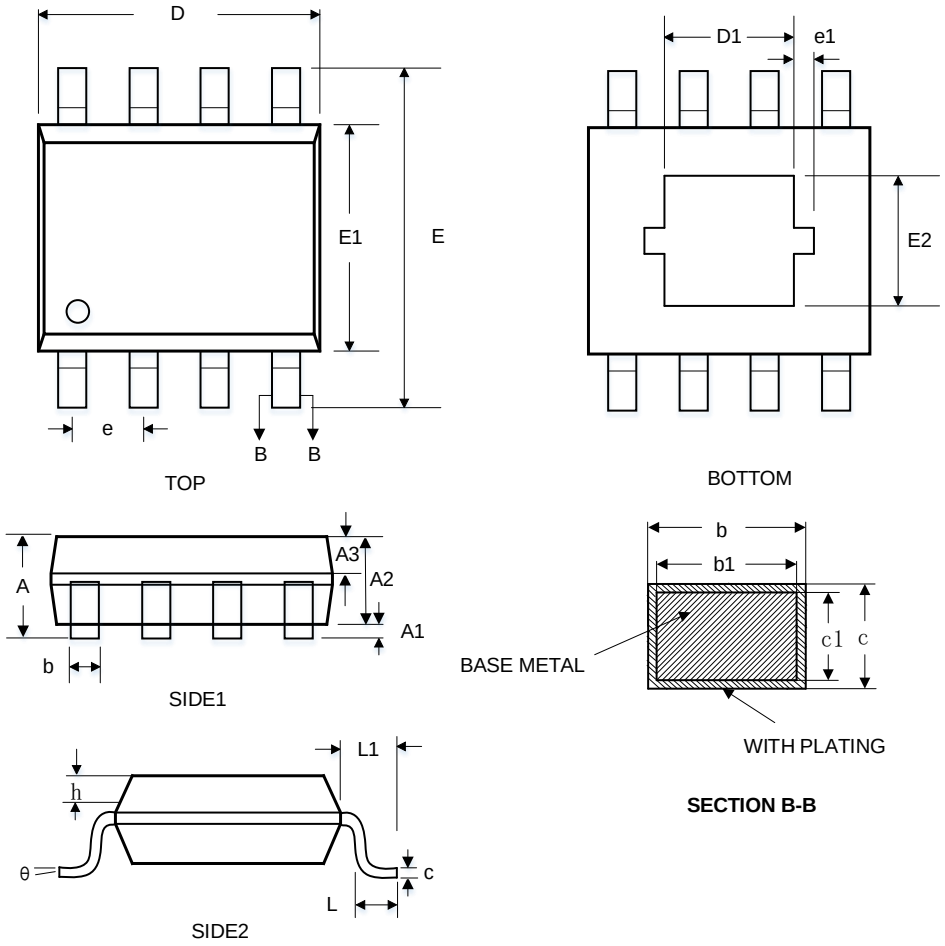

Ground Pin Current VS. Temperature
Ground Pin Current（μA）
Temperature(℃)
Vout=1.2V Load=500mA


Shutdown Curren VS. Temperature
Shutdown Curren(uA)
Temperature (℃)
Vin=20V
Vin=3V
Vout=1.2v Iout=0mA


Dropout Voltage VS. Temperature
Dropout Voltage（mV）
Temperature(℃)
Vout=3V Load=500mA

Package Dimension

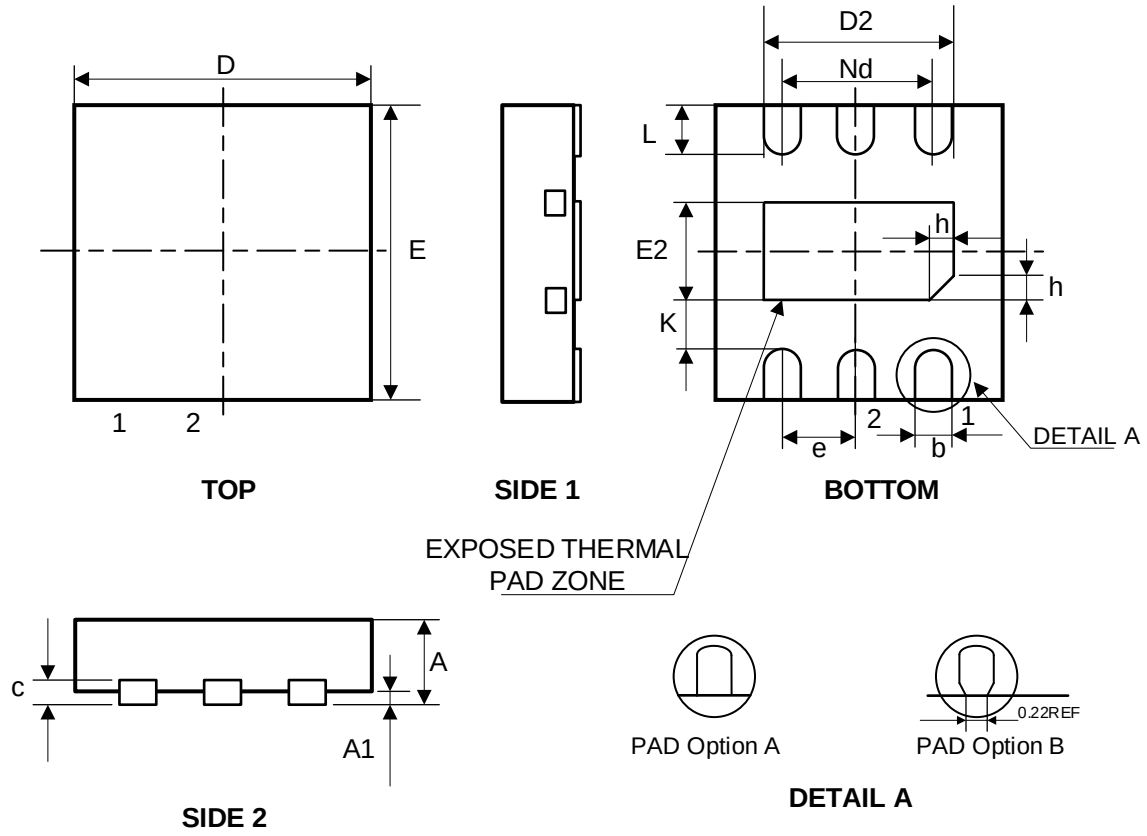
SOP8



(Unit：mm)

Unit / Symbol	MIN	NOM	MAX	Unit / Symbol	MIN	NOM	MAX
A	-	-	1.65	E	5.80	6.00	6.20
A1	0.05	-	0.15	E1	3.80	3.90	4.00
A2	1.30	1.40	1.50	E2	2.21 REF		
A3	0.60	0.65	0.70	e	1.27 BSC		
b	0.39	-	0.47	e1	0.10 REF		
b1	0.38	0.41	0.44	h	0.25	-	0.50
c	0.20	-	0.24	L	0.50	0.60	0.80
c1	0.19	0.20	0.21	L1	1.05 REF		
D	4.80	4.90	5.00	θ	0°	-	8°
D1	3.10 REF						

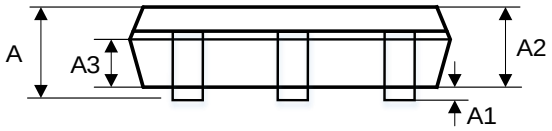
DFN6(2×2)



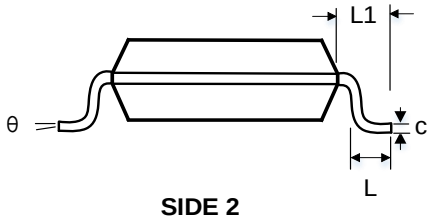
（Unit：mm）

Unit / Symbol	MIN	NOM	MAX	Unit / Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80	E	1.90	2.00	2.10
	0.85	0.90	0.95	E2	0.90	1.00	1.10
A1	-	0.02	0.05	e	0.65 BSC		
b	0.25	0.30	0.35	h	0.15	0.20	0.25
c	0.18	0.20	0.25	L	0.20	0.25	0.30
D	1.90	2.00	2.10	Nd	1.30 BSC		
D2	1.50	1.60	1.70	K	0.20	-	-

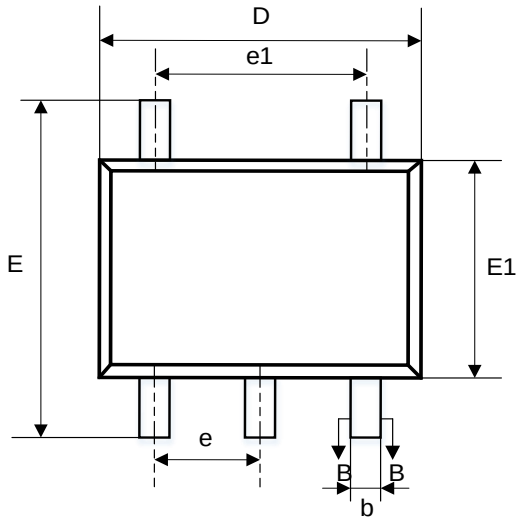
SOT23-5



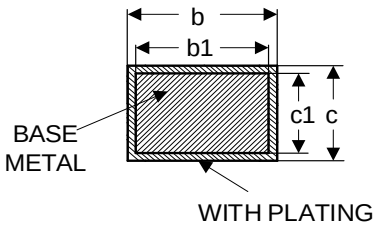
SIDE 1



SIDE 2



TOP



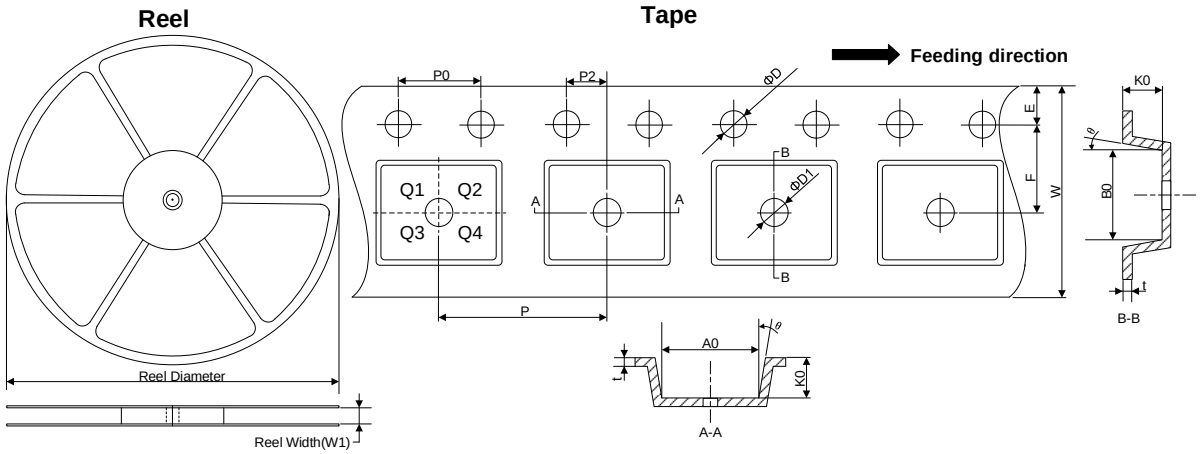
SECTION B-B

（Unit：mm）

Unit / Symbol	MIN	NOM	MAX	Unit / Symbol	MIN	NOM	MAX
A	-	-	1.25	D	2.82	2.92	3.02
A1	0.04	-	0.10	E	2.60	2.80	3.00
A2	1.00	1.10	1.20	E1	1.50	1.60	1.70
A3	0.60	0.65	0.70	e	0.95 BSC		
b	0.33	-	0.41	e1	1.90 BSC		
c	0.15	-	0.19	L	0.30	-	0.60
c1	0.14	0.15	0.16	θ	0°	-	8°

Tape and Reel Information

SOP8

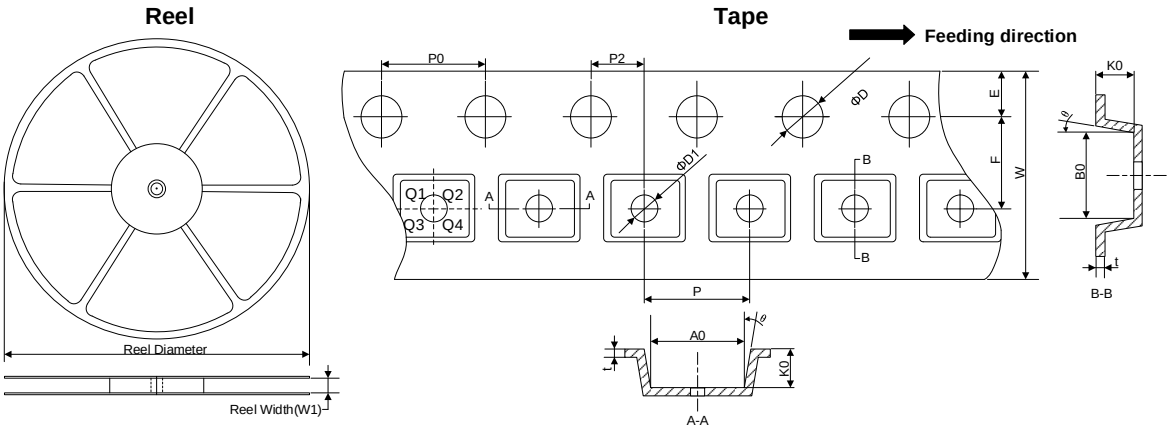


Symbol	Unit
Diameter	13″
Width	12.4

Symbol	Unit(mm)
E	1.75±0.10
F	5.50±0.10
P2	2.00±0.10
D	$1.50^{+0.1}_{0}$
D1	1.55±0.05
P0	4.00±0.10
10P0	40.00±0.20

Symbol	Unit(mm)
W	12.00±0.10
P	8.00±0.10
A0	6.55±0.15
B0	5.30±0.10
K0	2.00±0.15
t	0.25±0.05
θ	3-5°TYP
Pin1	Q3

DFN6(2×2)

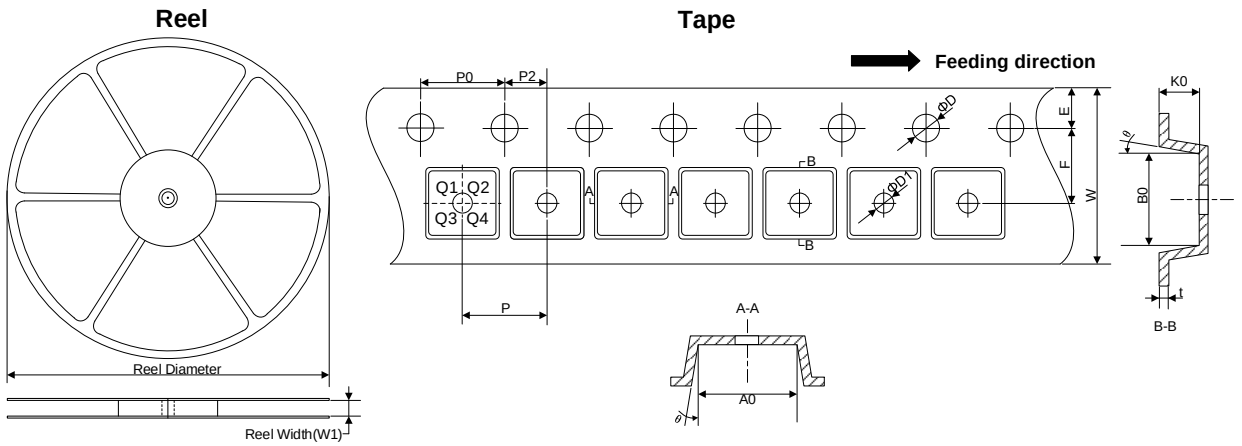


Symbol	Unit
Diameter	7″
Width	8.6

Symbol	Unit(mm)
E	1.75±0.10
F	3.50±0.05
P2	2.00±0.05
D	1.50±0.10
D1	$1.00^{+0.25}_{0}$
P0	4.00±0.10
10P0	40.00±0.20

Symbol	Unit(mm)
W	$8.00^{+0.3}_{-0.1}$
P	4.00±0.10
A0	2.15±0.03
B0	2.15±0.03
K0	0.88±0.05
t	0.254±0.02
θ	5°MAX
Pin1	Q1

SOT23-5



Symbol	Unit
Diameter	7″
Width	8.6

Symbol	Unit (mm)
E	1.75±0.10
F	3.50±0.05
P2	2.00±0.05
D	$1.50^{+0.10}_{0}$
D1	1.05±0.05
P0	4.00±0.10
10P0	40.00±0.20

Symbol	Unit (mm)
W	8.00±0.10
P	4.00±0.10
A0	3.26±0.10
B0	3.30±0.10
K0	1.40±0.10
t	0.20±0.02
θ	3-5°TYP
Pin1	Q3

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2020-07-08	Original Version	Wangp	Liuxm	Liujy
1.0	2024-11-02	Official Version	Yangxx	Liuxm	Liujy