Single D-type Flip-Flop; Positive Edge Trigger

General Description

The ETQ74LVC1G79 is a single positive edge triggered D-type flip-flop, Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in mixed 3.3V and 5V environments.

Schmitt trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging back-flow current through the device when it is powered down.

Features

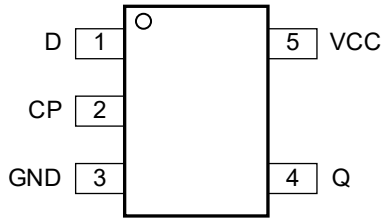
- Wide Supply Voltage Range from 1.65V to 5.5V
- Over Voltage Tolerant Inputs to 5.5V
- High Noise Immunity
- ±24mA Output Drive (V_{CC} = 3.0V)
- CMOS Low Power Consumption
- Direct Interface with TTL Levels
- IOFF Circuitry Provides Partial Power-down Mode Operation
- Multiple Package Options Automotive AEC-Q100 Grade 1 Qualified
  - -- Ambient Temperature Range of -40°C to +125°C
  - -- ESD HBM ±4KV PASS
  - -- ESD CDM ±1.5KV PASS
  - -- Latch Up Current to ±200mA PASS
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ETQ74AHCT1G79	SC70-5(1.3mm × 2.1mm)	Tape and Reel, 3K/Reel	1
ETQ74AHCT1G79T	SOT23-5(1.6mm × 2.9mm)	Tape and Reel, 3K/Reel	3

Applications

- Server
- LED Display Screen
- Network Switches
- Telecommunications Infrastructure
- Motor Driver
- I/O Extender

Pin Configuration



SC70-5/SOT23-5

TOP VIEW

Figure1. Pin Configuration

Pin Function

Pin No.	Pin Name	Pin Function
1	D	Data Input
2	CP	Clock Pulse Input
3	GND	Ground
4	Q	Data Output
5	VCC	Supply Voltage

Functional Diagram

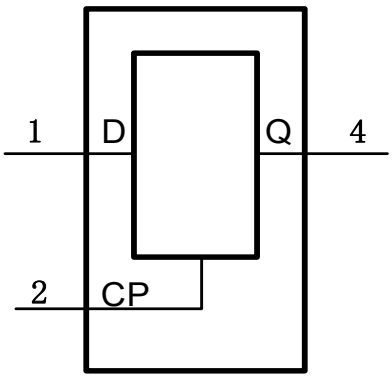


Figure2. Logic Symbol

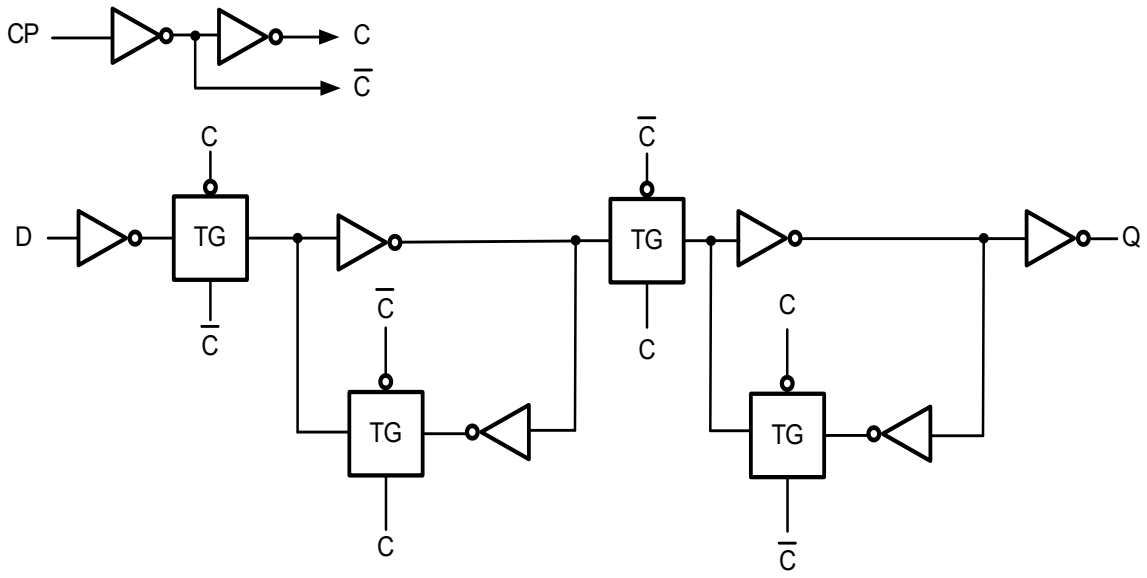


Figure3. Logic Diagram

Function Table

H = High voltage level; L = Low voltage level; ↑ = Low-to-High CP transition; X = don't care;
q = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.

Input		Output
CP	**D**	**Q**
↑	L	L
↑	H	H
L	X	q

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage(VCC Pin)		-0.5~6.5	V
I_{IK}	Input Clamping Current	V_I < 0V	-50	mA
V_I	Input Voltage (1)		-0.5~6.5	V
I_{OK}	Output Clamping Current	V_O > 0V or V_O < 0V	±50	mA
V_O	Output Voltage	Active Mode (1)	-0.5~V_{CC}+0.5	V
		Power-Down Mode V_{CC}=0V (1)	-0.5~+6.5	V
I_O	Output Current	V_O = 0V to V_{CC}	±50	mA
I_{CC}	Supply Current		+100	mA
I_{GND}	Ground Current		-100	mA
T_J	Operating Junction Range		-40 to +150	°C
T_{STG}	Storage Temperature		-65 to +150	°C
V_{ESD}	Human Body Mode (2)		±4000	V
	Charged Device Mode (3)		±1500	V
I_{LU}	Latch Up Current (4)		±200	mA

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per AEC-Q100-002(JEDEC JS-001);

Note3: CDM tested per AEC-Q100-011(JEDEC JS-002);

Note4: Latch up Current Maximum Rating tested per AEC-Q100-004(JEDEC JESD78F).

Recommended Operating Conditions

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage		1.65~5.5	V
V_I	Input Voltage		0~5.5	V
V_O	Output Voltage	Active Mode	0~V_{CC}	V
		Power-Down Mode V_{CC}= 0V	0~5.5	V
T_A	Ambient Temperature		-40 to +125	°C
Δt/ΔV	Input Transition Rise and Fall Rate	V_{CC} = 1.65V to 2.7V	<20	ns/V
		V_{CC} = 2.7V to 5.5V	<10	ns/V

Electrical Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40°C ≤ T_A ≤ +85°C			-40°C ≤ T_A ≤ +125°C		Unit
			Min	Typ [5]	Max	Min	Max	
V_{IH}	High−Level Input Voltage	V_{CC} = 1.65V to 1.95V	0.65V_{CC}			0.65V_{CC}		V
		V_{CC} = 2.3V to 2.7V	1.7			1.7		
		V_{CC} = 2.7V to 3.6V	2.0			2.0		
		V_{cc} = 4.5V to 5.5V	0.7V_{CC}			0.7V_{CC}		
V_{IL}	Low−Level Input Voltage	V_{CC} = 1.65V to 1.95V			0.35V_{CC}		0.35V_{CC}	V
		V_{CC} = 2.3V to 2.7V			0.7		0.7	
		V_{CC} = 2.7V to 3.6V			0.8		0.8	
		V_{cc} = 4.5V to 5.5V			0.3V_{CC}		0.3V_{CC}	
V_{OH}	High-Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_O = -100μA; V_{CC} = 1.65V to 5.5V	V_{CC}-0.1			V_{CC}-0.1		
		I_O = -4mA; V_{CC} = 1.65V	1.2	1.54		0.95		
		I_O = -8mA; V_{CC} = 2.3V	1.9	2.15		1.7		
		I_O = -12mA; V_{CC} = 2.7V	2.2	2.5		1.9		
		I_O = -24mA; V_{CC} = 3.0V	2.3	2.62		2.0		
		I_O = -32mA; V_{CC} = 4.5V	3.8	4.11		3.4		
V_{OL}	Low-Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_O = -100μA; V_{CC} = 1.65V to 5.5V			0.10		0.10	
		I_O = 4mA; V_{CC} = 1.65V		0.07	0.45		0.70	
		I_O = 8mA; V_{CC} = 2.3V		0.09	0.30		0.45	
		I_O = 12mA; V_{CC} = 2.7V		0.16	0.40		0.60	
		I_O = 24mA; V_{CC} = 3.0V		0.17	0.55		0.80	
		I_O = 32mA; V_{CC} = 4.5V		0.18	0.55		0.80	
I_I	Input Leakage Current	V_I = 5.5V or GND; V_{CC} = 0V to 5.5V		±0.1	±5		±20	uA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V; V_{CC} = 0V		±0.1	±10		±20	uA
I_{CC}	Supply Current	V_I = 5.5V or GND; V_{CC} = 1.65V to 5.5V; I_O = 0A		0.1	10		40	uA

ΔI_{CC}	Additional Supply Current	$V_I = V_{CC}$ - 0.6V; I_O = 0A; V_{CC} =2.3V to 5.5V		5.0	500		500	uA
C_I	Input Capacitance			4.5				pF

Dynamic Characteristics

Voltages are referenced to GND (ground = 0V); for test circuit see Figure6.

Symbol	Parameter	Conditions	-40°C ≤ T_A ≤ +85°C			-40°C ≤ T_A ≤ +125°C		Unit
			Min	Typ[5]	Max	Min	Max	
t_{pd}	Propagation Delay	CP to Q; See Figure4						ns
		V_{CC} = 1.65V to 1.95V	1.5	8.2	13.4	1.5	17	
		V_{CC} = 2.3V to 2.7V	1.0	4.6	7.1	1.0	9.0	
		V_{CC} = 2.7V	1.0	4.5	7.1	1.0	9.0	
		V_{CC} = 3.0V to 3.6V	1.0	4.3	5.7	1.0	7.5	
		V_{CC} = 4.5V to 5.5V	1.0	3.0	4.0	1.0	5.5	
t_W	Pulse Width	CP High or Low; See Figure4						ns
		V_{CC} = 1.65V to 1.95V	3			3.0		
		V_{CC} = 2.3V to 2.7V	2.5			2.5		
		V_{CC} = 2.7V	2.5			2.5		
		V_{CC} = 3.0V to 3.6V	2.5			2.5		
		V_{CC} = 4.5V to 5.5V	2.0			2.0		
t_{su}	Set-up Time	D to CP; See Figure4						ns
		V_{CC} = 1.65V to 1.95V	2.5			2.5		
		V_{CC} = 2.3V to 2.7V	1.7			1.7		
		V_{CC} = 2.7V	1.7			1.7		
		V_{CC} = 3.0V to 3.6V	1.3			1.2		
		V_{CC} = 4.5V to 5.5V	1.2			1.2		
t_h	Hold time	D to CP; See Figure4						ns
		V_{CC} = 1.65V to 1.95V	0			0		
		V_{CC} = 2.3V to 2.7V	0			0		
		V_{CC} = 2.7V	0.5			0.5		
		V_{CC} = 3.0V to 3.6V	0.5			0.5		
		V_{CC} = 4.5V to 5.5V	0.5			0.5		
f_{max}	Maximum Frequency	CP; See Figure4						MHz
		V_{CC} = 1.65V to 1.95V	160			160		
		V_{CC} = 2.3V to 2.7V	160			160		
		V_{CC} = 2.7V	160			160		
		V_{CC} = 3.0V to 3.6V	160			160		
		V_{CC} = 4.5V to 5.5V	200			200		

C_{PD} [5]	Power Dissipation Capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3V		27				pF

Note5: All typical values are measured at T_A = 25°C and V_{CC} = 3.3V.

Note6: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:

f_i = Input Frequency in MHz;

f_o = Output Frequency in MHz;

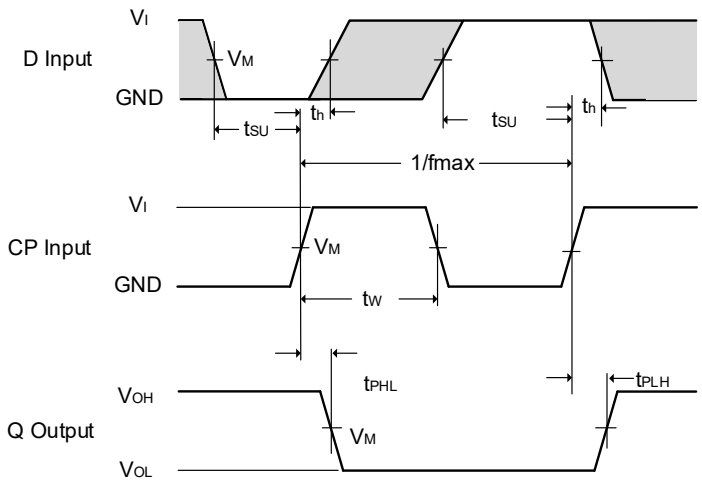
C_L = Output Load capacitance in pF;

V_{CC} = Supply Voltage in V;

N = Number of Inputs Switching;

$\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = Sum of Outputs.

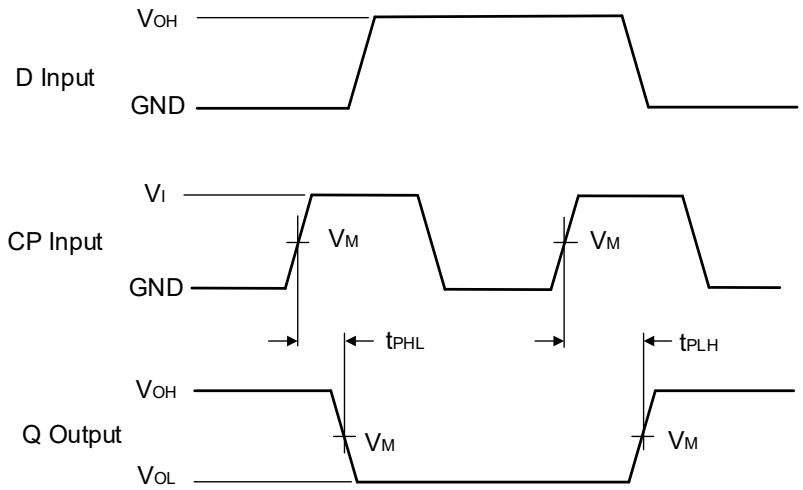
Test Circuit



Measurement points are given in Table 1.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output.

Figure4. Clock (CP) to output (Q) propagation delay times, clock pulse width, D to CP set-up times, CP to D hold times and maximum clock pulse frequency



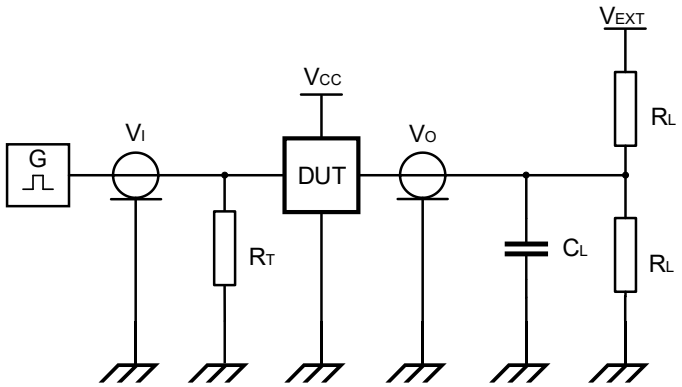
Measurement points are given in Table 1.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure5. Clock (CP) to output (Q) propagation delay times

Table 1. Measurement Points

Supply Voltage	Input	Output
V_{CC}	V_M	V_M
1.65V to 1.95V	0.5 × V_{CC}	0.5 × V_{CC}
2.3V to 2.7V	0.5 × V_{CC}	0.5 × V_{CC}
2.7V	1.5V	1.5V
3.0V to 3.6V	1.5V	1.5V
4.5V to 5.5V	0.5 × V_{CC}	0.5 × V_{CC}



Measurement points are given in Table 2.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

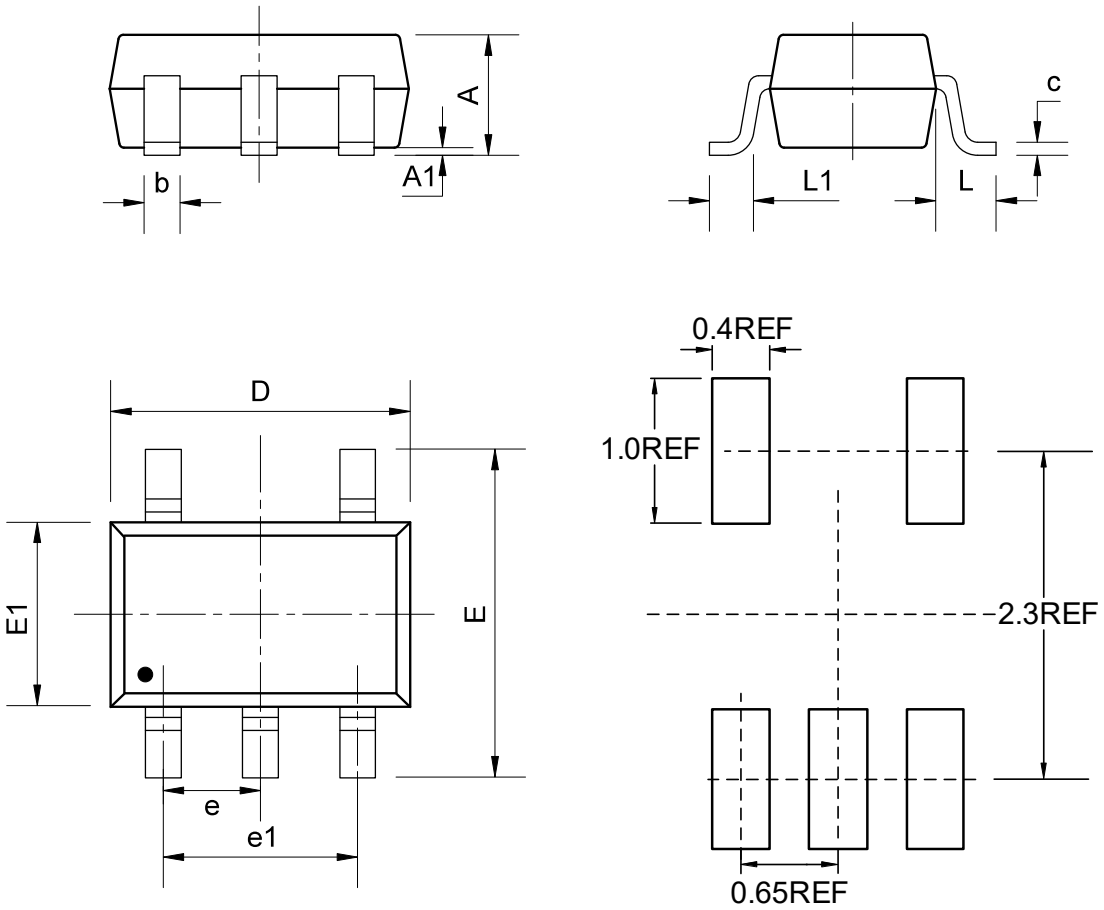
Figure6. Test circuit for measuring switching times

Table 2. Test Data

Supply Voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
1.65V to 1.95V	V_{CC}	≤ 2.0ns	30pF	1kΩ	Open
2.3V to 2.7V	V_{CC}	≤ 2.0ns	30pF	500Ω	Open
2.7V	2.7V	≤ 2.5ns	50pF	500Ω	Open
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω	Open
4.5V to 5.5V	V_{CC}	≤ 2.5ns	50pF	500Ω	Open

Package Dimension

SC70-5(1.3mm × 2.1mm)

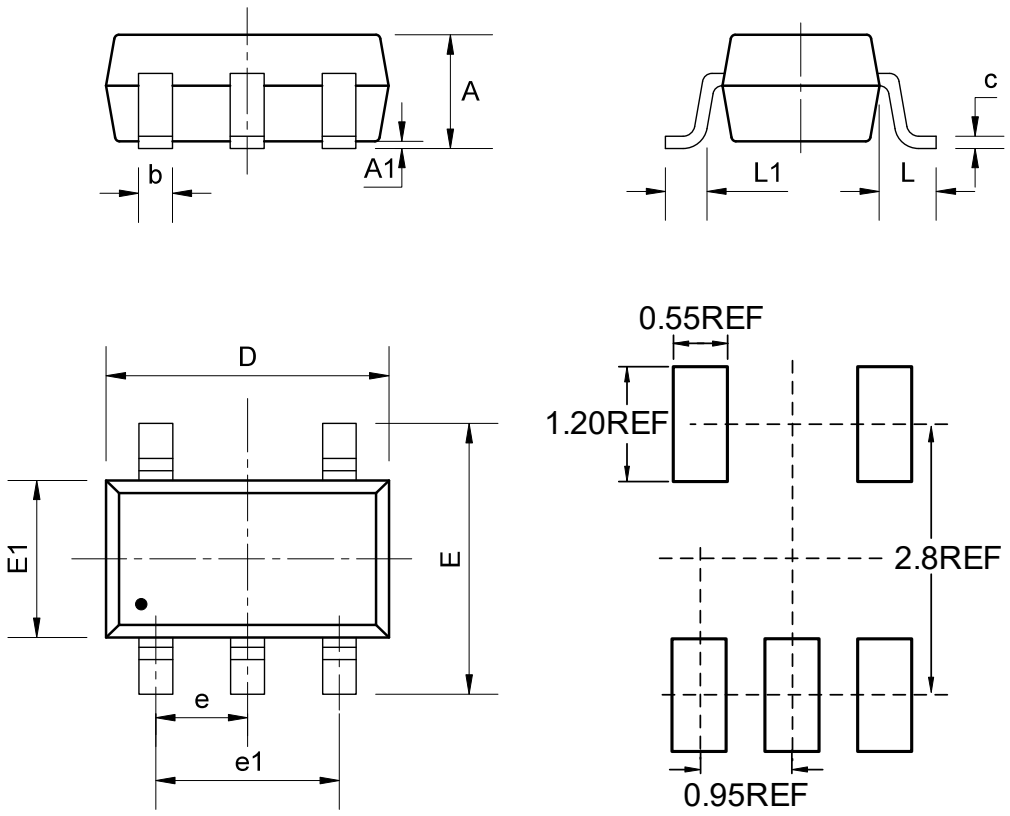


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.05
A1	0	-	0.15
b	0.17	-	0.33
c	0.12	-	0.20
D	2.00	2.10	2.20
e	0.65BSC		
e1	1.30BSC		
E	2.20	2.30	2.40
E1	1.21	1.30	1.35
L	0.50REF		
L1	0.33REF		

SOT23-5(1.6mm × 2.9mm)



COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.25
A1	0	-	0.15
b	0.36	-	0.50
c	0.12	-	0.20
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.60REF		
L1	0.30	0.45	0.60

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-08-20	Preliminary Version	Yu yifan	Tu guozhu	Liu jiaying
1.0	2025-03-29	Official Version	Wang anran	Yang xiaoxu	Liu jiaying
1.1	2025-06-07	Add Packing Option	Yang xiaoxu	Yang xiaoxu	Liu jiaying
1.2	2025-10-15	Update Format	Wang anran	Yang xiaoxu	Liu jiaying