

Single Inverter with Schmitt Trigger

General Description

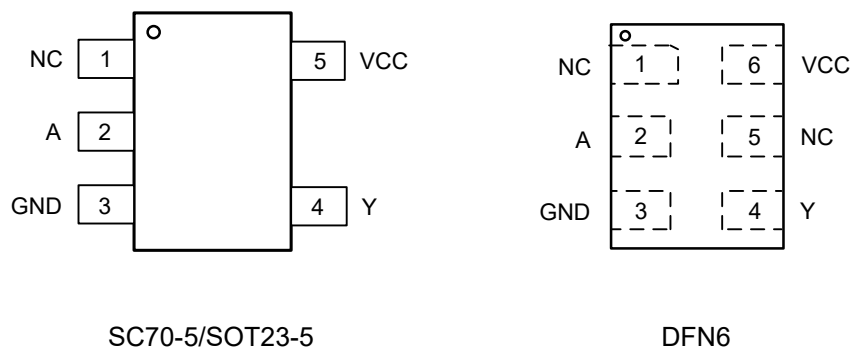
The ETQ74LVC1G14 is an inverter in three tiny footprint packages. The device performs much as LCX multi-gate products in speed and drive.

Features

- $\pm 24\text{mA}$ Sink and Source Output Capability
- Over-Voltage Tolerant Inputs and Outputs
- Chip Complexity: FETs = 20
- Designed for 1.65V to 5.5V V_{CC} Operation
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant.
- Multiple Package Options Automotive AEC-Q100 Grade 1 Qualified
 - Ambient Temperature Range of -40°C to $+125^{\circ}\text{C}$
 - ESD HBM $\pm 4\text{KV}$ PASS
 - ESD CDM $\pm 1\text{KV}$ PASS
 - Latch Up Current to $\pm 100\text{mA}$ PASS
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ETQ74LVC1G14	SC70-5(1.3mm $\times$ 2.1mm)	Tape and Reel, 3K/Reel	1
ETQ74LVC1G14T	SOT23-5(1.6mm $\times$ 2.9mm)	Tape and Reel, 3K/Reel	3
ETQ74LVC1G14Y	DFN6(1.0mm $\times$ 1.5mm)	Tape and Reel, 3K/Reel	1

Pin Configuration



TOP VIEW

Figure1. Pin Configuration

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Pin Function

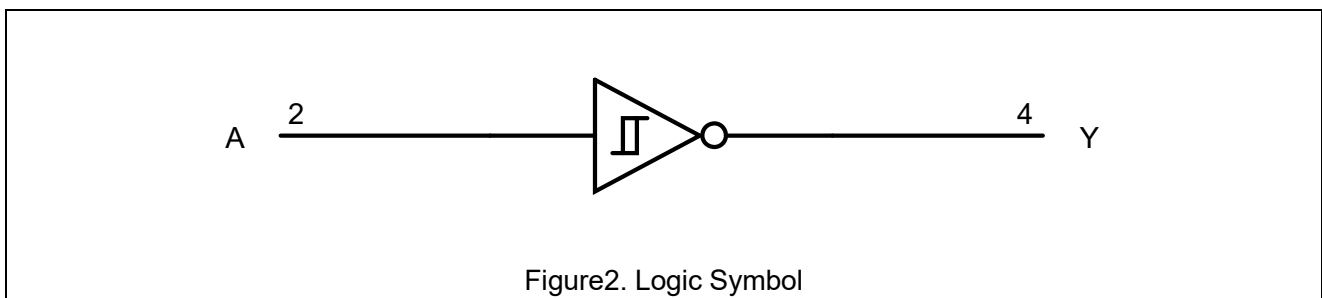
(SC70-5/ SOT23-5)

Pin No.	Pin Name	Function
1	NC	No connect
2	A	Input
3	GND	Ground
4	Y	Output
5	VCC	Supply Voltage

DFN6

Pin No.	Pin Name	Function
1	NC	No connect
2	A	Input
3	GND	Ground
4	Y	Output
5	NC	No Connect
6	VCC	Supply Voltage

Block Diagram



Functional Description

Function Table

Input A	Output Y
L	H
H	L

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Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage(VCC Pin)		-0.5 to 6.5	V
V _I	DC Input Voltage ⁽¹⁾		-0.5 ≤ V _I ≤ 6.5	V
V _O	DC Output Voltage Output in Higher or Low State		-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current V _I < GND		-50	mA
I _{OK}	DC Output Diode Current V _O < GND, V _O > V _{CC}		±50	mA
I _O	DC Output Sink Current		±50	mA
I _{CC}	DC Supply Current per Supply Pin		+100	mA
I _{GND}	DC Ground Current per Supply Pin		-100	mA
T _{STG}	Storage Temperature Range		-65 to 150	°C
T _L	Lead Temperature, Soldering 10 Seconds		260	°C
T _J	Max Junction Temperature		150	°C
V _{ESD}	ESD Classification	Human Body Model ⁽²⁾	±4000	V
		Charged Device Model ⁽³⁾	±1000	
I _{LU}	Max Latch Up Current Above V _{CC} and GND at 125°C ⁽⁴⁾		±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per AEC-Q100-002(JEDEC JS-001);

Note3: CDM tested per AEC-Q100-011(JEDEC JS-002);

Note4: Latch up Current Maximum Rating tested per AEC-Q100-004(JEDEC JESD78F).

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
R _{θJA}	SC70-5	Thermal Characteristics, Thermal Resistance, Junction-to-Air	300	°C/W
	SOT23-5		250	
	DFN6		440	

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage Operating		1.65	5.5	V
	Data Retention		1.5	5.5	
V _{IN}	DC Input Voltage		0	5.5	V
V _{OUT}	DC Output Voltage (High or Low State)		0	5.5	V
T _A	Operating Temperature Range		-40	125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2.5V ± 0.2V	0	20	ns/V
		V _{CC} = 3.0V ± 0.3V	0	10	
		V _{CC} = 5.0V ± 0.5V	0	5	

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Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25 °C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65to1.95 2.3 to 5.5	0.75V _{CC} 0.7V _{CC}			0.75V _{CC} 0.7V _{CC}		V
V _{IL}	Low-Level Input Voltage		1.65to1.95 2.3 to 5.5			0.25V _{CC} 0.3V _{CC}		0.25V _{CC} 0.3V _{CC}	V
V _{OH}	High-Level Output Voltage V _{IN} = V _{IL}	I _{OH} =-100μA	1.65 to 5.5	V _{CC} -0.1	V _{CC}		V _{CC} -0.1		V
		I _{OH} =-3mA	1.65	1.29	1.52		1.29		
		I _{OH} =-8mA	2.3	1.9	2.1		1.9		
		I _{OH} =-12mA	2.7	2.2	2.4		2.2		
		I _{OH} =-16mA	3.0	2.4	2.7		2.4		
		I _{OH} =-24mA	3.0	2.3	2.5		2.3		
		I _{OH} =-32mA	4.5	3.8	4.0		3.8		
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IH}	I _{OL} =100μA	1.65 to 5.5		0.0	0.1		0.1	V
		I _{OL} =3mA	1.65		0.08	0.24		0.24	
		I _{OL} =8mA	2.3		0.20	0.3		0.3	
		I _{OL} =12mA	2.7		0.22	0.4		0.4	
		I _{OL} =16mA	3.0		0.28	0.4		0.4	
		I _{OL} =24mA	3.0		0.38	0.55		0.55	
		I _{OL} =32mA	4.5		0.42	0.55		0.55	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5		±0.1			±1.0	μA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or V _{OUT} = 5.5 V	0			1		10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = 5.5 V or GND	5.5					10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC Electrical Characteristics

$t_r = t_f = 5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\ \Omega$.

Symbol	Parameter	Condition	$V_{CC}(\text{V})$	$T_A = 25\ ^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay (Figure3 and 4)	$R_L = 1\text{M}\Omega$ $C_L = 15\text{pF}$	1.65	2.0	5.3	11.4	2.0	12.0	ns
			1.8	2.0	4.4	9.5	2.0	10.0	
		$R_L = 1\text{M}\Omega$ $C_L = 15\text{pF}$	2.5 ± 0.2	0.2	3.5	6.5	0.8	7.0	
		$R_L = 1\text{M}\Omega$ $C_L = 15\text{pF}$	3.3 ± 0.3	0.8	2.1	4.5	0.5	4.7	
		$R_L = 500\Omega$ $C_L = 50\text{pF}$		1.2	2.9	5.5	1.5	5.2	
		$R_L = 1\text{M}\Omega$ $C_L = 15\text{pF}$	5.0 ± 0.5	0.5	1.8	3.9	0.5	4.1	
		$R_L = 500\Omega$ $C_L = 50\text{pF}$		0.8	2.4	4.3	0.8	4.5	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5\text{ V}$, $V_I = 0\text{ V}$ or V_{CC}	>2.5	pF
C_{PD}	Power Dissipation Capacitance (5)	10 MHz, $V_{CC} = 3.3\text{ V}$, $V_I = 0\text{ V}$ or V_{CC}	9	pF
		10 MHz, $V_{CC} = 5.5\text{ V}$, $V_I = 0\text{ V}$ or V_{CC}	11	

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

AC Test Circuit

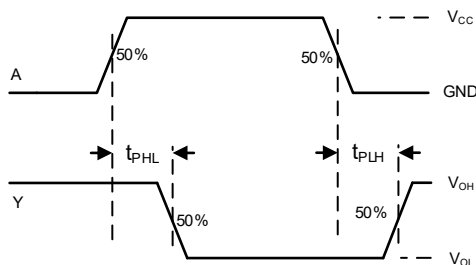


Figure3. Switching Waveform

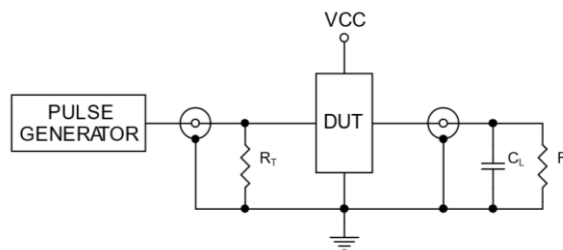
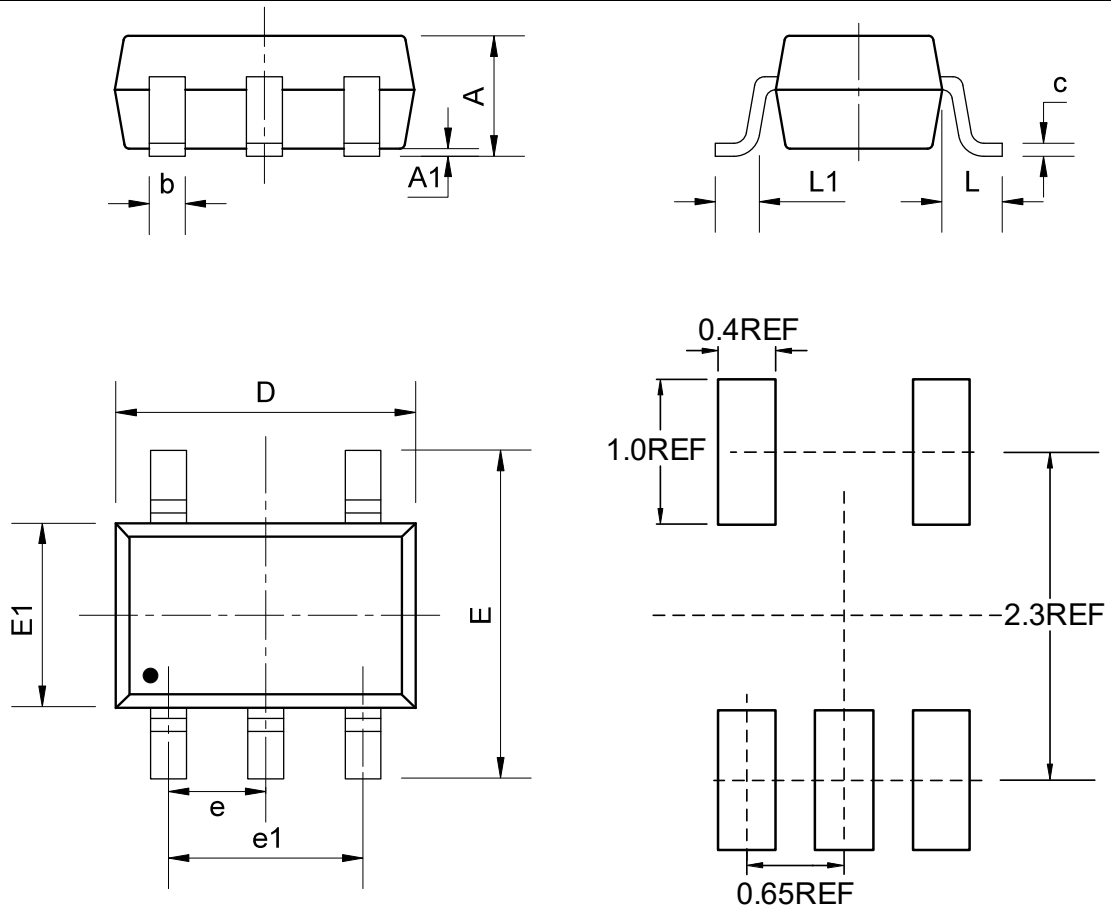


Figure4. Test Circuit

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Package Dimension

SC70-5(1.3mm × 2.1mm)



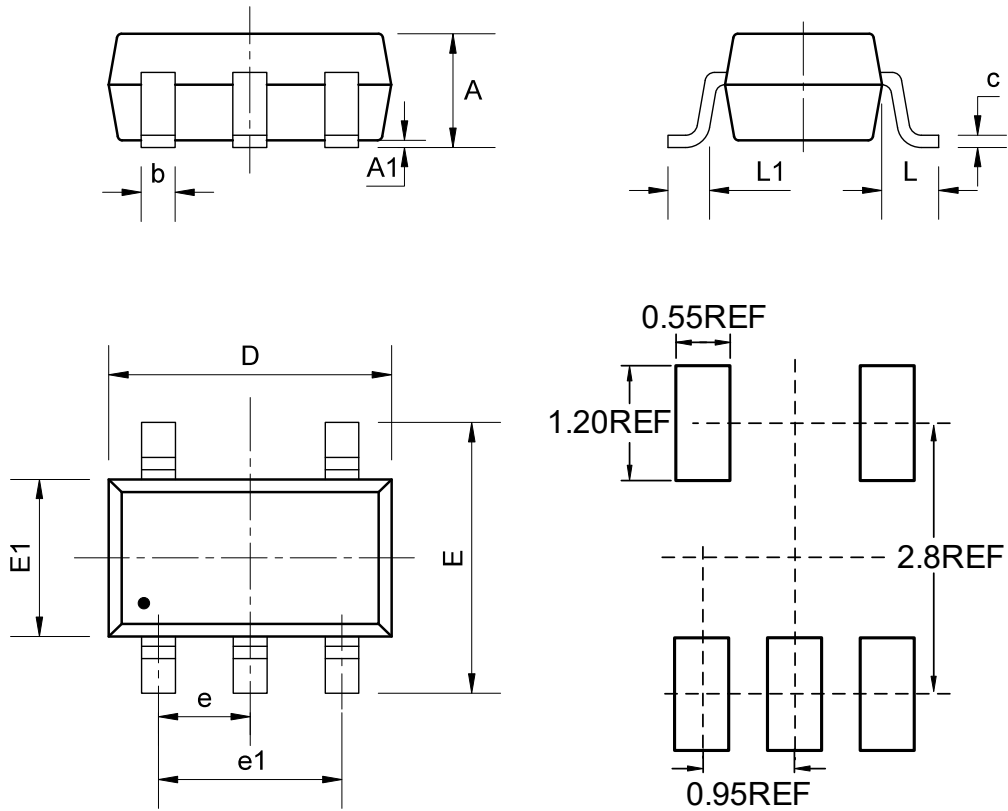
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.05
A1	0	-	0.15
b	0.17	-	0.33
c	0.12	-	0.20
D	2.00	2.10	2.20
e	0.65BSC		
e1	1.30BSC		
E	2.20	2.30	2.40
E1	1.21	1.30	1.35
L	0.50REF		
L1	0.33REF		

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SOT23-5(1.6mm × 2.9mm)



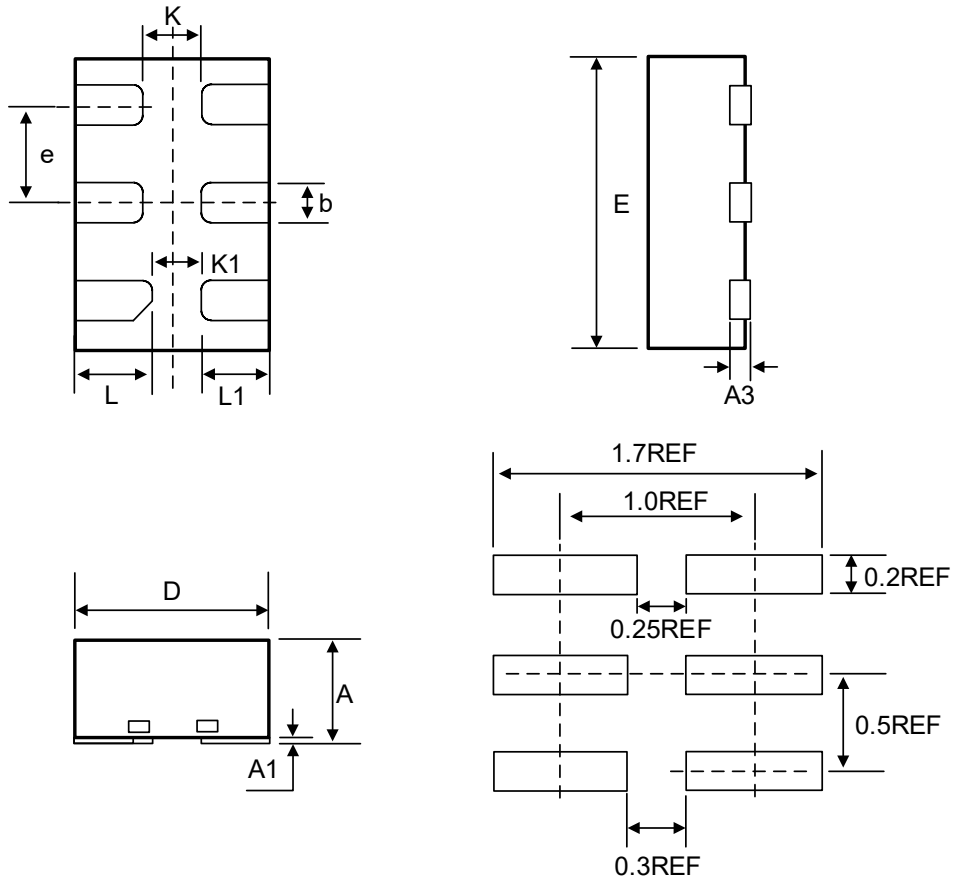
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.25
A1	0	-	0.15
b	0.36	-	0.50
c	0.12	-	0.20
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.60REF		
L1	0.30	0.45	0.60

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DFN6 (1.0mm × 1.5mm)



COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	0.34	0.37	0.40
A1	0	0.02	0.05
A3	0.10REF		
b	0.10	0.15	0.20
D	0.95	1.00	1.05
E	0.95	1.00	1.05
e	0.30	0.35	0.40
H	0.10REF		
K	0.15	--	--
L	0.35	0.40	0.45
L1	0.075REF		

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Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2017-07-19	Original Version	Ma Yong jian	Ma Yong jian	Liu Jia Ying
1.1	2019-07-18	Update AC Table and Device Information	Ma Yong jian	Ma Yong jian	Liu Jia Ying
1.2	2021-06-25	Update Cpd in AC Table and Lin/Loff/Lcc in Dc Table	Ma Yong jian	Ma Yong jian	Liu Jia Ying
1.3	2022-01-18	Add SC70-5 Recommended Pad Layout	Shi bo	Shi bo	Zhu junli
1.4	2022-06-10	ESD Update	Shi bo	Shi bo	Zhu junli
1.5	2022-10-14	Update format and Thermal Characteristics	Wu han	Shi bo	Zhu junli
1.6	2023-11-29	Update Typeset /ESD	Shi bo	Shi bo	Shi bo
1.7	2025-06-07	Add Packing Option	Yang xiaoxu	Yang xiaoxu	Liu jiaying
1.8	2025-10-15	Update Format	Wang anran	Yang xiaoxu	Liu jiaying