ET61092 - Constant Current LED Matrix Driving Circuit

General Description

ET61092 is a dedicated constant-current LED matrix driver IC, supporting display arrays of up to 16×9 pixels. It utilizes a two-wire serial communication interface and incorporates multiple internal registers for configuring diverse display effects. Each pixel supports 256 levels of grayscale brightness adjustment. The device is primarily employed in driving display panels for home appliance applications and is available in QFN32 or LQFP32 package options.

Features

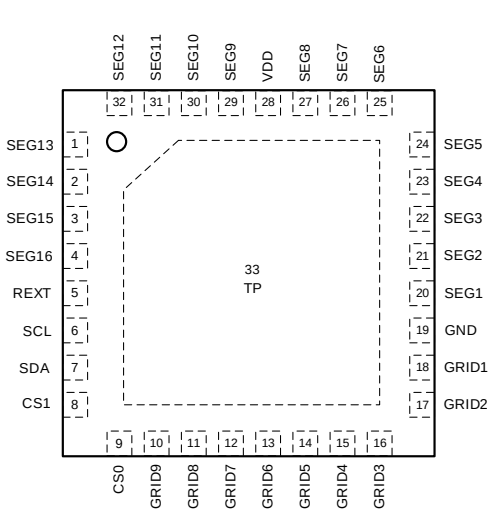
- Power supply voltage range: 2.7～5.5V
- Maximum application dot matrix: 16 x 9, maximum driving capacity: 144 LEDs
- 16-channel constant current drive, maximum output current: 30mA (under internal resistance condition)
- Overall current supports 64-level adjustment
- Each point supports 256-level brightness adjustment
- Communication interface: 2-wire serial interface
- Built-in clock module
- Built-in power-on reset module
- Built-in sleep mode
- Built-in blanking function
- Product name and packaging form:

Part No.	Package	Packing Option	MSL
ET61092Y	QFN32(5.0mm × 5.0mm)	Tape and Reel, 3K/Reel	3
ET61092Q	LQFP32(7.0mm × 7.0mm)	Tape and Reel, 3K/Reel	3

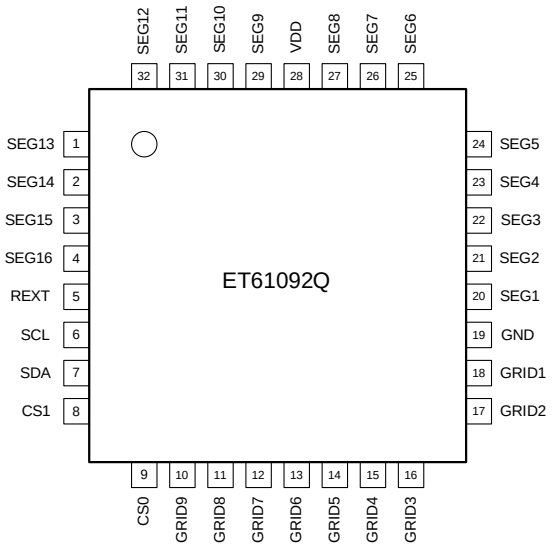
Applications

- Household applications, Toy display
- Smart portable devices, Smart audio applications

Pin Configuration



ET61092Y(QFN32)



ET61092Q(LQFP32)

Figure 1. Pin Configuration (Top View)

Pin Function

Pin No. QFN32/LQFP32	Pin Name	Pin Function
1~4,20~27,29~32	SEG1~SEG16	Segment output port, connect LED positive
5	REXT	Connect external resistor to GND set the output current of all output channels.; it is recommended to use a minimum value of 2kΩ
6	SCL	Clock input
7	SDA	Data input
8	CS1	Communication interface slave address configuration port 1
9	CS0	Communication interface slave address configuration port 0
10~18	GRID1~GRID9	Grid output port, connected to LED negative
19	GND	Ground pad
28	VDD	Power supply
33 (QFN32)	TP	Thermal Pad, Connect to GND or floating

Block Diagram

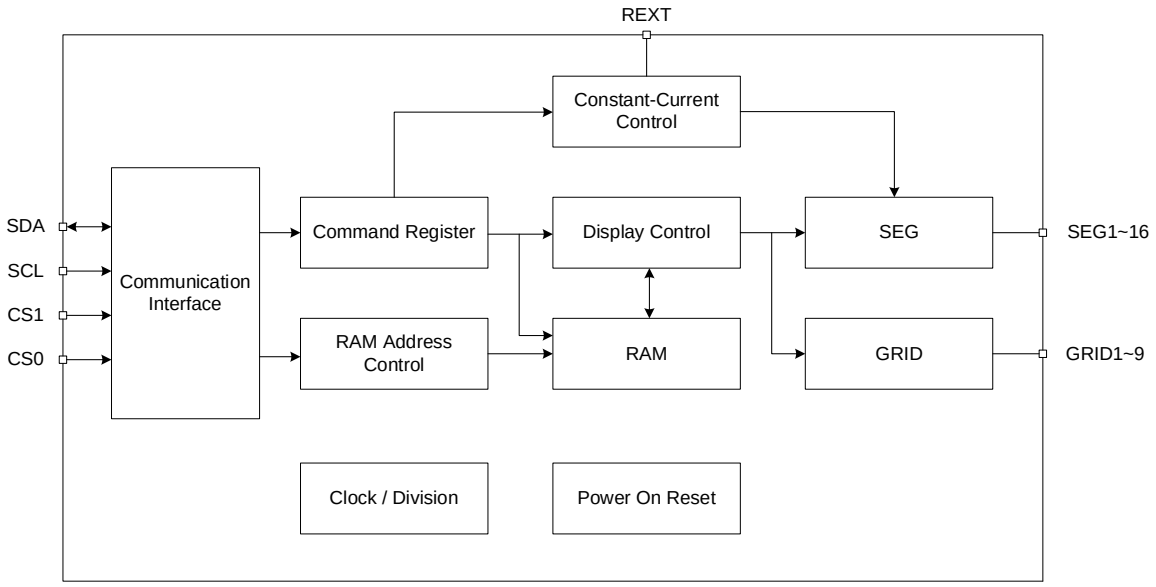


Figure 2. Function Block Diagram

Functions Description

Communication Protocol

Bus Interface

The MCU transmits data to ET61092 through the SDA and SCL ports. The SDA and SCL form a two-wire serial communication interface, transmitting data in the form of data packets, and each data packet requires data verification. An upper pull-up resistor needs to be connected to the power terminal. The slave address is matched through the CS1 and CS0 ports.

Data Validity

Each byte of the data line consists of 8 bits. The first data transmitted is the MSB.

When the SCL signal is at a high level, the data on the SDA port is stable and valid. Only when the SCL signal is at a low level can the level of the SDA port be changed.

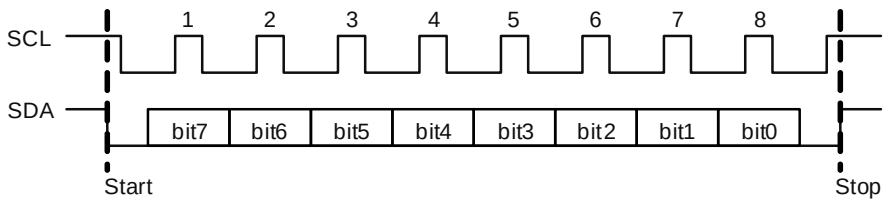


Figure 3. Data Transmission Format

Instruction Data Packet

Byte1	Byte2	Byte3	Byte4
0x5A	0xFF	Instruct	Check code

Note： Byte1 and Byte2 are fixed data, and the instruction data packet check code is the lower 8 bits of the sum of the first 3 bytes of the data.

Instruct								
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Description**
0	0	CS1	CS0	0	0	0	1	Write the configuration register
				0	0	1	0	Write display data
				0	1	0	0	Update display content
				0	1	1	1	Read flag bit
				1	0	0	0	Refresh display
				1	0	1	1	Global reset
				1	1	0	1	Wake up mode
				1	1	1	0	Sleep mode

Note1： When writing read flag bits, refreshing display, performing global reset, or issuing sleep mode instructions through the command data packets, it is necessary to turn on the corresponding enable switch in register 4; otherwise, the operation will be invalid.

Note2： The wake-up instruction or the selection of configuration register 4 to disable entering the sleep mode (SLEEP = 0) can both exit the sleep mode; the global reset instruction can also exit the sleep mode, while resetting the configuration register and the display address pointer, and the RAM data will remain unchanged.

Register data packet

Byte1	Byte2	Byte3	Byte4	Byte5
Register 1	Register 2	Register 3	Register 4	Check code

Note： The checksum of the register data packet is the lower 8 bits of the sum of the first 4 bytes of the data.

Register 1					
Bit	**Bit name**	**Default**	**Access**	**Description**	
[7:6]	-	00	-	Reserved	
[5:0]	CUR	000000	W	SEGn port outputs continuous current I_{SEG}(n=1~16)	
				000000	6.375mA (Use internal resistance) 9.52mA (Use 2kΩ external resistor)
				.....	.....
				111111	30mA (Use internal resistance) 43mA (Use 2kΩ external resistor)

Register 2					
Bit	**Bit name**	**Default**	**Access**	**Description**	
[7]	OSC	0	W	Internal/External Clock Selection Enable	
				0	Using internal clock
				1	Using SCL input clock
[6]	-	0	-	Reserved	
[5:2]	G_N	0000	W	Selection of Scan Line	
				0000	1 Scan Line (GRID1)
				0001	2 Scan Line (GRID1~2)
				.....	.....
				0111	8 Scan Line (GRID1~8)
				1000~1111	9 Scan Line (GRID1~9)
[1]	TEST	0	W	Enable test mode	
				0	Normal working mode
				1	Test mode
[0]	UP	0	W	Update display content	
				0	Manual update
				1	Auto update

Register 3					
Bit	**Bit name**	**Default**	**Access**	**Description**	
[7]	TP1	0	W	Over-temperature protection 1	
				0	Enable Over-temperature Protection 1. When the IC temperature exceeds 125°C, the SEG output current changes to 2/3 of the originally set value.
				1	Disable over-temperature protection 1
[6]	RES	0	W	Internal/External Resistance setting constant current selection enable	
				0	Using internal resistance
				1	Using external resistor of the REXT port
[5:4]	FR	00	W	Frame rate setting (Under the 9 Scan Line condition)	
				00	400Hz
				01	800Hz
				10	1600Hz
				11	3200Hz
[3]	DON	0	W	SEG display switch	

				0	SEG display disable
				1	SEG display enable
[2]	GS	0	W	Blanking function switch	
				0	SEG blanking function disable
				1	SEG blanking function enable
[1:0]	DT	00	W	Grid dead zone time setting	
				00	4 system clock
				01	8 system clock
				10	16 system clock
				11	24 system clock

Register 4					
Bit	**Bit name**	**Default**	**Access**	**Description**	
[7]	-	0	-	Reserved	
[6]	SLEEP	0	W/R	Sleep mode enable	
				0	Sleep mode enable
				1	Enable sleep mode through the command data packet (sleep mode)
[5:2]	-	0000	-	Reserved	
[1]	TP2	0	W/R	Over-temperature protection 2	
				0	Enable Over-temperature Protection 2. When the IC temperature exceeds 150℃, turn off the SEG output.
				1	Disable Over-temperature protection 2
[0]	-	0	-	Reserved	

Display data packets

Byte1	Byte2	Byte3	·····	Byte(n)	Byte(n+1)
Display data 1	Display data 2	Display data 3	·····	Display data (n)	Check code

Note1： The length of the display data packet is related to the number of scan lines. The length of the display data packet is 16 times the number of scan lines plus 1 (for the check code), and the RAM address always starts from 0x00. For example, for 9 scans, the length of the display data packet is 16*9 + 1 = 145 bytes. When the written display data length does not match the length of the display data packet, the written data will be invalid.

Note2： The displayed data packet check code represents the lower 8 bits of the sum of all the input displayed data.

LEDn PWM (n=1~144)				
RAM Addr	**Bit**	**Bit Name**	**Description**	
00H~8FH	[7:0]	ledn_pwm	LEDn PWM (n=1~144)	
			00000000b	0/255 duty cycle
			00000001b	1/255 duty cycle
			……	……
			11111110b	254/255 duty cycle
			11111111b	255/255 duty cycle

LED dot matrix diagram

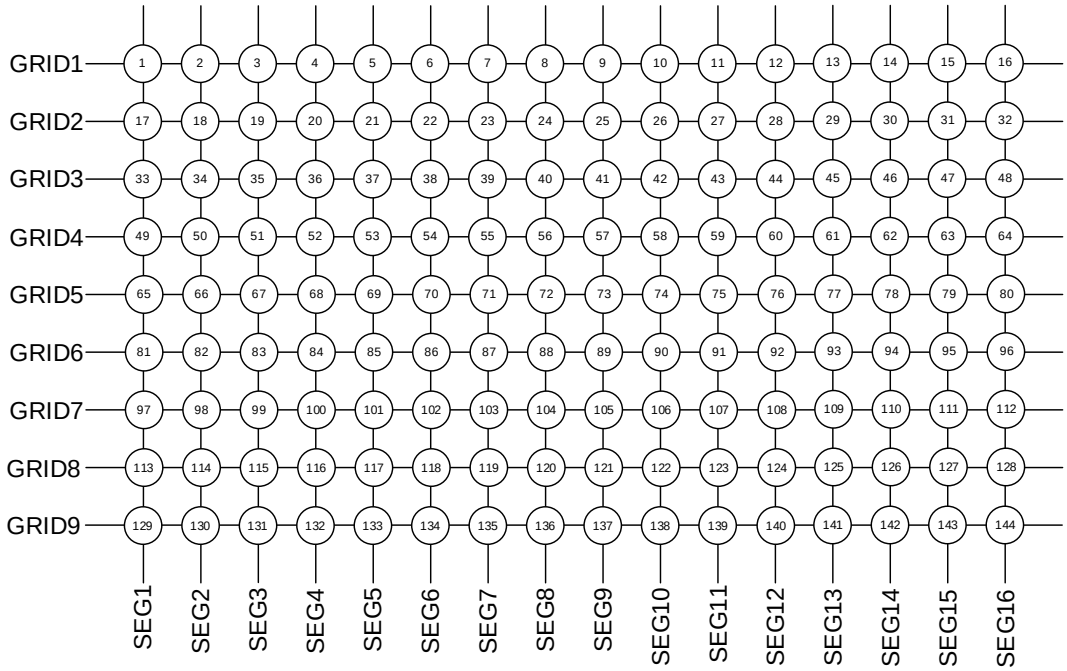


Figure 4. LED dot matrix diagram

Note： The PWM data corresponding to point 1 in the figure is as shown in the table as LED1PWM. The PWM data corresponding to point 144 in the figure is as shown in the table as LED144PWM. The same pattern applies to other points.

RAM Address and LED Matrix Correspondence Table

ADDR	Description	ADDR	Description	ADDR	Description	ADDR	Description
00H	LED1PWM	01H	LED2PWM	02H	LED3PWM	03H	LED4PWM
04H	LED5PWM	05H	LED6PWM	06H	LED7PWM	07H	LED8PWM
08H	LED9PWM	09H	LED10PWM	0AH	LED11PWM	0BH	LED12PWM
0CH	LED13PWM	0DH	LED14PWM	0EH	LED15PWM	0FH	LED16PWM
10H	LED17PWM	11H	LED18PWM	12H	LED19PWM	13H	LED20PWM
14H	LED21PWM	15H	LED22PWM	16H	LED23PWM	17H	LED24PWM
18H	LED25PWM	19H	LED26PWM	1AH	LED27PWM	1BH	LED28PWM
1CH	LED29PWM	1DH	LED30PWM	1EH	LED31PWM	1FH	LED32PWM
20H	LED33PWM	21H	LED34PWM	22H	LED35PWM	23H	LED36PWM
24H	LED37PWM	25H	LED38PWM	26H	LED39PWM	27H	LED40PWM
28H	LED41PWM	29H	LED42PWM	2AH	LED43PWM	2BH	LED44PWM
2CH	LED45PWM	2DH	LED46PWM	2EH	LED47PWM	2FH	LED48PWM
30H	LED49PWM	31H	LED50PWM	32H	LED51PWM	33H	LED52PWM
34H	LED53PWM	35H	LED54PWM	36H	LED55PWM	37H	LED56PWM
38H	LED57PWM	39H	LED58PWM	3AH	LED59PWM	3BH	LED60PWM
3CH	LED61PWM	3DH	LED62PWM	3EH	LED63PWM	3FH	LED64PWM
40H	LED65PWM	41H	LED66PWM	42H	LED67PWM	43H	LED68PWM
44H	LED69PWM	45H	LED70PWM	46H	LED71PWM	47H	LED72PWM
48H	LED73PWM	49H	LED74PWM	4AH	LED75PWM	4BH	LED76PWM
4CH	LED77PWM	4DH	LED78PWM	4EH	LED79PWM	4FH	LED80PWM
50H	LED81PWM	51H	LED82PWM	52H	LED83PWM	53H	LED84PWM
54H	LED85PWM	55H	LED86PWM	56H	LED87PWM	57H	LED88PWM
58H	LED89PWM	59H	LED90PWM	5AH	LED91PWM	5BH	LED92PWM
5CH	LED93PWM	5DH	LED94PWM	5EH	LED95PWM	5FH	LED96PWM
60H	LED97PWM	61H	LED98PWM	62H	LED99PWM	63H	LED100PWM
64H	LED101PWM	65H	LED102PWM	66H	LED103PWM	67H	LED104PWM
68H	LED105PWM	69H	LED106PWM	6AH	LED107PWM	6BH	LED108PWM
6CH	LED109PWM	6DH	LED110PWM	6EH	LED111PWM	6FH	LED112PWM
70H	LED113PWM	71H	LED114PWM	72H	LED115PWM	73H	LED116PWM
74H	LED117PWM	75H	LED118PWM	76H	LED119PWM	77H	LED120PWM
78H	LED121PWM	79H	LED122PWM	7AH	LED123PWM	7BH	LED124PWM
7CH	LED125PWM	7DH	LED126PWM	7EH	LED127PWM	7FH	LED128PWM
80H	LED129PWM	81H	LED130PWM	82H	LED131PWM	83H	LED132PWM
84H	LED133PWM	85H	LED134PWM	86H	LED135PWM	87H	LED136PWM
88H	LED137PWM	89H	LED138PWM	8AH	LED139PWM	8BH	LED140PWM
8CH	LED141PWM	8DH	LED142PWM	8EH	LED143PWM	8FH	LED144PWM

Note： Each address contains 8 bits of data, corresponding to the PWM level of that point (256 levels).

Workflow

1. Set the instruction 0x01 (write the configuration register, the slave addresses CS1 and CS0 are both grounded at 0), and the instruction data packet data is 0x5A, 0xFF, 0x01, 0x5A (0x5A is the check code);
2. Set the register data packet data. The register data packet data consists of four register data values plus a checksum.
3. Set the command 0x02 (write display data, with the slave addresses CS1 and CS0 grounded at 0), and the command data packet data is 0x5A, 0xFF, 0x02, 0x5B (0x5B is the check code);
4. Set the display of data packets to show the data packet data as n pieces of displayed data plus a check code.

Note1： 0x5A and 0xFF are the fixed data of the instruction data packet.

Note2： When writing data, there must be no redundant clocks between data packets and the data must be written continuously.

Note3： The length of the displayed data packets should match the number of scanned lines. Writing too much or too little data will not enable effective display of the data.

Absolute Maximum Ratings

Symbol	Characteristic	Rating	Unit
V_{DD}	Supply Voltage	-0.3~6.0	V
V_I	Logic Input Voltage	-0.3~V_{DD}+0.3	V
θ_{JA}	Thermal Resistance (QFN32,5×5)	41	°C/W
	Thermal Resistance (LQFP32)	89	
T_{JMAX}	Max Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65～150	°C
V_{ESD}	HBM	±2.0	KV
	CDM	±1.0	KV

Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	2.7	5.0	5.5	V
V_{IH}	High Level Input Voltage	3.0	-	V_{DD}	V
V_{IL}	Low Level Input Voltage	0	-	1.5	V
T_A	Operating Temperature	-40	-	+85	°C

Electrical Characteristics

(Unless otherwise specified，T_A = 25°C，V_{DD}= 5V，GND= 0V)

Symbol	Characteristic	Test Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		2.7	5.0	5.5	V
I_{SEG}	High Level Output Current	V_{SEGn} = 4V, I[5:0] = 111111	-28	-30	-32	mA
I_{GRID}	Low Level Output Current	V_{GRIDn} = 0.4V	500			mA
V_{IH}	High Level Input Voltage	SCL, SDA	3.0		V_{DD}	V
V_{IL}	Low Level Input Voltage	SCL, SDA	0		1.5	V
I_{DD}	Dynamic current Dissipation	No load, Display off			5	mA
I_{SLEEP}	Sleep current	Sleep mode			300	uA

Two-line communication timing characteristics

(Unless otherwise specified，T_A = 25°C，V_{DD}= 5V，GND= 0V)

Symbol	Test Condition	Min	Typ	Max	Unit
F_{SCL}	SCL Clock Frequency	-	-	1	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	-	0.5	-	μs
$t_{HD:STA}$	Hold Time (Repeated) START Condition	-	0.26	-	μs
t_{LOW}	Low Period of SCL Clock	-	0.5	-	μs
t_{HIGH}	HIGH Period of SCL Clock	-	0.26	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	-	0.26	-	μs
$t_{HD:DAT}$	Data Hold Time	-	0	-	μs
$t_{SU:DAT}$	Data Setup Time	-	50	-	ns
t_R	Data Hold Time2	-	-	300	ns
t_F	Data Hold Time2	-	-	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.26		μs

Note: Cb=total capacitance of one bus line in PF unit.

Interface Timing Waveform

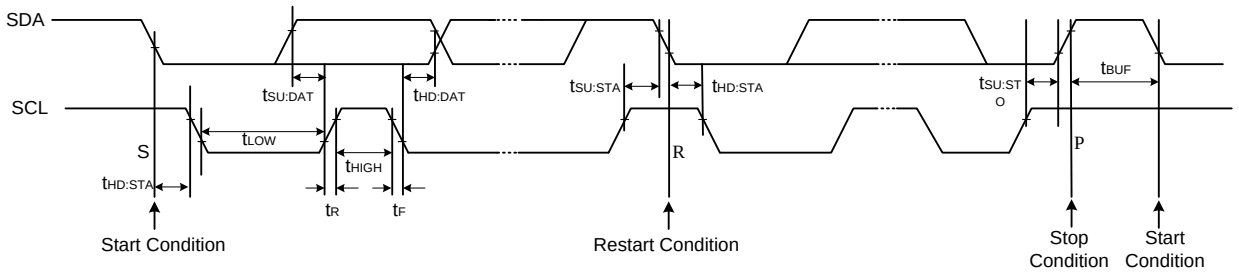


Figure 5. I²C Timing Waveform

Application circuit

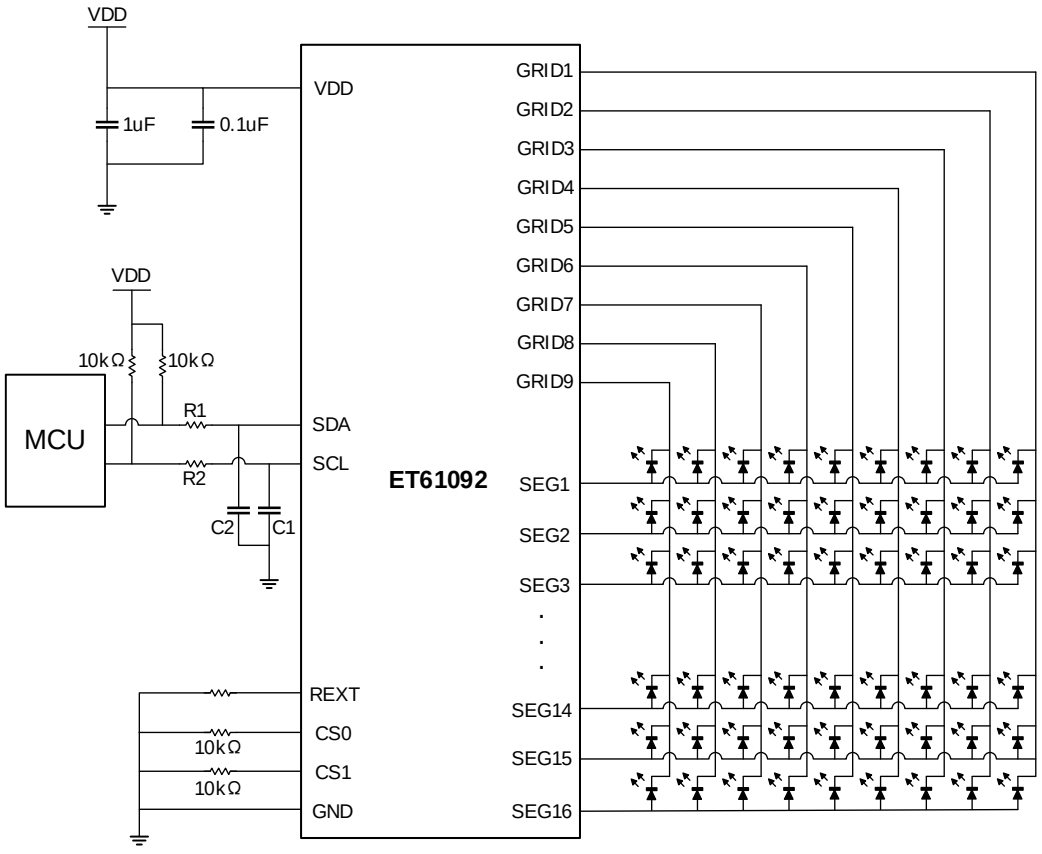


Figure 6. Application Circuit

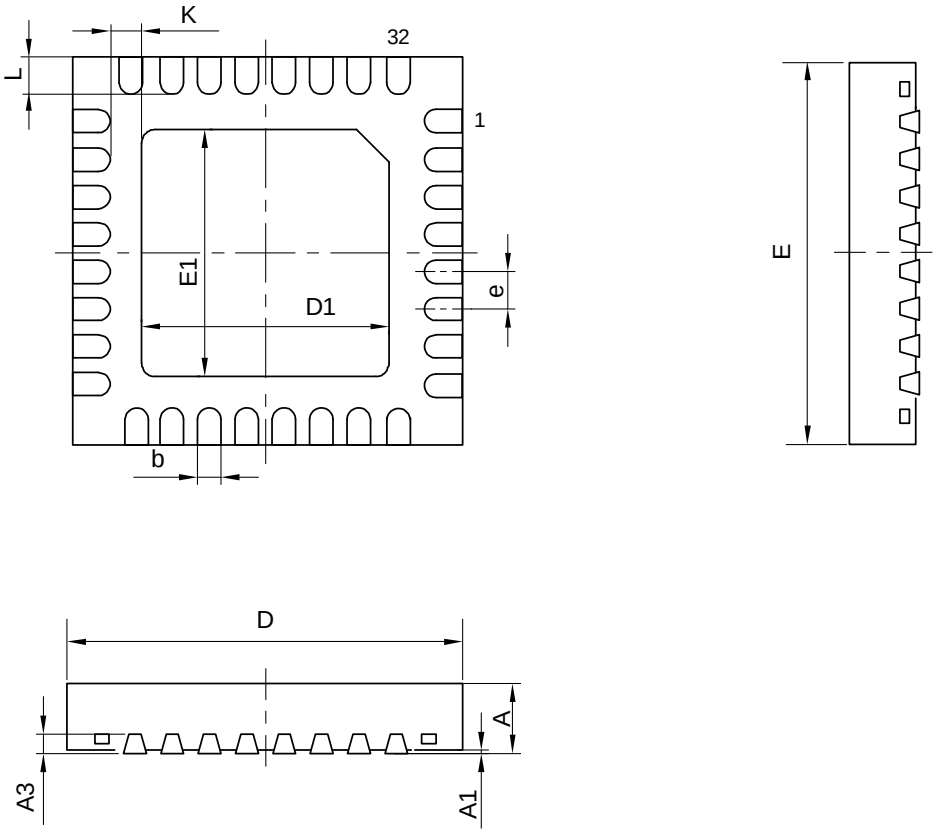
Note： This application diagram is for reference only.

It is recommended that the power filter capacitor be placed as close as possible to the VDD pin;

Adding RC filtering to the communication port can enhance the anti-interference capability, and it should be placed as close as possible to the chip end. The values of the resistors and capacitors (R1 = R2 = 100Ω, C1 = C2 = 100pF) can be adjusted according to the actual anti-interference requirements and verification results.

Package Dimension

QFN32(5.0mm × 5.0mm)

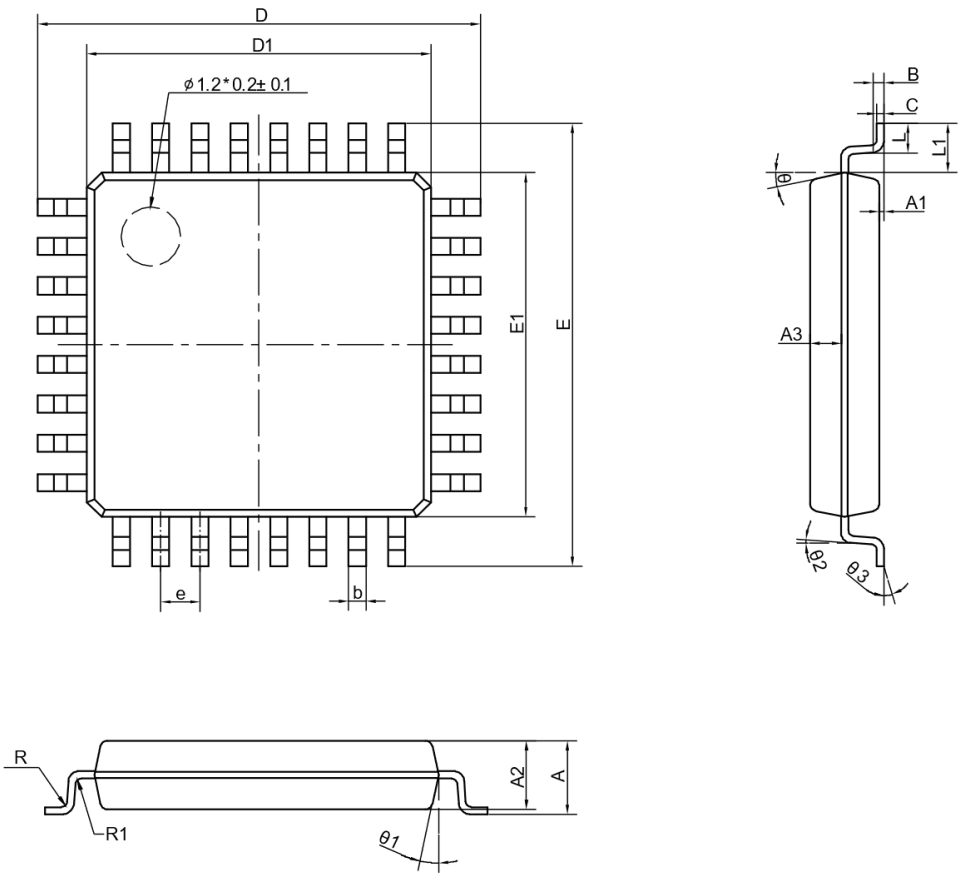


COMMON DIMENSIONS

(Units : mm)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	--	0.05
A3		0.203REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D1	3.30	3.40	3.50
E1	3.30	3.40	3.50
e		0.50TYP	
K	0.20	--	--
L	0.32	0.40	0.48

LQFP32



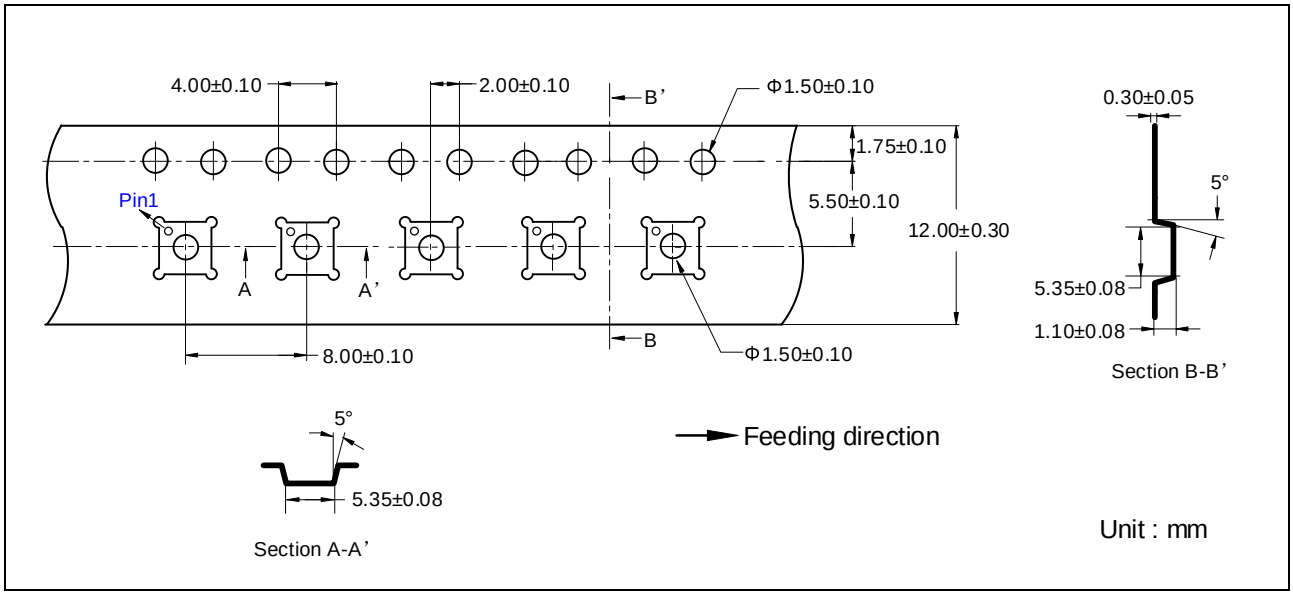
COMMON DIMENSIONS

(Units : mm)

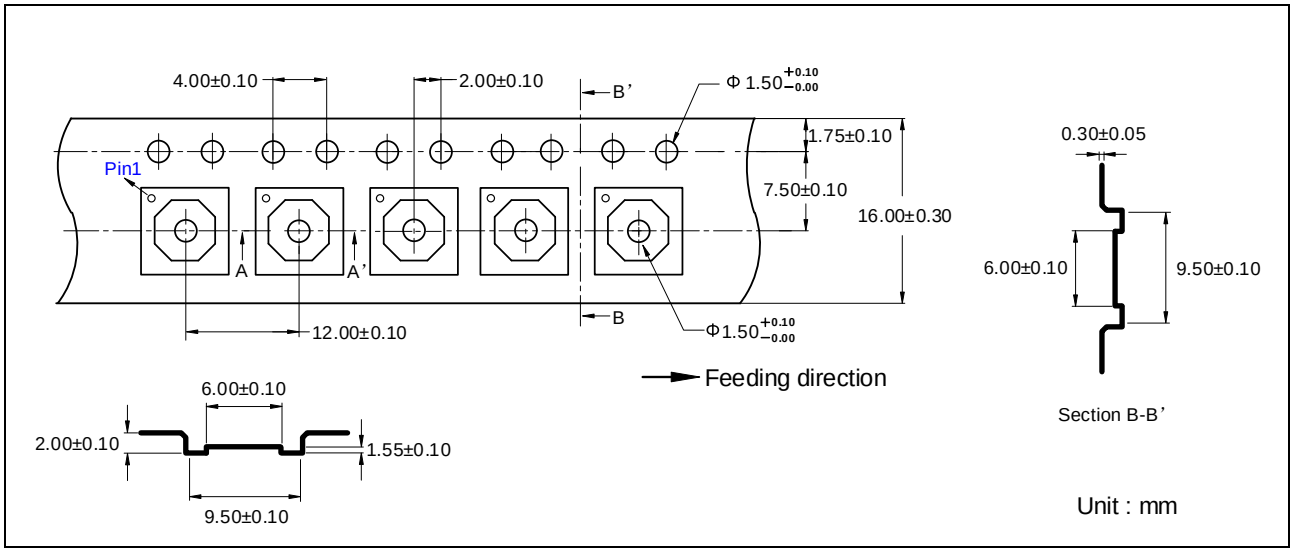
SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A	--	1.60	E1	6.90	7.10
A1	0.05	0.15	e	0.80TYP	
A2	1.35	1.45	L	0.50	0.80
A3	0.64TYP		L1	1.00BSC	
B	0.25TYP		θ	12° TYP	
b	0.32	0.43	θ1	12° TYP	
C	0.127	0.16	θ2	4° TYP	
D	8.80	9.20	θ3	0° ~ 8°	
D1	6.90	7.10	R	0.15TYP	
E	8.80	9.20	R1	0.12TYP	

Tape Information

QFN32(5.0mm × 5.0mm)



LQFP32



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-10-20	Original Version	Tian Qi He	Li Chen Xuan	Liu Jia Ying