16-bit Constant Current LED Sink Driver

General Description

ET6024 is designed for LED displays. ET6024 contains a serial buffer and data latches which convert serial input data into parallel output format. At ET6024 output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of V_F variations.

ET6024 provides users with great flexibility and device performance while using ET6024 in their system design for LED display applications, e.g. LED panels. Users may adjust the output current from 3mA to 45mA through an external resistor, R_{EXT}, which gives users flexibility in controlling the light intensity of LEDs. ET6024 guarantees to endure maximum 20V at the output port. The high clock frequency, 25MHz, also satisfies the system requirements of high volume data transmission.

Features

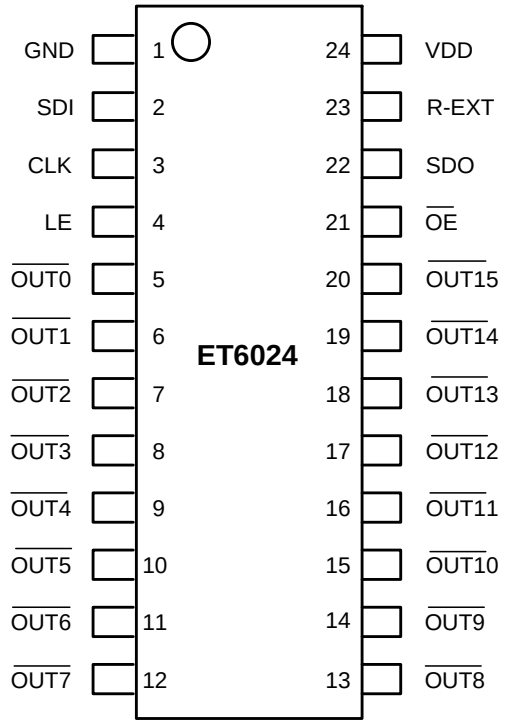
- 16 constant-current output channels
- Constant output current invariant to load voltage change
- Excellent output current accuracy:
- Current accuracy

Current Accuracy		Conditions
Between Channels	Between ICs	
<±3%	<±6%	I_{OUT} =3mA～30mA@V_{DS}=0.8V,V_{DD}=3.3V I_{OUT} =3mA～45mA@V_{DS}=0.8V,V_{DD}=5.0V

- Output current adjusted through an external resistor
- Constant output current range: 3～45mA
- Fast response of output current,
- $\overline{OE}$ (min) is 40ns (V_{DD}= 3.3V)
- 25MHz clock frequency
- Schmitt trigger input
- Supply voltage：3.3V～5.5V
- Part No. and package:

Part No.	Package	Size
ET6024S	SSOP24-3	6mm x 13mm
ET6024SN	SSOP24-2	3.9mm x 8.6mm

Pin Assignments

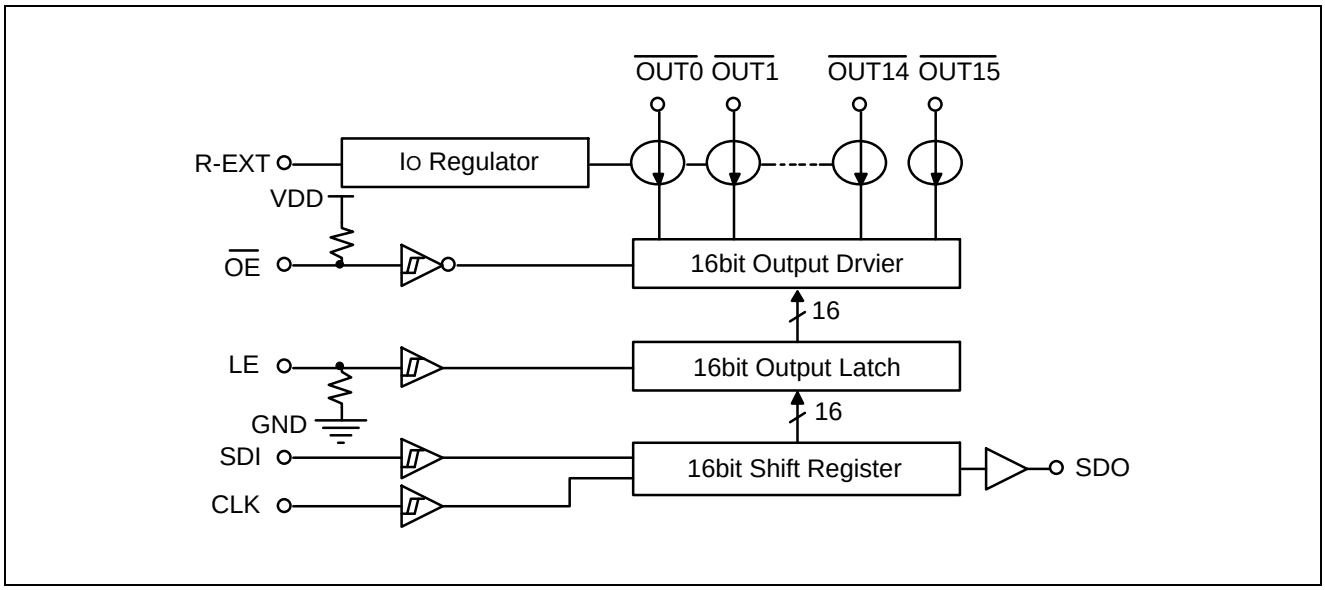


TOP VIEW

Pin. Function

No.	Pin Name	Function
1	GND	Ground terminal for control logic and current sink.
2	SDI	Serial-data input to the shift register.
3	CLK	Clock input terminal for data shift on rising edge.
4	LE	Data strobe input terminal. Serial data is transferred to the output latch when LE is high. The data is latched when LE goes low.
5～20	$\overline{OUT0}$ ～ $\overline{OUT15}$	Constant current output terminals.
21	$\overline{OE}$	Output enable terminal. When $\overline{OE}$ (active) low, the output drivers are enabled; when $\overline{OE}$ high, all output drivers are turned OFF (blanked).
22	SDO	Serial-data output to the following SDI of next driver IC.
23	R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels.
24	VDD	5V supply voltage terminal

Block Diagram



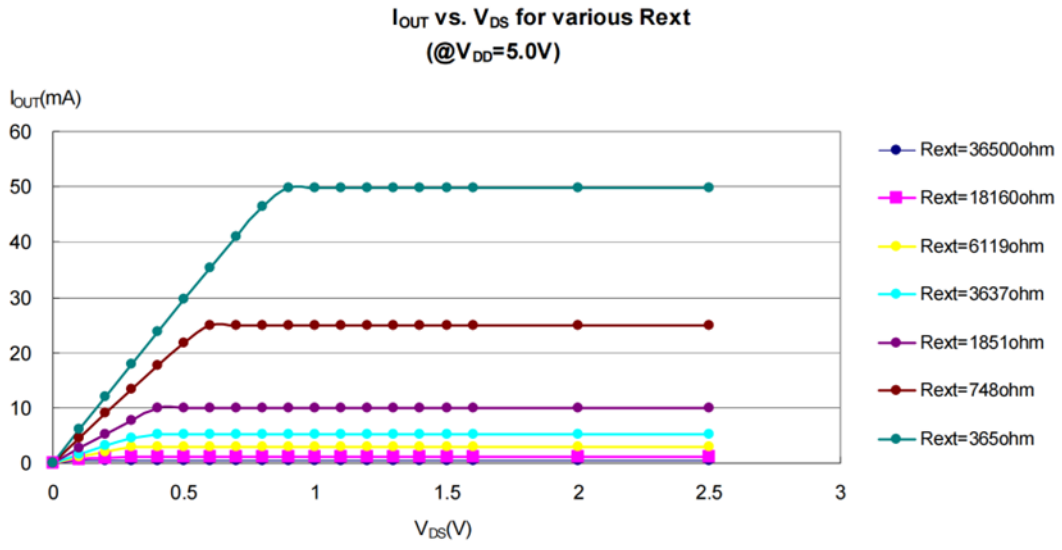
Functional Description

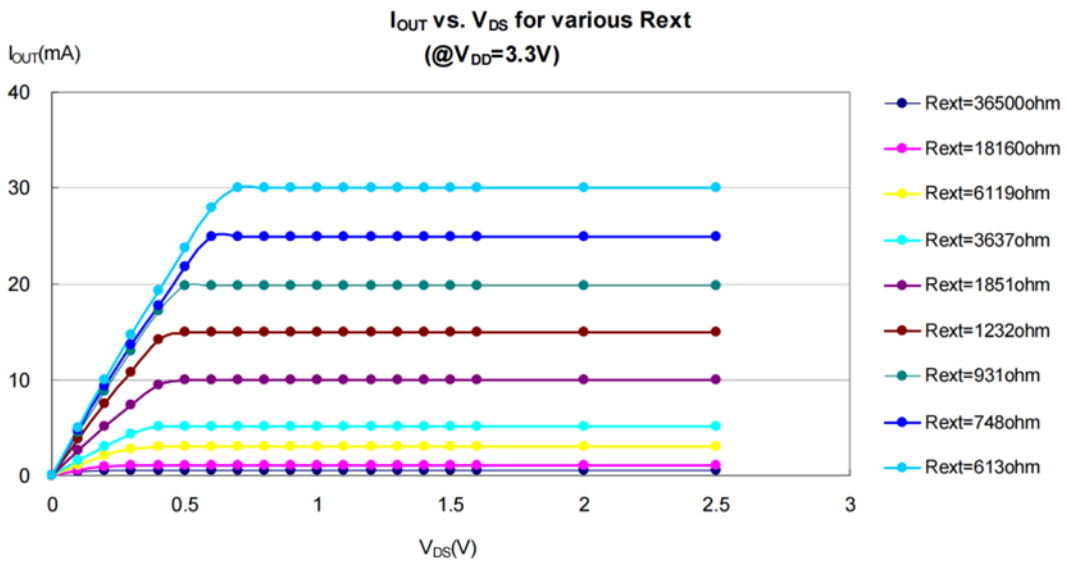
Constant Current

In LED display application, ET6024 provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximum current variation between channels is less than ±3%(typical), and that between ICs is less than ±6%(typical).

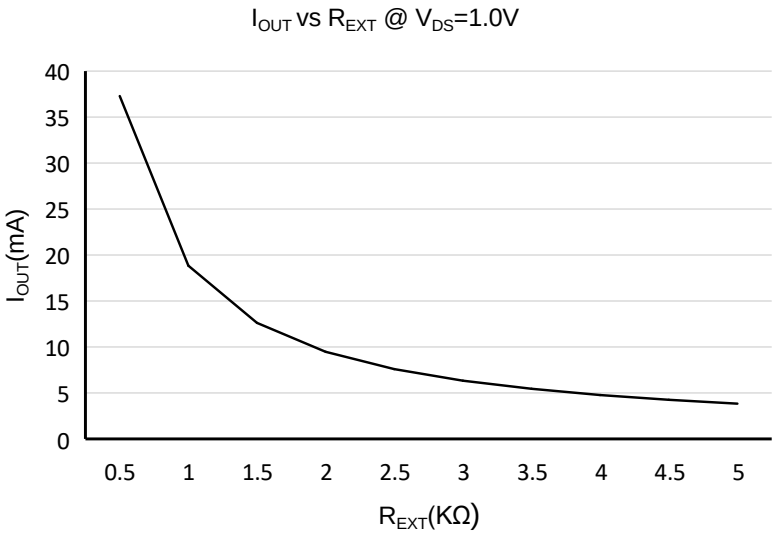
2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (Vf). This performs as a perfection of load regulation.





Adjusting Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, R_{EXT}. The relationship between Iout and R_{EXT} is shown in the following figure.



Resistance of the external resistor, R_{EXT}(KΩ)

Also, the output current can be calculated from the equation:

$$V_{R\text{-}EXT} = 1.24V;\ I_{OUT} = (V_{R\text{-}EXT} / R_{EXT}) \times 15$$

Where R_{EXT} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is the voltage of R-EXT terminal. The magnitude of current (as a function of R_{EXT}) is around 25mA at 744Ω and 10mA at 1860Ω.

Package Power Dissipation (P_D)

The maximum allowable package power dissipation is determined as P_D (max)=(T_J-T_A)/ $R_{\theta(JA)}$.

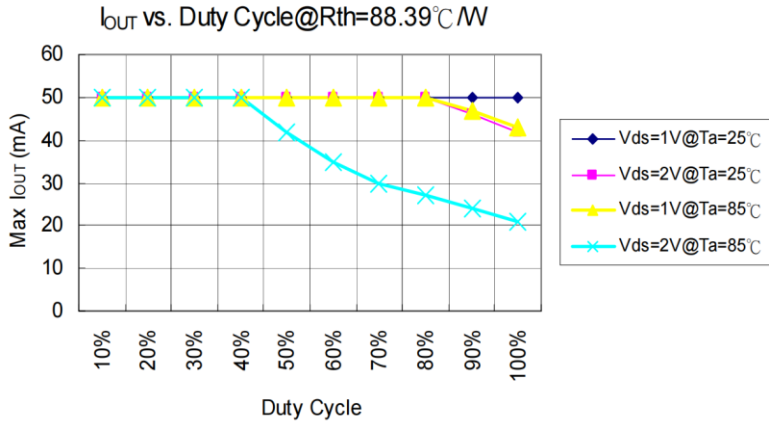
When 16 output channels are turned on simultaneously, the actual package power dissipation is

P_D (act)=(I_{DD}×V_{DD})+(I_{OUT}×Duty×V_{DS}×16).

Therefore, to keep P_D (act) ≤P_D (max), the allowable maximum output current as a function of duty cycle is:

I_{OUT} = {[(T_J – T_A) / $R_{\theta(JA)}$] – (I_{DD}×V_{DD})} / V_{DS} / Duty / 16,

where T_J = 150°C.

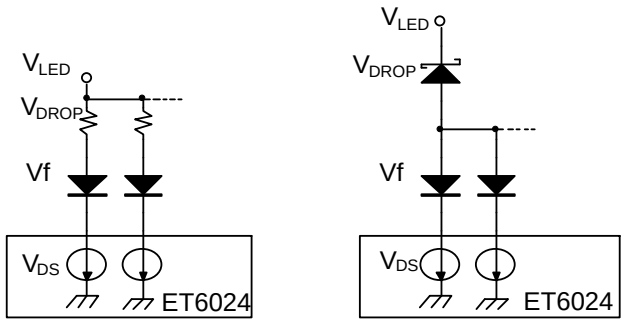


Condition: I_{OUT}= 50mA,16 output Channels	
Device Type	$R_{\theta(JA)}$(°C/W)
SSOP24-2	88.39
SSOP24-3	88.39

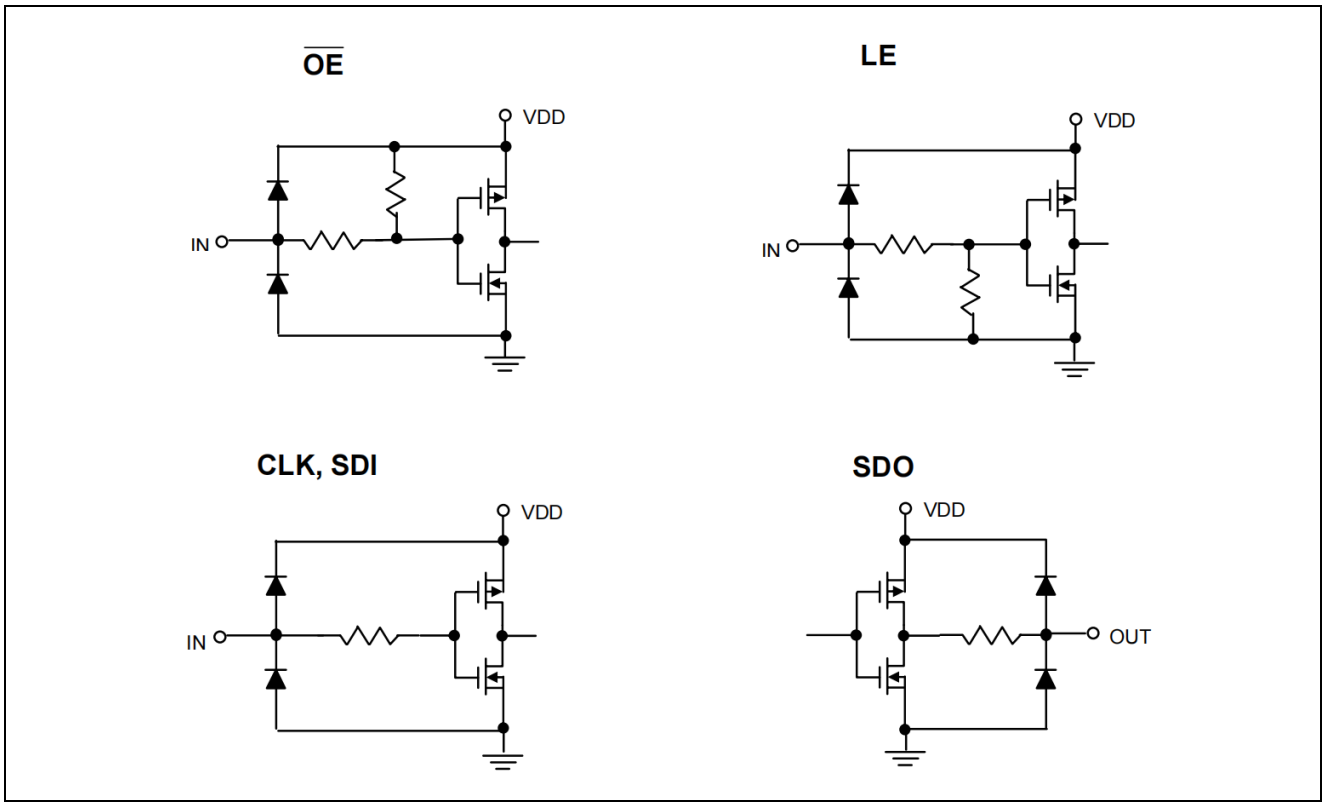
Load Supply Voltage (V_{LED})

ET6024 are designed to operate with V_{DS} ranging from 0.4V to 1.0V considering the package power dissipating limits. V_{DS} may be higher enough to make P_D(act) > P_D (max); when V_{LED}= 5V and V_{DS} = V_{LED} – Vf, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}. A voltage reducer lets V_{DS} = (V_{LED}–Vf) – V_{DROP}.

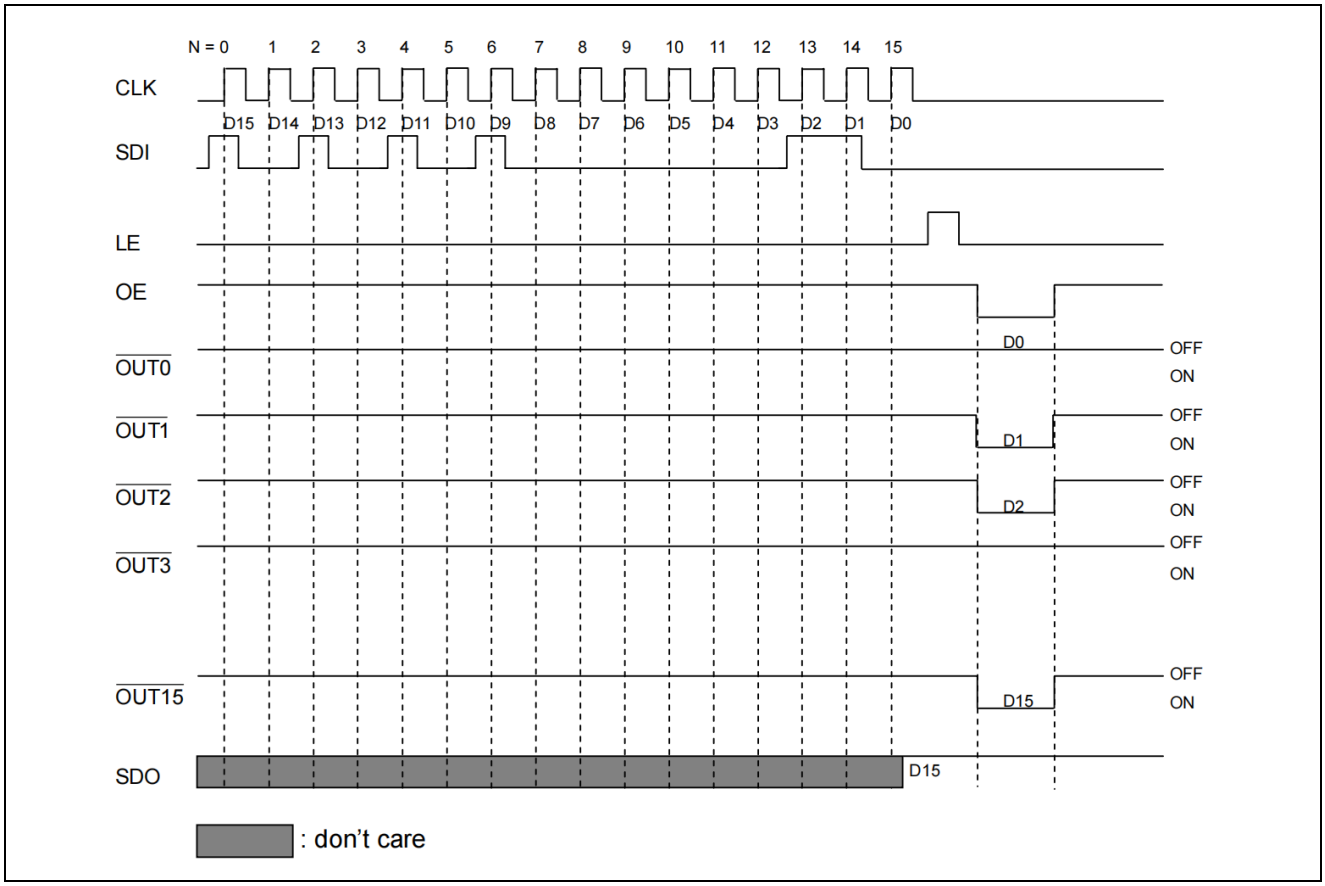
Resistors or Zener diode can be used in the applications as shown in the following figures.



Equivalent Circuits of Inputs and Outputs



Timing Diagram



Truth Table

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$ … $\overline{OUT7}$ … $\overline{OUT15}$	SDO
↑	H	L	D_n	$\overline{D_n}$ ..... $\overline{D_{n-7}}$ ..... $\overline{D_{n-15}}$	D_{n-15}
↑	L	L	D_{n+1}	No Change	D_{n-14}
↑	H	L	D_{n+2}	$\overline{D_{n+2}}$ ..... $\overline{D_{n-5}}$ ..... $\overline{D_{n-13}}$	D_{n-13}
↓	X	L	D_{n+3}	$\overline{D_{n+2}}$ ..... $\overline{D_{n-5}}$ ..... $\overline{D_{n-13}}$	D_{n-13}
↓	X	H	D_{n+3}	Off	D_{n-13}

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Unit
Supply Voltage	V_{DD}	0～7.0	V
Input Voltage	V_{IN}	-0.4～V_{DD} +0.4	V
Output Current	I_{OUT}	+60	mA
Output Voltage	V_{DS}	-0.5～20.0	V
Clock Frequency	F_{CLK}	25	MHz
GND Terminal Current	I_{GND}	1000	mA
Power Dissipation	P_D	1.4	W
Operating Temperature	T_A	-40～+85	°C
Storage Temperature	T_{STG}	-65～+150	°C

Electrical Characteristics (V_{DD}=5V, T_A=25°C)

Characteristic		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ～ $\overline{OUT15}$		-	-	20.0	V
Output Current		I_{OUT}	DC Test Circuit		3	-	45	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	T_A=-40～85°C		0.7V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	T_A=-40～85°C		GND	-	0.3V_{DD}	V
Output Leakage Current		I_{OH}	V_{OH} =20.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL} =+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH} =-1.0mA		4.6	-	-	V
Output Current 1		I_{OUT1}	V_{DS} =1.0V	R_{EXT} =1240Ω	-	15	-	mA
Current Skew (between channels)		dI_{OUT1}	I_{OL}=15mA V_{DS} =1.0V	R_{EXT}=1240Ω	-	±1.5	±3	%
Output Current 2		I_{OUT2}	V_{DS} =1.0V	R_{EXT} =620Ω	-	30	-	mA
Current Skew		dI_{OUT2}	I_{OL}=30mA	R_{EXT} =620Ω	-	±1.5	±3	%

(between channels)			V_{DS} =1.0V					
Current Skew (between ICs)		dI_{OUT3}	I_{OL}=30mA V_{DS} =1.0V	R_{EXT} =620Ω		±3	±6	%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS} within 1.0V to 3.0V		-	±0.1	-	%/V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 4.5V to 5.5V		-	±1	-	%/V
Pull-up Resistor		R_{IN} (up)	$\overline{OE}$		250	500	800	KΩ
Pull-down Resistor		R_{IN} (down)	LE		250	500	800	KΩ
Supply Current	"OFF"	I_{DD} (off)1	R_{EXT} =Unterminal, $\overline{OUT0}$ ～ $\overline{OUT15}$ =Off		-	2.5	5	mA
		I_{DD} (off)2	R_{EXT} =1240Ω, $\overline{OUT0}$ ～ $\overline{OUT15}$ =Off		-	4.5	7.0	
		I_{DD} (off)3	R_{EXT}=620Ω, $\overline{OUT0}$ ～ $\overline{OUT15}$ =Off		-	6	9.0	
	"ON"	I_{DD} (on)1	R_{EXT} =1240Ω, $\overline{OUT0}$ ～ $\overline{OUT15}$ =On		-	5.2	8.5	
		I_{DD} (on)2	R_{EXT}=620Ω, $\overline{OUT0}$ ～ $\overline{OUT15}$ =On			6.5	9.5	

Electrical Characteristics (V_{DD}=3.3V, T_A=25°C)

Characteristic		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	4.5	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ～ $\overline{OUT15}$		-	-	20.0	V
Output Current		I_{OUT}	DC Test Circuit		3	-	30	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	[illegible]		0.7V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	[illegible]		GND	-	0.3V_{DD}	V
Output Leakage Current		I_{OH}	V_{OH} =20.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL} =+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH} =-1.0mA		2.9	-	-	V
Output Current 1		I_{OUT1}	V_{DS} =1.0V	R_{EXT}=1860Ω	-	10	-	mA
Current Skew (between channels)		dI_{OUT1}	I_{OL}=10mA V_{DS} =1.0V	R_{EXT}=1860Ω	-	±1.5	±3	%
Output Current 2		I_{OUT2}	V_{DS} =1.0V	R_{EXT}=744Ω	-	30	-	mA
Current Skew (between channels)		dI_{OUT2}	I_{OL}=25mA V_{DS} =1.0V	R_{EXT}=744Ω	-	±1.5	±3	%
Current Skew (between ICs)		dI_{OUT3}	I_{OL}=25mA V_{DS} =1.0V	R_{EXT}=744Ω		±3	±6	%
Output Current vs. Output Voltage		%/dV_{DS}	V_{DS} within 1.0V to 3.0V		-	±0.1	-	%/V

Regulation							
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 3.0V to 3.6V	-	±1	-	%/V
Pull-up Resistor		R_{IN} (up)	$\overline{OE}$	250	500	800	KΩ
Pull-down Resistor		R_{IN}(down)	LE	250	500	800	KΩ
Supply Current	"OFF"	I_{DD} (off)1	R_{EXT} = Unterminal, $\overline{OUT0} \sim \overline{OUT15}$ =Off	-	1.8	5.0	mA
		I_{DD} (off)2	R_{EXT} =1860Ω, $\overline{OUT0} \sim \overline{OUT15}$ =Off	-	4.1	7.0	
		I_{DD} (off)3	R_{EXT} =744Ω, $\overline{OUT0} \sim \overline{OUT15}$ =Off	-	5.2	8.5	
	"ON"	I_{DD} (on)1	R_{EXT} =1860Ω, $\overline{OUT0} \sim \overline{OUT15}$ =On	-	4.5	7.0	
		I_{DD} (on)2	R_{EXT}=744Ω, $\overline{OUT0} \sim \overline{OUT15}$ =On		5.4	8.5	

Switching Characteristics (V_{DD}=5V, T_A=25°C)

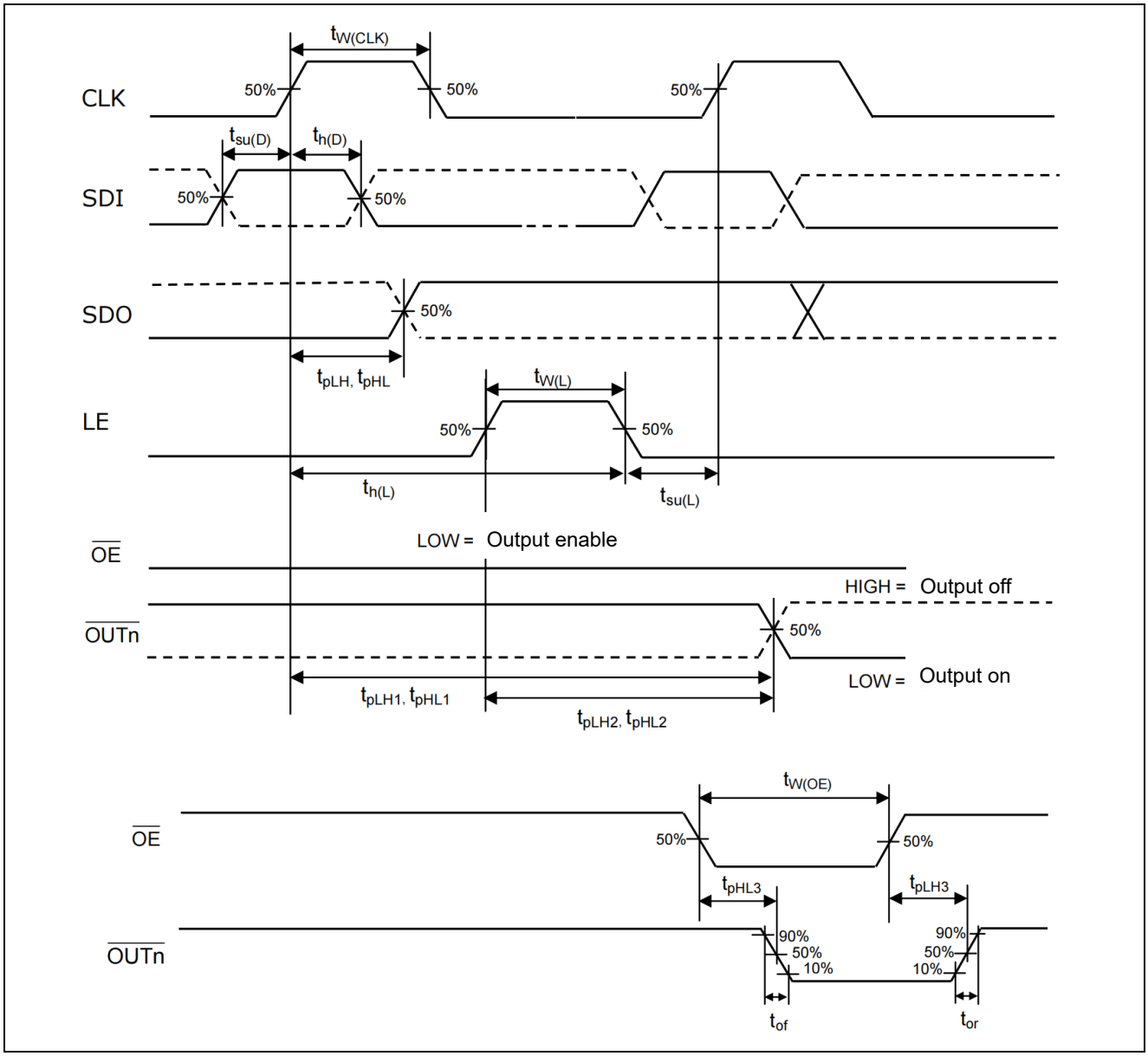
Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	CLK- $\overline{OUTn}$	t_{PLH1}	V_{DD} =5.0V V_{DS} =1.0V V_{IH} = V_{DD} V_{IL} =GND R_{ext} =930Ω V_L =4.5V R_L =162Ω C_L =10pF	-	80	100	ns
	LE - $\overline{OUTn}$	t_{PLH2}		-	80	100	ns
	$\overline{OE}$ - $\overline{OUTn}$	t_{PLH3}		-	115	135	ns
	CLK-SDO	t_{PLH}		-	20	40	ns
Propagation Delay Time ("H" to "L")	CLK- $\overline{OUTn}$	t_{PHL1}		-	80	100	ns
	LE - $\overline{OUTn}$	t_{PHL2}		-	80	100	ns
	$\overline{OE}$ - $\overline{OUTn}$	t_{PHL3}		-	115	135	ns
	CLK-SDO	t_{PHL}		-	20	40	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
	$\overline{OE}$	$t_{w(OE)}$		250	-	-	ns
Hold Time for LE		$t_{h(L)}$		5	-	-	ns
Setup Time for LE		$t_{su(L)}$		5	-	-	ns
Maximum CLK Rise Time		t_r**		-	-	500	ns
Maximum CLK Fall Time		t_f**		-	-	500	ns
Output Rise Time of Vout (turn off)		t_{or}		-	160	180	ns
Output Fall Time of Vout (turn on)		t_{of}		-	70	90	ns

Switching Characteristics (V_{DD}=3.3V, T_A=25°C)

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	CLK- $\overline{OUTn}$	t_{PLH1}	V_{DD} =3.3V V_{DS} =1.0V V_{IH} = V_{DD} V_{IL} =GND R_{ext} =930Ω	-	80	100	ns
	LE - $\overline{OUTn}$	t_{PLH2}		-	80	100	ns
	$\overline{OE}$ - $\overline{OUTn}$	t_{PLH3}		-	115	135	ns
	CLK-SDO	t_{PLH}		-	20	40	ns
Propagation Delay	CLK- $\overline{OUTn}$	t_{PHL1}		-	100	120	ns

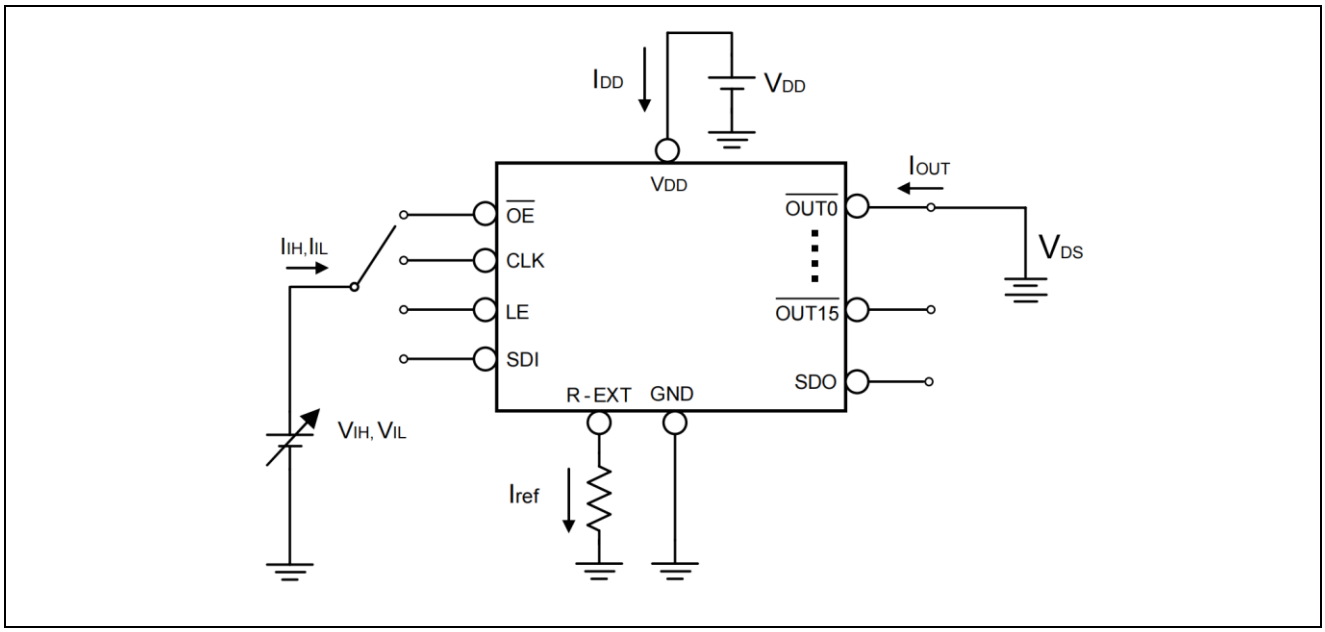
Time (“H” to “L”)	LE - $\overline{OUTn}$	t_{PHL2}	V_L =3.0V	-	80	100	ns
	$\overline{OE}$ - $\overline{OUTn}$	t_{PHL3}	R_L =100Ω	-	115	135	ns
	CLK-SDO	t_{PHL}	C_L =10pF	-	20	40	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
	$\overline{OE}$	$t_{w(OE)}$		300	-	-	ns
Hold Time for LE		$t_{h(L)}$		5	-	-	ns
Setup Time for LE		$t_{su(L)}$		5	-	-	ns
Maximum CLK Rise Time		t_r**		-	-	500	ns
Maximum CLK Fall Time		t_f**		-	-	500	ns
Output Rise Time of Vout (turn off)		t_{or}		-	160	180	ns
Output Fall Time of Vout (turn on)		t_{of}		-	70	90	ns

Timing Waveform

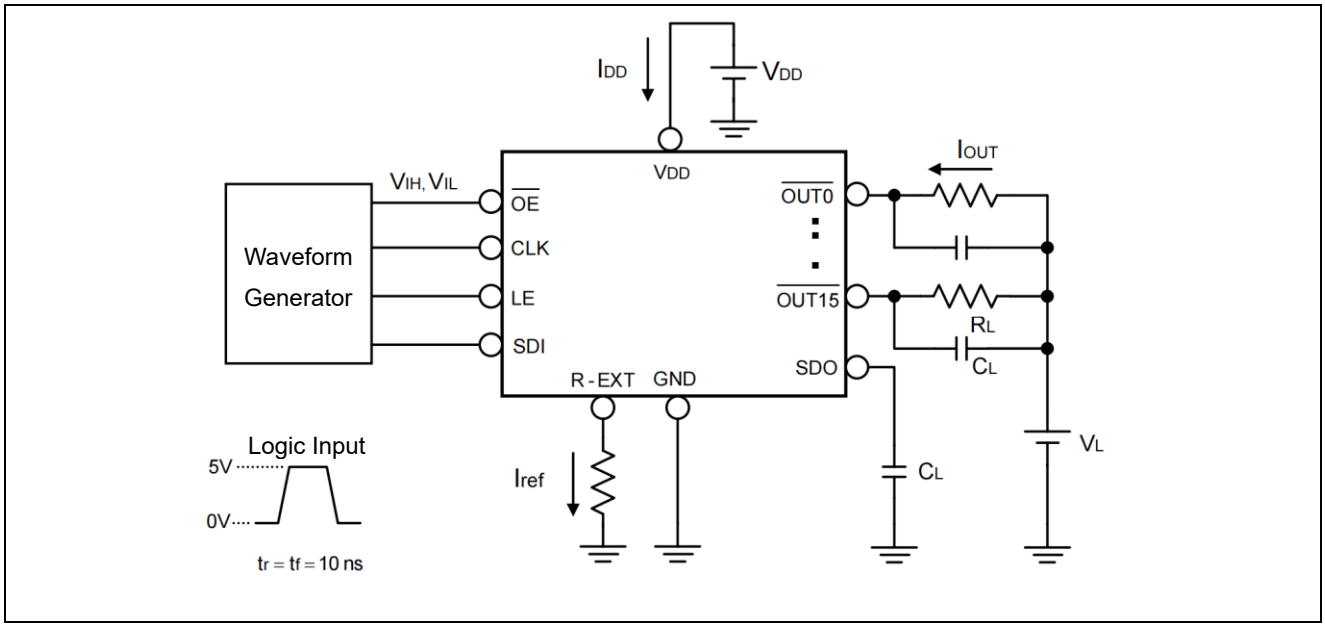


Application Circuits

Test Circuit for Electrical Characteristics

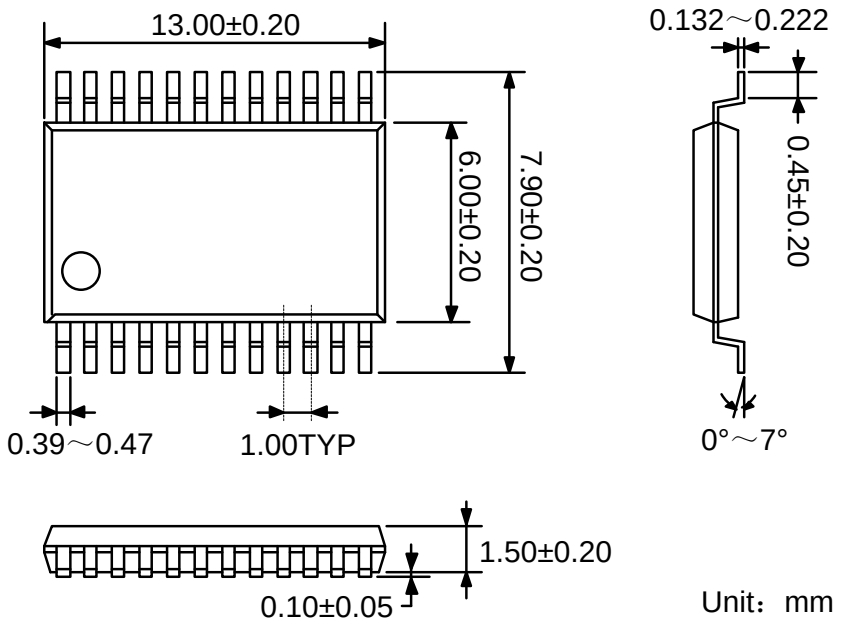


Test Circuit for Switching Characteristics



Package Dimension

SSOP24-3



SSOP24-2