High-Current Over-voltage Protectors with Adjustable OVLO and Input Voltage Detection

General Description

ET9640 can disconnect the systems from its output pin (OUT) in case wrong input operating conditions are detected. The system is positive over-voltage protected up to 28V. The internal over-voltage threshold (OVLO) is 13.75V. ET9640 has internal Thermal-Shutdown Protection and Input Voltage detection.

The device is packaged in advanced full-Green compliant DFN10 3mm×3mm.

Features

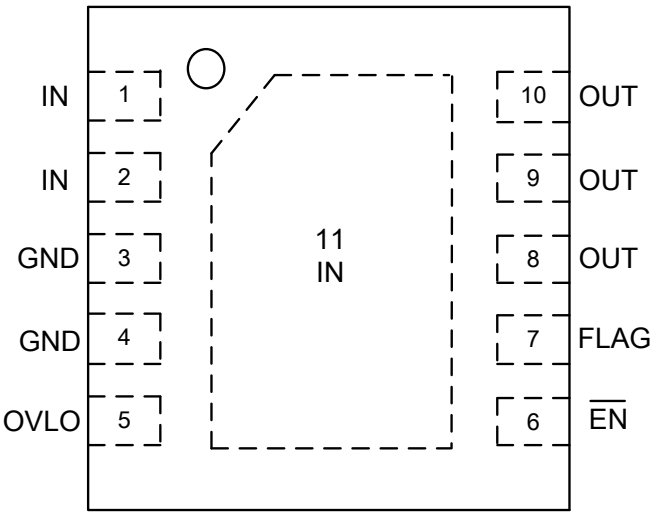
- 7A Continuous Current Capability
- Typical R_{ON}: 8mΩ N-Channel MOSFET
- V_{IN} Operating Range: 2.5V to 28V
- Internal Over-voltage Lockout: 13.75V
- Over-voltage-Protection Response Time: 80ns(TYP)
- Startup Debounce Time: 20ms(TYP)
- Internal Thermal-Shutdown Protection
- Surge immunity to ±100V
- ESD Protected: Human Body Model , All pins: ±2KV Pass
- Part No. and Package

Part No.	Package	Packing Option	MSL
ET9640	DFN10 (3mm×3mm)	Tape and Reel, 3K/Reel	1

Application

- Smartphones, Tablet PC
- HDD, Storage and Solid State Memory Devices
- Portable Media Devices, Laptop & MID
- SLR Digital Cameras
- GPS and Navigation Equipment
- Industrial Handheld and Enterprise Equipment

Pin Configuration

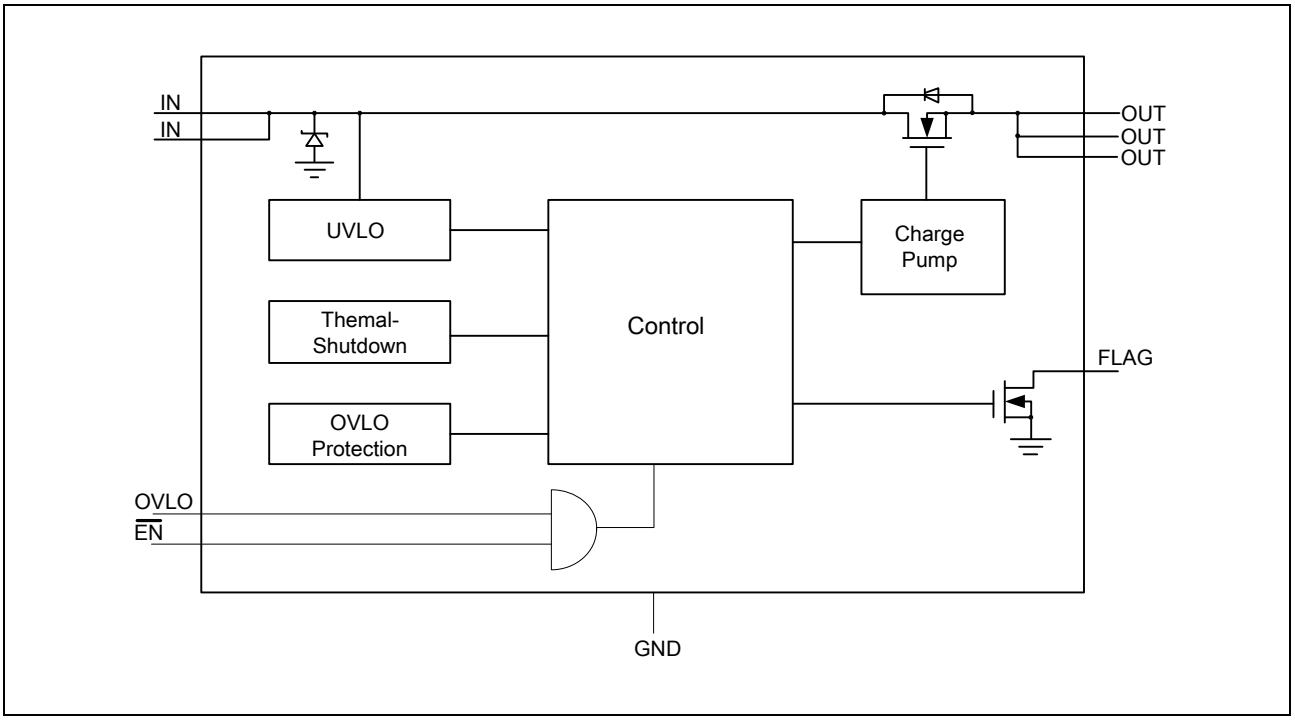


Top View

Pin Function

Pin	Name	Description		
1、2、11	IN	Voltage Input. Connect IN pins together for proper operation.		
3、4	GND	Ground. Connect GND pins together for proper operation.		
5	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.		
6	$\overline{EN}$	Device Enable. Active low.		
7	FLAG	Power status indicator	1	$V_{IN}<V_{UVLO}$ or $V_{IN}>V_{OVLO}$
			0	V_{IN} Stable
8、9、10	OUT	Output Voltage. Output of internal switch. Connect OUT pins together for proper operation.		

Block Diagram



Functional Description

The OVP switch with over-voltage protection feature a low 8mΩ(TYP) on-resistance (R_{ON}) internal FET and protect low-voltage systems against voltage faults up to 28VDC. $\overline{EN}$ is in the logic low state, when the input voltage (VIN) exceeds 13.75V, the internal FET is quickly turned off to prevent damage to the protected downstream components and the flag pin will output logic high state. If $\overline{EN}$ is in the logic high state, the switch will be shutdown. If there is no input voltage at IN pin, the flag pin output logic high state.

When input (OVLO) is set lower than 0.2V. The over-voltage protection threshold is 13.75V. The over-voltage protection threshold can also be adjusted by external resistors when input (OVLO) is set higher than 0.3V.

$$V_{IN_OVLO} = V_{OVLO_TH} \times (1 + \frac{R1}{R2})$$

Note：V_{OVLO_TH} = 1.2V(TYP).

The internal FET turns off when the junction temperature exceeds +155° C (TYP.). The device exits thermal shutdown after the junction temperature cools by 20° C (TYP.).

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor 1uF or lager must be placed between the VIN and GND pins.

Output Capacitor

A 1uF or lager capacitor should be placed between the OUT and GND pins.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters			Min	Max	Unit
V_{IN}	VIN to GND			-0.3	29	V
V_{OUT}	VOUT to GND			-0.3	V_{IN}+0.3	V
V_{OVLO}	OVLO to GND			-0.3	7	V
$V_{/EN}$	$\overline{EN}$ to GND			-0.3	7	V
V_{FLAG}	FLAG to GND			-0.3	7	V
I_{SW1}	Maximum Continuous Current of switch IN-OUT				7	A
I_{SW2}	Maximum Peak Current of switch IN-OUT (10ms)				12	A
P_D	Power Dissipation at T_A= +25°C				1.5	W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance				85	°C/W
T_{STG}	Storage Junction Temperature			-65	+150	°C
T_A	Operating Temperature Range			-40	+85	°C
T_S	Soldering Temperature (reflow)				+260	°C
T_J	Junction Temperature				+150	°C
V_{ESD}	Electrostatic Discharge Capability	IEC 61000-4-2 System Level ESD	Air Discharge	-15	+15	kV
			Contact Discharge	-8	+8	
		Human Body Mode ANSI/ESDA/JEDEC JS-001-2012	All Pins	-2	+2	
		Charged Device Model, JESD22-C101	All Pins	-1.5	+1.5	
V_{SURGE}		VIN to GND IEC 61000-4-5 Surge Protection	VBUS	-100	100	V

Electrical Characteristics

Unless otherwise noted, V_{IN}=2.5V to 28V, T_A=-40°C to 85°C, Typical values are at V_{IN}=5V, I_{VIN}≤2A, C_{VIN}=1uF and T_A=25°C.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
TVS Characteristics						
V_{BR}	Reverse Breakdown Voltage	I_T=10mA, T_A=25°C	29	31	35	V
I_{PP}	Peak Pulse Current(1)	t_P=8/20μs(+100V), T_A=25°C	28	32	35	A
V_C	Clamping Voltage(1)	I_{PP}=32A, t_P=8/20μs, T_A=25°C	32	36	40	V
I_{PP_NEG}	Reverse Peak Pulse Current(1)	t_p=8/20μs(-100V surge) , T_A=25°C	-44	-48	-52	A
V_{C_NEG}	Reverse Clamping Voltage(1)	I_{PP}=-48A, t_P=8/20μs, T_A=25°C	-1	-4	-6	V
V_F	Forward Voltage	I_F=10mA, T_A=25°C	0.2	0.6	0.8	V
Basic Operation						
V_{IN}	Input Voltage		2.5		28	V
I_{IN}	V_{IN} Quiescent Current	V_{IN}=5V, OUT floating	110	150	220	μA
I_{IN_OVLO}	OVLO Supply Current	V_{IN}=15V, $V_{/EN}$=0V, OUT floating	150	190	250	uA
R_{ON}	On-Resistance of Switch IN-OUT	V_{IN}=5.0V, I_{OUT}=1A, T_A=25°C	4	8	15	mΩ
V_{OVLO}	Over-voltage protect of V_{IN}	V_{IN} Rising	13.5	13.75	14	V
V_{OVLO_HYS}	Over-voltage protect hysteresis of V_{IN}		0.1	0.3	0.5	V
V_{OVLO_ADJ}	Adjustable OVLO Threshold Range		4		28	V
V_{OVLO_TH}	OVLO Set Threshold		1.17	1.2	1.23	V
V_{OVLO_ST}	External OVLO Select Threshold		0.2		0.3	V
V_{UVLO}	Under Voltage Lockout Threshold	V_{IN} Rising	1.7	2.0	2.4	V
		V_{IN} Falling	1.5	1.8	2.2	
I_{OVLO}	OVLO Input Leakage Current	V_{OVLO}=V_{OVLO_TH}	-100		100	nA
V_{OL_FLAG}	FLAG Output Logic Low Voltage	V_{PU}=1.8V, I_{SINK}=1mA	0	0.1	0.2	V
I_{FLAG_LEAK}	FLAG Output High Leakage Current	V_{FLAG}=5V	-0.5		0.5	uA
V_{IH}	$\overline{EN}$ Input Logic High Voltage	V_{IN}=2.5V to 28V	1.4			V

Electrical Characteristics (Continued)

Unless otherwise noted, V_{IN}=2.5V to 28V, T_A=-40°C to 85°C, Typical values are at V_{IN}=5V, I_{VIN}≤2A, C_{VIN}=1uF and T_A=25°C.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IL}	$\overline{EN}$ Input Logic Low Voltage	V_{IN}=2.5V to 28V			0.3	V
I_{OUT}	OUT discharge current	V_{IN}=5.0V, $\overline{EN}$=1.4V, V_{OUT}=1V	5	10	15	mA
T_{SHDN}	Thermal Shutdown(1)		135	155	175	°C
T_{HYS}	Thermal-shutdown Hysteresis(1)		10	20	30	°C
Dynamic Characteristics: see figure						
t_{DEB}	Debounce Time	Time from V_{UVLO}<V_{IN}< V_{OVLO} to V_{OUT}=10% of V_{IN}		20	32	ms
t_{SS}	Soft-start time	Time from V_{UVLO}<V_{IN}< V_{OVLO} to 0.2×FLAG, VIO=1.8V with 10kΩ Pull-up Resistor		33	45	ms
t_{ON}	Switch Turn-On Time	R_L=100Ω, C_L=22uF, V_{OUT} from 0.1×V_{IN} to 0.9×V_{IN}		6	13	ms
t_{OFF_RES}	Switch turn-off response time(1)	R_L=100Ω, No C_L, V_{IN} > V_{OVLO} to Vo stop rising		80	150	ns

Note1： Guaranteed by characterization and design.

Timing Waveform

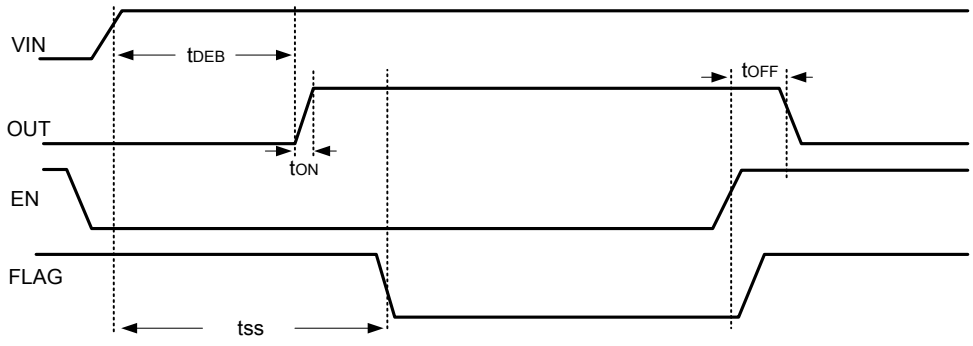


Figure1. Timing for Power Up and Normal Operation

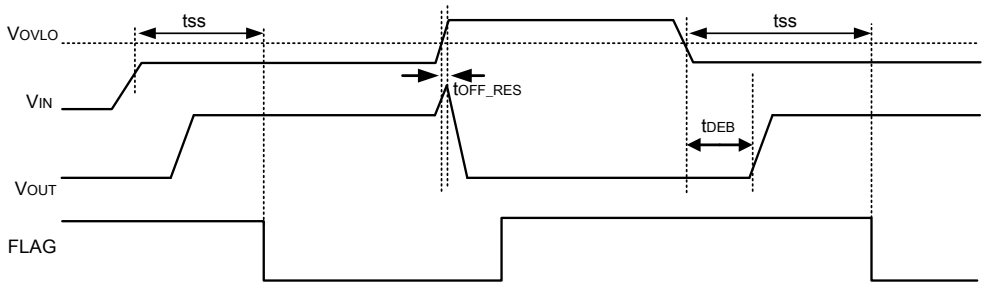


Figure2. Timing for OVLO Trip

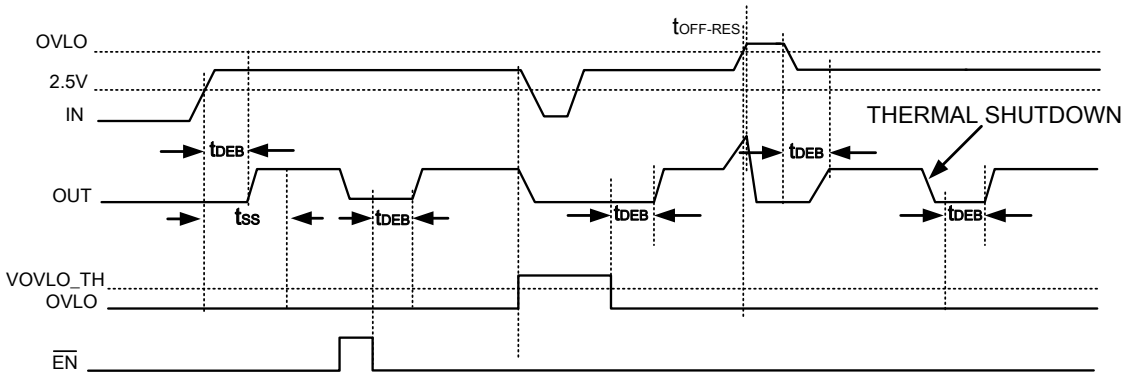
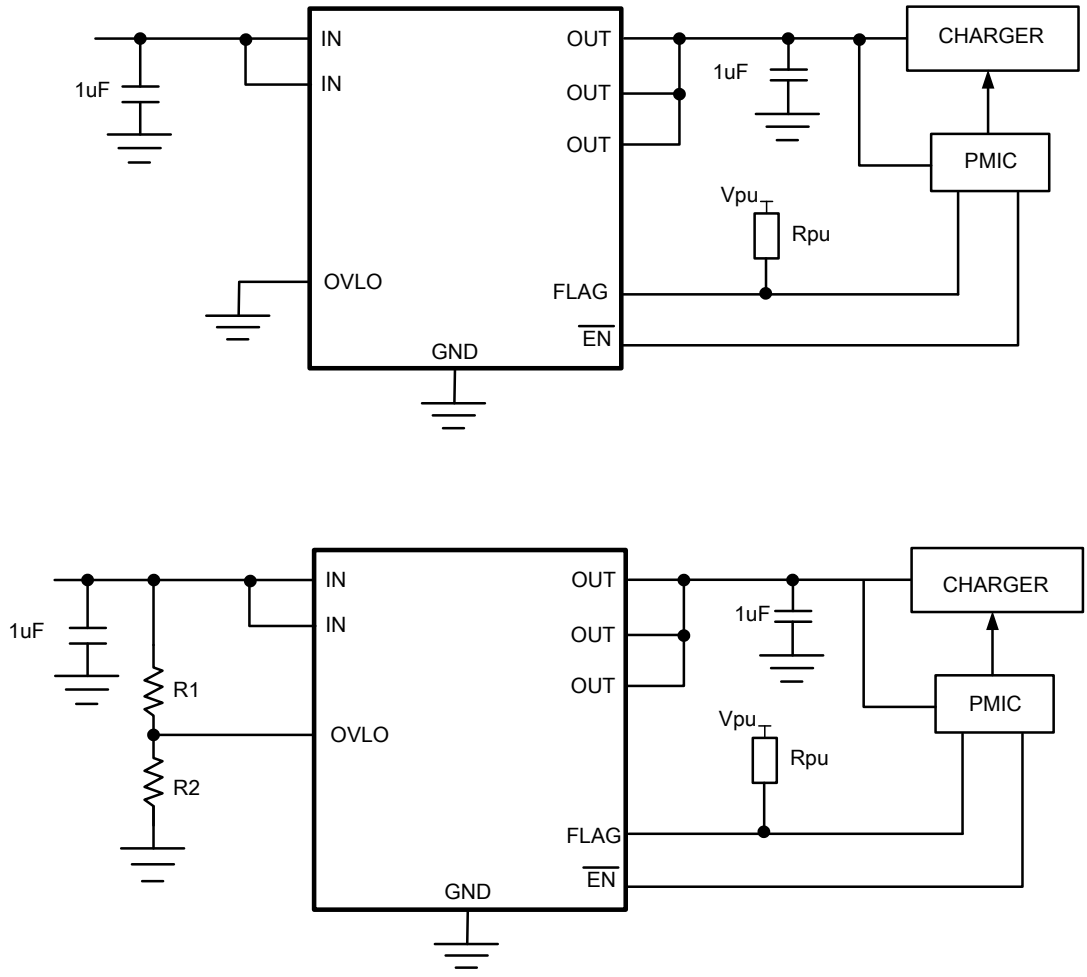


Figure3. Timing Waveform

Application Circuits



Notes:

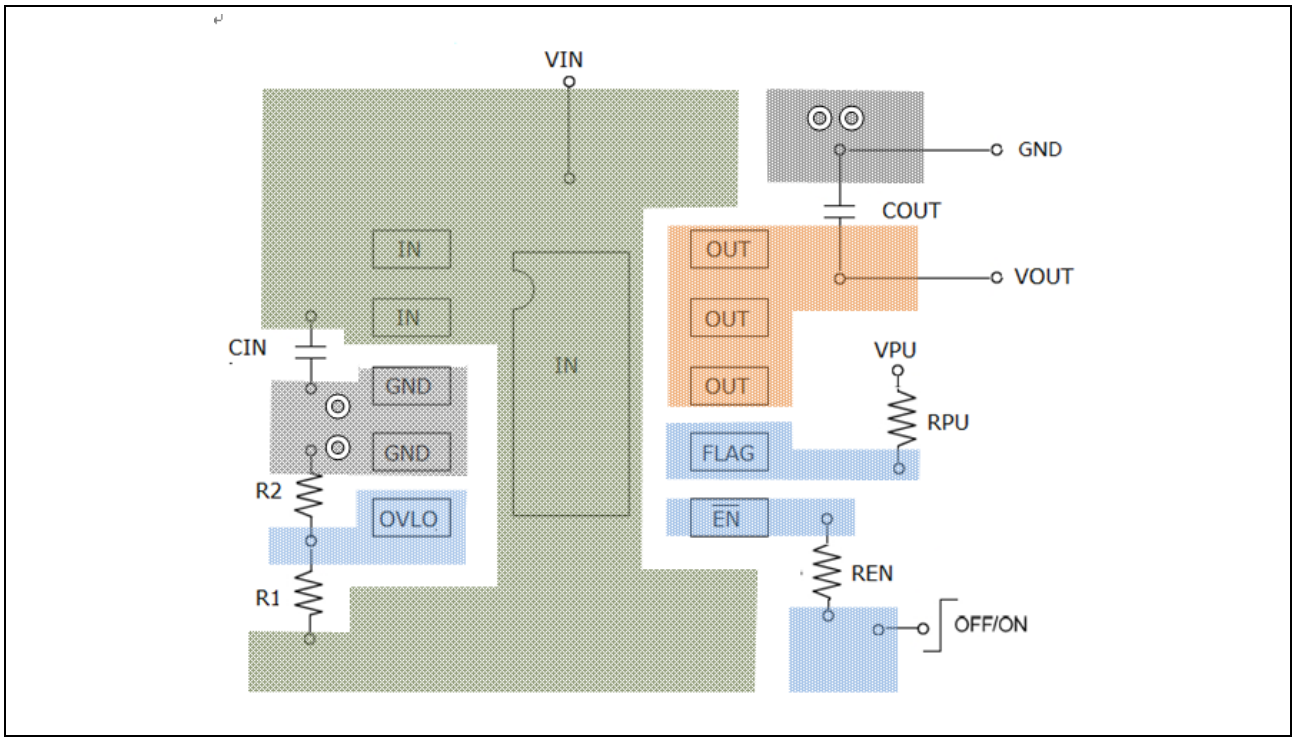
(1) This electric circuit only supplies for reference.

(2) R1 and R2 are only required for adjustable OVLO; otherwise connect OVLO to GND.

(3) Recommend 30K ≤ R2 ≤ 51K

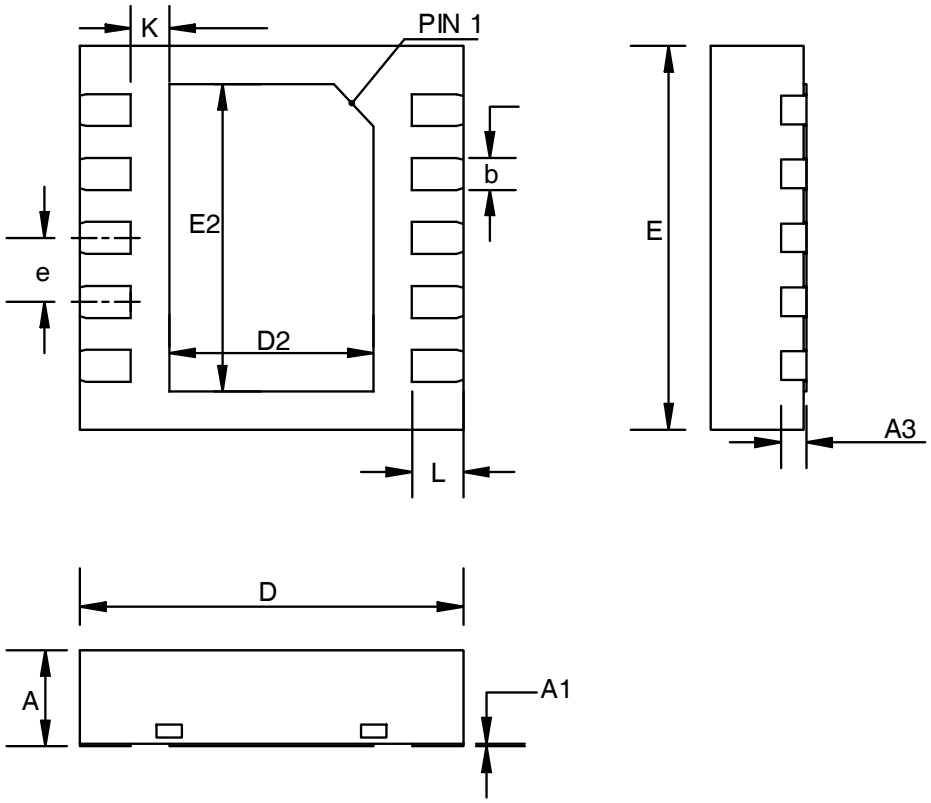
Board Layout

ET9640 can be routed in a single layer PCB. PCB traces to IN, OUT, $\overline{EN}$, FLAG, OVLO and GND can be routed in the fashion shown in below picture.



The decoupling capacitors per the recommended operating settings should be placed as close as possible to the ET9640. There should be a short path from the device ground pins to the system ground plane. This ensures best protection under ESD and surge transients.

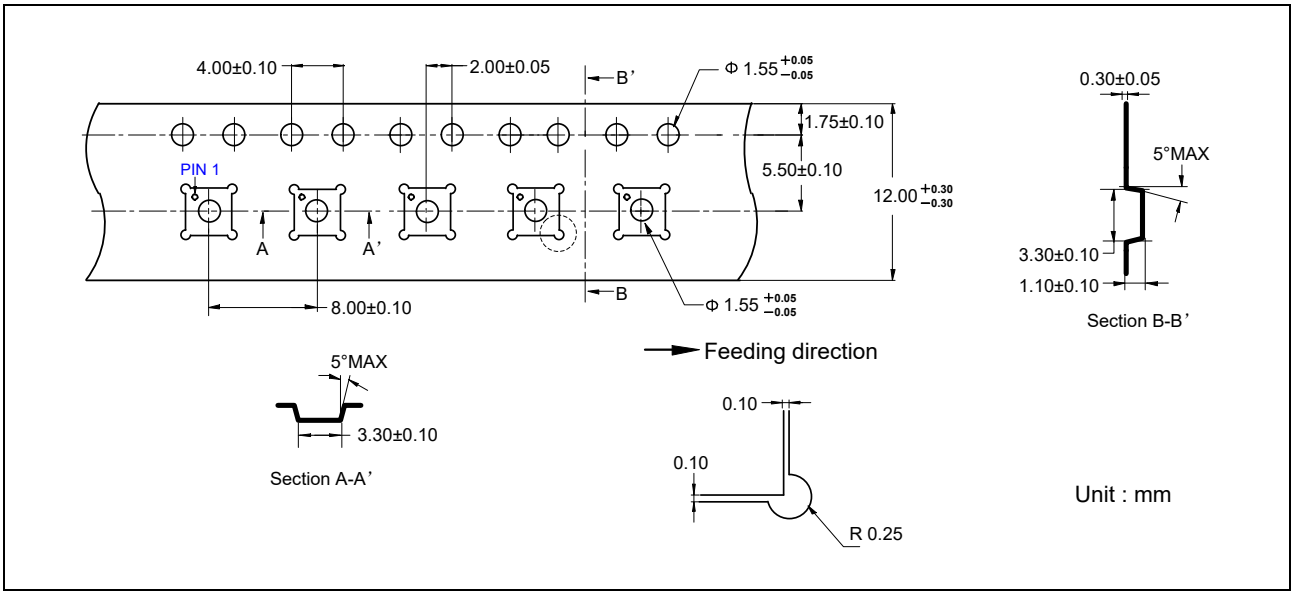
Package Dimension



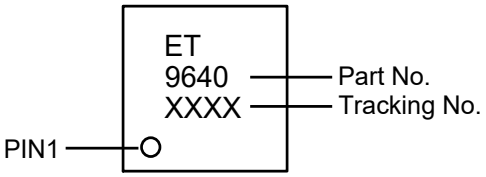
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
A3		0.203 REF	
b	0.2	0.25	0.3
D	2.9	3.0	3.1
E	2.9	3.0	3.1
D2	1.6	1.7	1.8
E2	2.5	2.6	2.7
e		0.5 BSC	
K		0.25 REF	
L	0.3	0.4	0.5

Tape Information



Marking



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2017-01-23	Original Version	Wu Xiang Jun	Wu Xiang Jun	Zhu Jun Li
1.1	2017-02-05	Add Iout	Wu Xiang Jun	Wu Xiang Jun	Zhu Jun Li
1.2	2017-04-25	Updated package dimension	Wu Xiang Jun	Wu Xiang Jun	Zhu Jun Li
1.3	2022-11-16	Update Typeset	Shi bo	Wu Xiang Jun	Liu Jia Ying
1.4	2024-08-12	Add up Data	Cao Jia Chen	Wu Xiang Jun	Liu Jia Ying
1.5	2025-12-12	Add Tape	Cao Jia Chen	Wu Xiang Jun	Liu Jia Ying
1.6	2026-05-22	Update Timing Waveform	Caojc	Wuhs	Liujy