# Linear Single Cell Li-Ion Battery Charger with Power Path Management and I²C-Control

## General Description

ET9562 is a linear single cell Li-ion battery charger integrated power path management. The charger uses a CC/CV charge profile required by Li-ion battery. It also accepts an input voltage up to 24V and will cut off rapidly when the input voltage exceeds OVP threshold (Typically 6.0V). The charger features trickle charge, constant current and constant voltage regulation, charge termination, and charge status.

The internal Power Path Management can balance the input current to system and battery, which ensures continuous power to the system from input, battery or both. Also ET9562 integrates dynamic power management. When system load is heavy, the charge current will be reduced to keep input current or input voltage in regulation.

ET9562 provides over-current protection from input to the system and battery to the system. This can prevent the Li-on battery from being damaged by excessively high current. Input and battery under-voltage lockout (UVLO) will cuts off the load path when power supply is unstable. An integrated I²C control interface allows the ET9562 to program the critical parameters, such as battery constant voltage, constant charge current, trickle charge threshold, battery regulation voltage, battery UVLO, input voltage regulation, input current regulation, and system voltage regulation.

The ET9562's high integration can simply system design and reduce the number of components outside. The device is packaged in advanced Full-Green compliant WCSP package.

## Features

- 24V Maximum Rating for VIN Power
- Internal 6.0V Over Input Voltage Protection
- Fully Autonomous Charger for Single-Cell Li-on Battery
- Auto Power Path Management for Powering the System and Charging the Battery
- Integrated Power MOSFETs for System load and Charging Mode
- ±0.5% Charging Voltage Accuracy
- I²C Interface for Setting Parameters
- Built-In input and battery UVLO Protection
- Thermal Limiting Regulation On-Chip
- Outside OTP Sensing by NTC pin

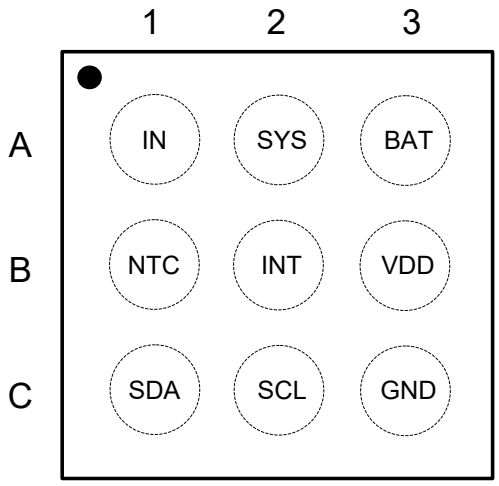
## Device Information

| Part No. | Package | MSL |
|---|---|---|
| ET9562 | CSP9(1.69mm×1.69mm) | Level 1 |

## Application

- Smart Watches
- Wearable Devices
- IP Camera

## Pin Configuration

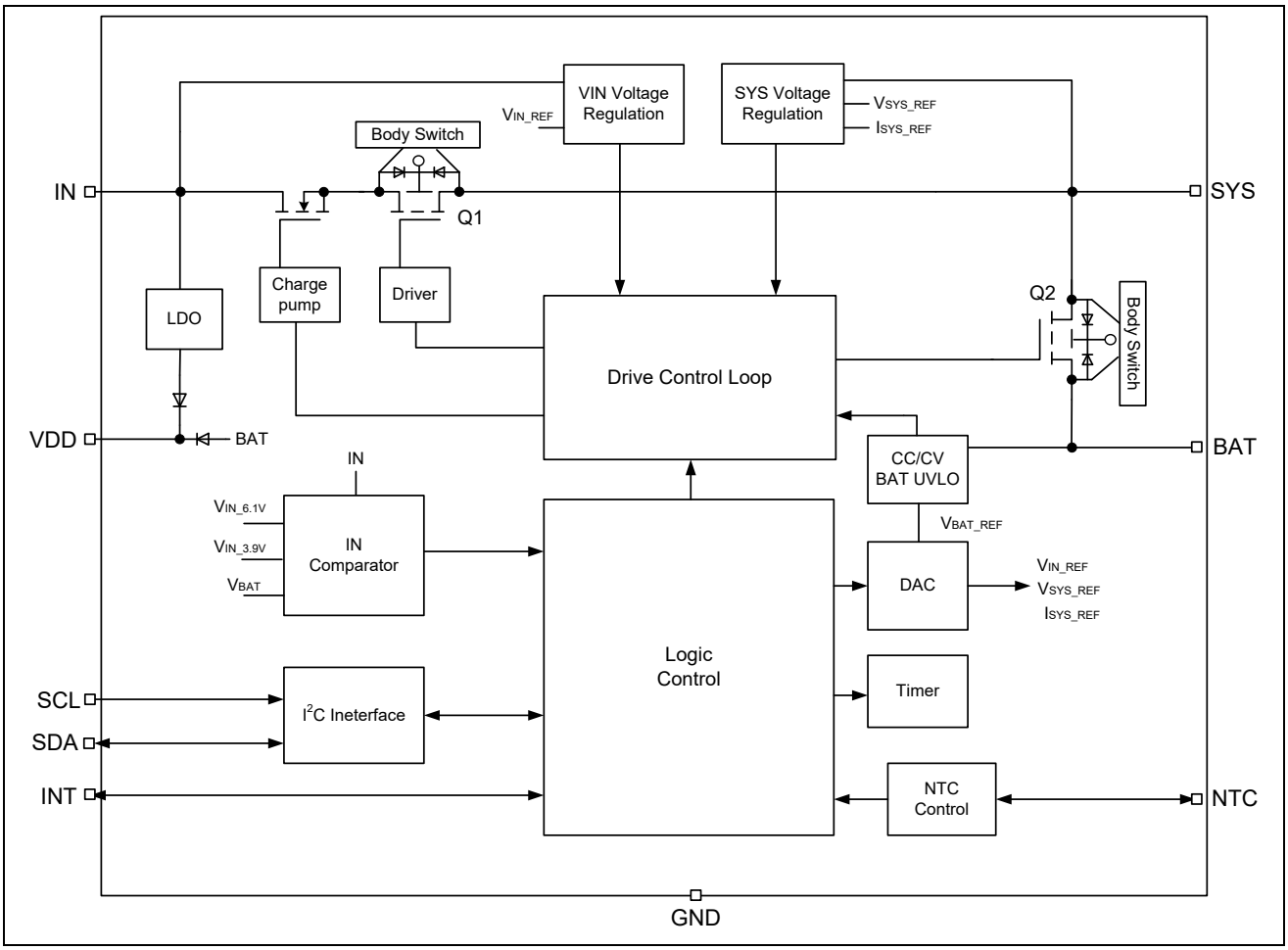



Top View

## Pin Function

| Pin No. | Pin Name | Description |
|---|---|---|
| A1 | IN | Power Supply Input Pin. |
| A2 | SYS | System Connect Pin. |
| A3 | BAT | Charge Output Pin. |
| B1 | NTC | Thermal sense Pin. |
| B2 | INT | Open Drain interrupt output. |
| B3 | VDD | Internal control power supply. |
| C1 | SDA | $I^2C$ interface data. |
| C2 | SCL | $I^2C$ interface clock. |
| C3 | GND | Ground. |

## Block Diagram



## Functional Description

ET9562 is a linear single cell Li-ion battery charger integrated power path management. The charger uses a CC/CV charge profile required by Li-ion battery. It also accepts an input voltage up to 24V and will cut off rapidly when the input voltage exceeds OVP threshold (Typically 6.0V). The charger features trickle charge, constant current and constant voltage regulation, charge termination, and charge status.

The internal Power Path Management can balance the input current to system and battery, which ensures continuous power to the system from input, battery or both. It allows for separate control between the system and the battery, and has high priority to power supply system.

The internal Dynamic Power Management can regulates the input voltage to $V_{IN\_REG}$ when the load is over the input power capacity. The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is at zero and the input source is still over-loaded, system voltage starts to fall down. Once the system voltage falls below the battery voltage, ET9562 enters battery supplement mode.

ET9562 provides over-current protection from input to the system and battery to the system. This can prevent the Li-on battery from being damaged by excessively high current. Input and battery under-voltage lockout (UVLO) will cuts off the load path when power supply is unstable. An integrated $I^2C$ control interface allows the ET9562 to program the critical parameters, such as battery constant voltage, constant charge current, trickle charge threshold, battery regulation voltage, battery UVLO, input voltage regulation, input current regulation, and system voltage regulation.

ET9562 include Battery Discharge Mode, Battery Supplement Mode, Battery Charge Mode, Only Power System Mode and Shipping Mode, Figure 1 is shown the internal state machine conversion.

(1) Battery Discharge Mode: Only Battery to SYS Path is enabled.
(2) Battery Supplement Mode: IN to SYS path and Battery to SYS path are enabled.
(3) Battery Charge Mode: IN to SYS path and IN to Battery path are enabled.
(4) Only Power System Mode: Only IN to SYS Path is enabled.
(5) Shipping Mode: All paths are disabled, ET9562 enters into low power consumption state.

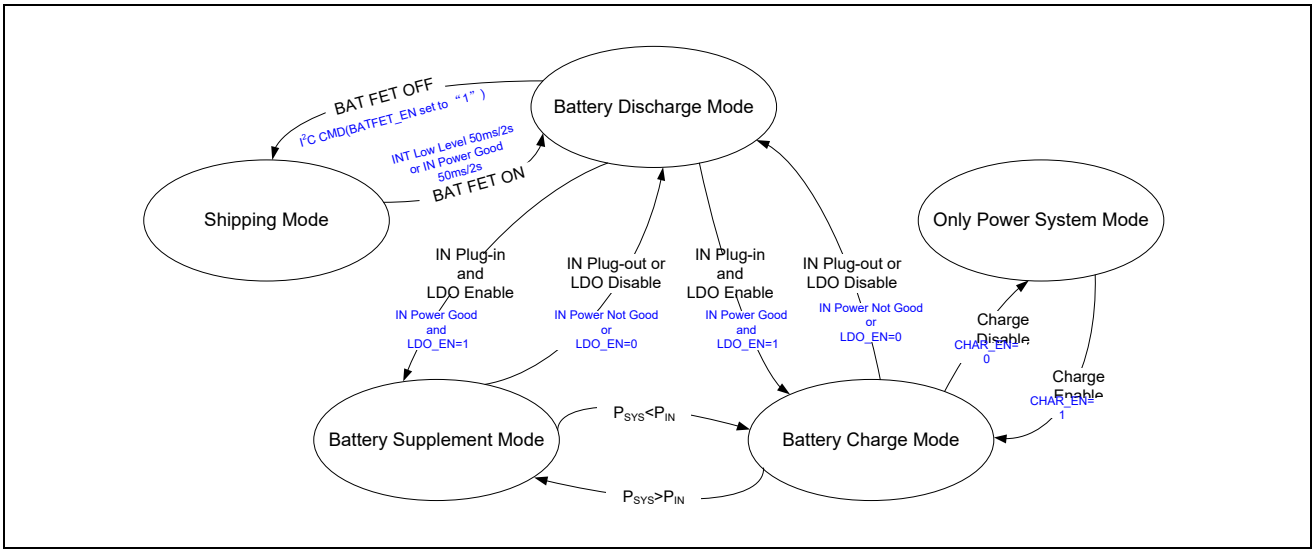



Figure 1. State Machine Conversion

## Power Supply

The internal bias circuit of the IC is powered from the higher voltage of IN or BAT. When IN or BAT rises above the respective under voltage lockout (UVLO) threshold, the sleep comparator, battery depletion comparator, and the battery MOSFET driver are active. After 2ms, the $I^2C$ interface is ready for communication and all registers are reset to the default value. The host can access all registers.

## Input OVP and UVLO

The ET9562 has an input over-voltage protection (OVP) threshold and an input UVLO threshold. Once the input voltage exits the normal input voltage range, the Q1 MOSFET is turned off immediately.

When the input voltage is identified as a good source, a 450us immunity timer is active. If the input power is still sufficient until the 450us timer expires, the system starts up. Otherwise, Q1 remains off. Figure 2 depicts the operation profile.

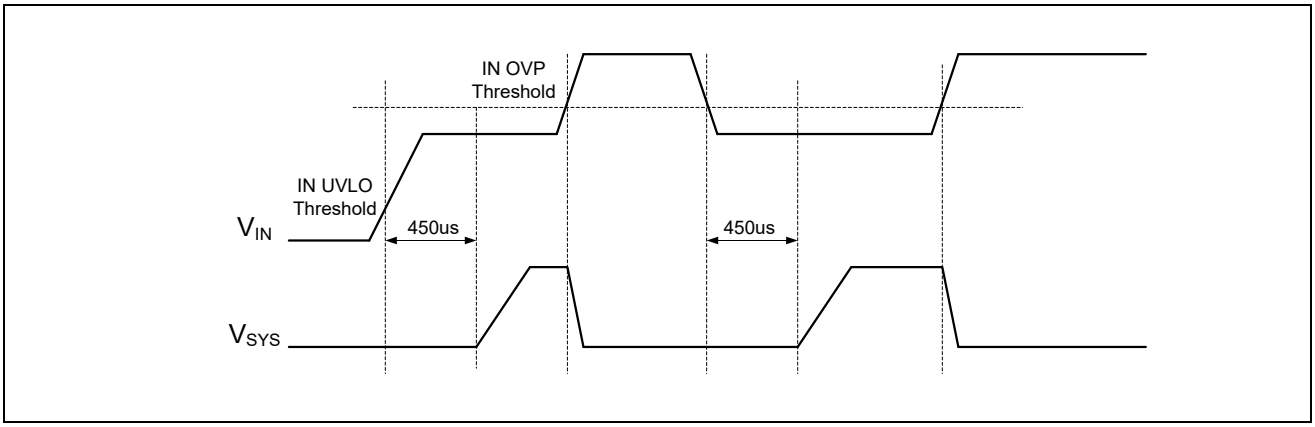



Figure 2. Input Power Detection Operation Profile

## Power Path Management

The IC employs a direct power path structure with the battery MOSFET decoupling the system from the battery, which allows for separate control between the system and the battery. The system is given the priority to start up even with a deeply discharged or missed battery. When the input power is available, even with a depleted battery, the system voltage is always regulated to $V_{SYS\_VSET}$ by the integrated LDO MOSFET. The system voltage can be programmable via Reg09[5:3], and the system voltage must higher than $V_{BAT\_REG}$+200mV.

As shown in Figure 3, the direct power structure is composed of a frond-end LDO MOSFET between IN and SYS and a battery FET between SYS and BAT.

The input LDO (using an LDO MOSFET) provides power to the system, which drives the system load directly and charges the battery through the battery FET. And the input LDO can be changed to switch mode by setting Reg01[4]=1.

For the system voltage control, when the input voltage is higher than $V_{SYS\_REG}$, the system voltage is regulated to $V_{SYS\_REG}$. When the input voltage is lower than $V_{SYS\_REG}$, the LDO MOSFET is fully on with the input current limit.

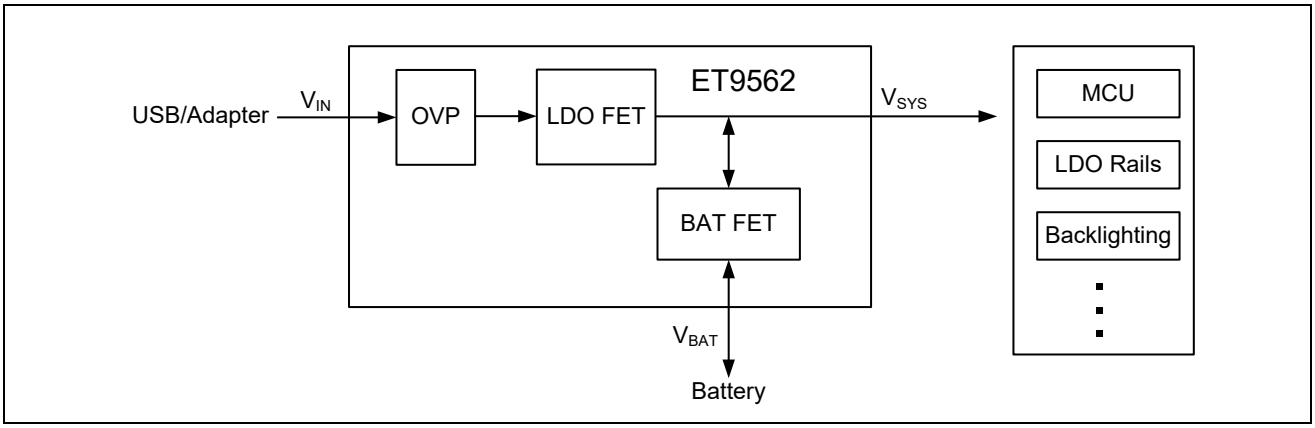



Figure 3. Power Path Management Structure

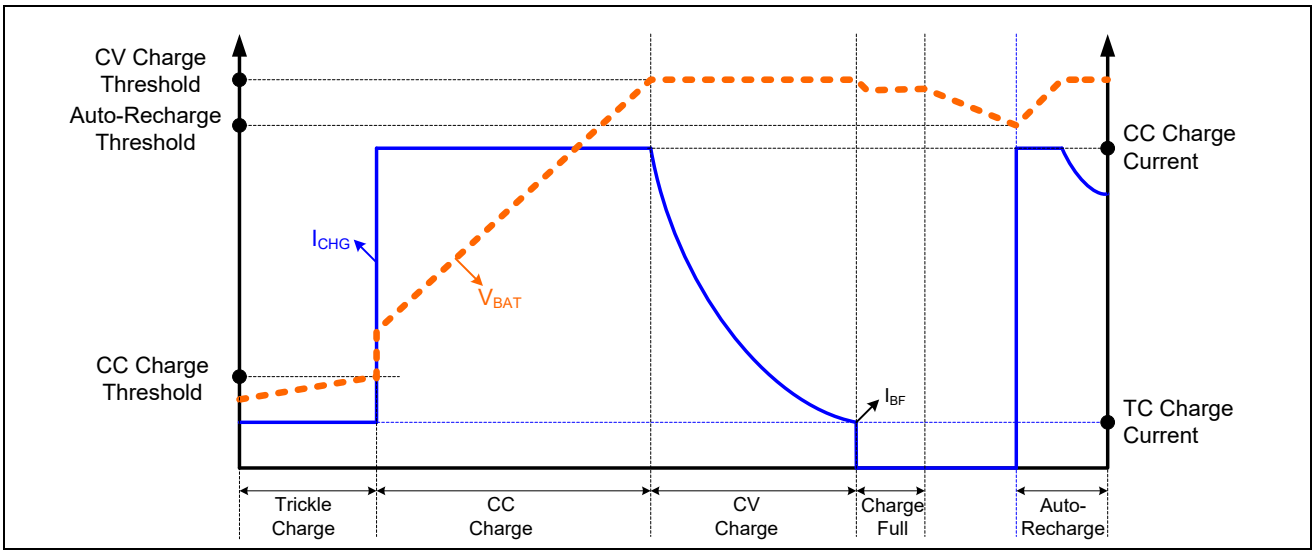



Figure 4. Battery Charge Profile

## Battery Charge Profile

The IC provides three main charging phases: trickle charge, constant current charge, and constant voltage charge (see Figure 4).

Phase 1 (trickle current charge): The IC is able to safely trickle charge the deeply depleted battery until the battery voltage reaches the trickle charge to the fast charge threshold ($V_{BAT\_LOW}$). The trickle charge current is programmable via Reg09[2:0]. If $V_{BAT\_LOW}$ is not reached before the precharge timer (1hr) expires, the charge cycle is ceased, and a corresponding timeout fault signal is asserted.

Phase 2 (constant current charge): When the battery voltage exceeds $V_{BAT\_LOW}$, the IC enters a constant-current charge (fast charge) phase. The fast charge current can be programmable via Reg02[5:0].

Phase 3 (constant voltage charge): When the battery voltage rises to the programmable charge full voltage ($V_{BAT\_REG}$) set via Reg04 bit [7:2], the charge mode changes from CC mode to CV mode, and the charge current begins to taper off.

Assuming the termination function (BF_EN) is set via Reg05[6] = 1, the charge cycle is considered complete when the following conditions are valid:

- The charge current ($I_{BAT}$) reaches the end of charge (EOC) current threshold ($I_{BF}$), and the 250ms delay timer is initiated.
- During the 250ms delay period, $I_{BAT}$ is always smaller than $I_{BF}$。

The charge status is marked as complete once the 250ms delay timer expires.

The charge current is terminated at the same time if TERMI_TEN is set via Reg05[0] = 0; otherwise, the charge current keeps tapering off.

If BF_EN=0, the termination function is disabled, the above actions will not occur. During the charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation. If the input current or the input voltage reach their limits during the CV charge, the charge full termination is not influenced when the charge current is not so close to the EOC current specification.

A new charge cycle starts when the following conditions are valid:
- The input power is recycled
- Battery charging is enabled by the $I^2C$
- Auto-recharge kicks in

Under the following conditions:
- No thermistor fault at NTC
- No safety timer fault
- No battery over-voltage
- BATFET is not forced to turn off

### Automatic Recharge

When the battery is fully charged and the charging is terminated, the battery may be discharged due to system consumption or self discharge. When the battery voltage is discharged below the recharge threshold, and VIN is still in the operation range, the IC begins another new charging cycle automatically without the requirement of restarting a charging cycle manually.

The auto-recharge function is valid only when BF_EN=1 and TERMI_TEN=0.

### Battery Over-Voltage Protection (OVP)

The IC is designed with a built-in battery over-voltage limit about 130mV higher than $V_{BAT\_REG}$. When the battery over-voltage event occurs, the IC suspends the charging immediately and asserts a fault.

### Input Current and Input Voltage Based Power Management

To meet the input source (usually USB) maximum current limit specification, the IC uses input current-based power management by monitoring the input current continuously. The total input current limit can be programmed via the $I^2C$ to prevent the input source from overloading.

If the pre-set input current limit is higher than the rating of the input source, back-up input voltage-based power management also works to prevent the input source from being overloaded. If either the input current limit or the input voltage limit is reached, the Q1 MOSFET between IN and SYS are regulated so that the total

input power is limited. As a result, the system voltage drops. Once the system declines to the minimum value of $V_{SYS}$-90mV or $V_{IN}$-160mV, the charge current is reduced to prevent the system voltage from dropping further.

Voltage-based DPM regulates the input voltage to $V_{IN\_REG}$ when the load is over the input power capacity. $V_{IN\_REG}$ set via the $I^2C$ should be at least 400mV higher than $V_{BAT\_REG}$ to ensure the stable operation of the regulator.

### Battery Supplement Mode

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is at zero, and the input source is still overloaded due to a heavy system load, the system voltage starts to fall off. Once the system voltage falls below the battery voltage, the IC enters battery supplement mode. When the system voltage is 30mV below the battery voltage, the ideal diode mode is enabled. The battery MOSFET is regulated to maintain $V_{BAT}$-$V_{SYS}$ at 22.5mV. If the supplement current $I_{DSG}$*$R_{ON\_BAT}$ is higher than 22.5mV, the battery MOSFET is fully turned on to keep the ideal forward voltage. When the system load decreases, once $V_{SYS}$ is higher than $V_{BAT}$+20mV, ideal diode mode is disabled.

Figure 5 shows the dynamic power management and battery supplement mode operation profile.

When VIN is not available, the IC operates in discharge mode, and the battery MOSFET is always fully on to reduce loss.

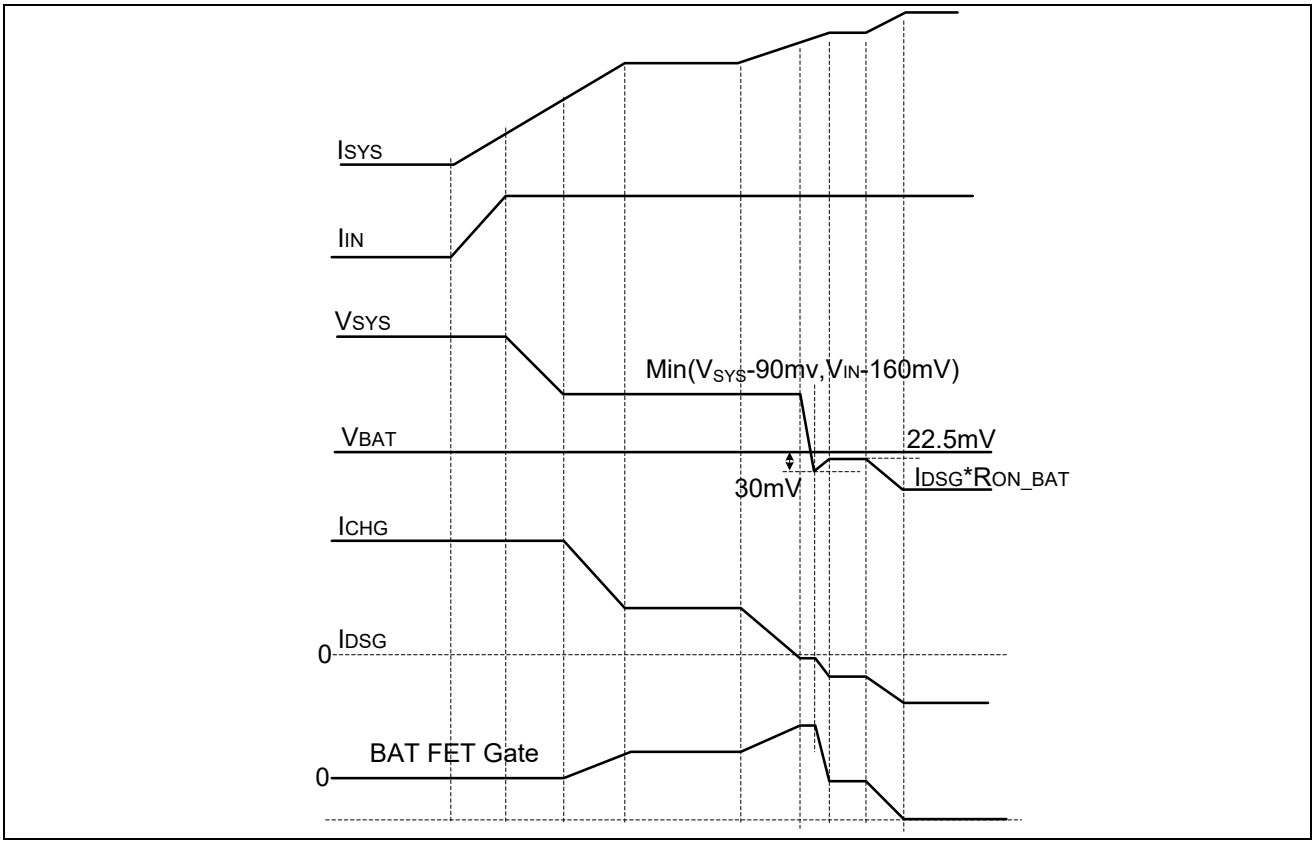



Figure 5. Dynamic Power Management and Battery Supplement Operation Profile

### Battery Charge Full Voltage

The battery voltage for the constant voltage regulation phase is $V_{BAT\_REG}$. When $V_{BAT\_REG}$ is 4.2V, it has a ±0.5% accuracy over the ambient temperature range of 0°C to +50°C. When the battery is removed, the BAT voltage is between $V_{BAT\_REG}$-$V_{RECHG}$ and $V_{BAT\_REG}$.

### Thermal Regulation and Thermal Shutdown

The IC monitors the internal junction temperature continuously to maximize power delivery and prevent the chip from overheating.

When the internal junction temperature reaches the pre-set limit of $T_{REG}$ (default 120°C), the IC reduces the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from 60°C to 120°C help the system design meet the thermal requirement in different applications. The junction temperature regulation threshold can be set via Reg06 bit [1:0].

When the junction temperature reaches 150°C, IN to SYS path and SYS to BAT path will be closed. But the BAT to SYS discharge path is still open .

### Negative Temperature Coefficient (NTC) Temperature Sensor

NTC allows the IC to sense the battery temperature using the thermistor usually available in the battery pack to ensure a safe operating environment for the chip. A resistor with an appropriate value should be connected from VDD to NTC, and the thermistor should be connected from NTC to ground. The voltage on NTC is determined by the resistor divider, whose divide ratio depends on the temperature. The IC sets a pre-determined upper and lower bound of the divide ratio internally for NTC cold and NTC hot. In the ET9562, the I²C default setting is the PCB OTP. The function can be changed through the I²C (see Table 1).

| I²C Control | | NTC PIN | Function |
|---|---|---|---|
| NTC_EN | PCB_OTP_EN | | |
| 0 | X | Not Floating | Disable |
| 1 | 0 | | NTC |
| 1 | 1 | | PCB OTP |
| X | X | Floating | Disable |

Table 1. NTC Function Selection Table

When PCB OTP is selected, if the NTC voltage is lower than the NTC hot threshold, both the LDO MOSFET and battery MOSFET are off. The PCB OTP fault sets the NTCH_FAULT status (Reg08 bit [1]) to 1 to indicate the fault. Operation resumes once the NTC voltage is higher than the NTC hot threshold.

The NTC function only works in charge mode. Once the NTC voltage falls out of the divide ratio (the temperature is outside the safe operating range), the IC stops the charging and reports it on the status bits. Charging resumes automatically after the temperature falls back into the safe range.

When NTC Pin is floating, NTC and PCB OTP function are disabled.

### Safety Timer

The IC provides both a pre-charge and a fast charge safety timer to prevent extended charging cycles due to abnormal battery conditions. The safety timer is one hour when the battery voltage is below $V_{TRICKLE\_CHAR\_VSET}$. The fast charge safety timer begins when the battery enters fast charging. The fast charge safety timer can be programmed through the $I^2C$. The safety timer feature can be disabled via the $I^2C$.

The following actions restart the safety timer:

- A new charge cycle is kicked in Reg01 bit[3] is written from 0 to 1 (charge enable)
- Reg05 bit [3] is written from 0 to 1 (safety timer enable)
- Reg01 bit [7] is written from 0 to 1 (software reset)

### Host Mode and Default Mode

The IC is a host-controlled device. After the power-on reset, all registers are in the default settings.

Any write to the IC changes it to host mode. All charge parameters are programmable. If the watchdog timer (Reg05 bit [5:4]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to the Reg01 bit [6] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the IC returns to default mode. The watchdog timer limit can also be programmed or disabled by the host control. When there is VIN, the default state of the watchdog timer is on, and the value is set as 160s. When there is no VIN, the default state of the watchdog timer is suspended. (Figure 6) Also, if the Reg05 bit[7] set to 1, then watchdog timer can also work when there is only Battery and no VIN.

The operation can also be changed to default mode when one of the following conditions occur:

- Refresh input without battery
- Re-insert battery with no VIN
- Register reset Reg01 bit [7] is reset

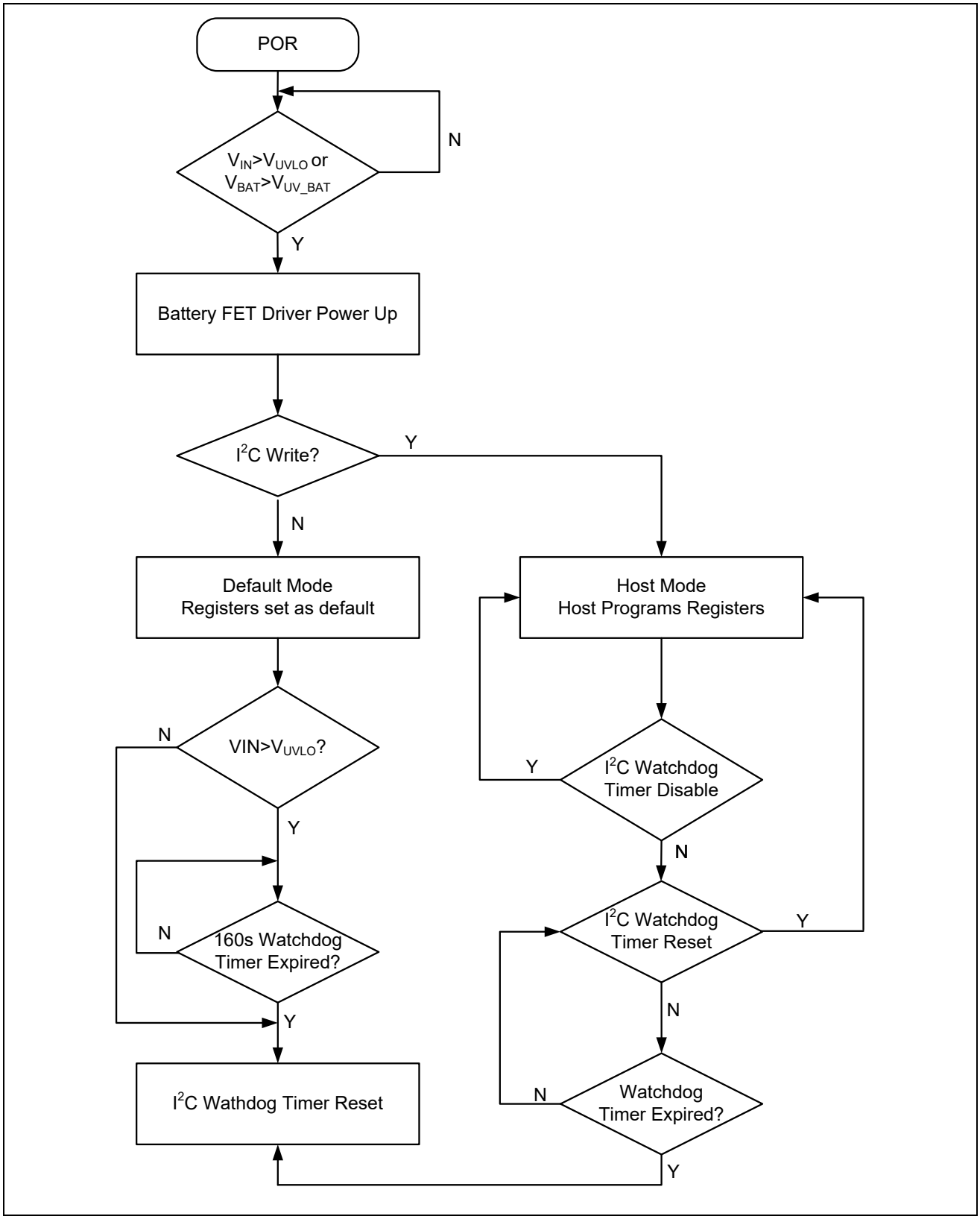



Figure 6. Default mode and Host mode Selection

### Battery Discharge Function

If battery is connected and the input source is missing, the battery MOSFET is fully on when VBAT is above the $V_{UV\_BAT}$ threshold. The 100mΩ battery MOSFET minimizes conduction loss during discharge. The quiescent current of the IC is as low as 11μA in this mode. The low on resistance and low quiescent current help extend the running time of the battery.

### Over-Discharge Current Protection

The IC has an over-discharge current protection in discharge mode and supplement mode. Once $I_{BAT}$ exceeds the programmable discharge current limit (default 2A), the battery MOSFET is turned off after a 60μs delay, and the ET9562 enters hiccup mode in over-current protection. The discharge current can be programmed high to 2.67A through the $I^2C$.If the discharge current goes high to reach the internal fixed current limit (about 3.7A), the battery MOSFET is turned off and starts hiccup mode immediately. The interval of the hiccup mode is 800μs.

Similarly, when the battery voltage falls below the programmable $V_{UV\_BAT}$ threshold (default 2.8V), the battery MOSFET is turned off to prevent over-discharge.

### System Short-Circuit Protection (SCP)

The ET9562 features SYS node short-circuit protection (SCP) for the IN to SYS path and the BAT to SYS path.

The system voltage is continuously monitored. If $V_{SYS}$ is lower than 1.5V, the system (SCP) for the IN to SYS path and the BAT to SYS path are active. $I_{BATOC}$ is decreased to half of the original value.

1) IN to SYS path: Once $I_{IN}$ is over the 360mA protection threshold, both the LDO MOSFET and the BAT MOSFET are turned off immediately, and the IC enters hiccup mode. Otherwise, the max current limit (360mA) are not reached and the setting input current limit are reached, and $I_{IN}$ is regulated at IN_ILMTI_SET. Hiccup mode also starts after a 60μs delay. The interval of the hiccup mode is 800μs.

2) BAT to SYS path: Once $I_{BAT}$ is over the 3.7A protection threshold, both the LDO MOSFET and the BAT MOSFET are turned off immediately, and the IC enters hiccup mode. When the battery discharge current limit threshold is reached, hiccup mode starts after a 60μs delay. The interval of the hiccup mode is 800μs.

If a system short-circuit occurs when both the input and battery are present, the protection mechanism of both paths work, with the faster one dominating the hiccup operation. (Figure 7)

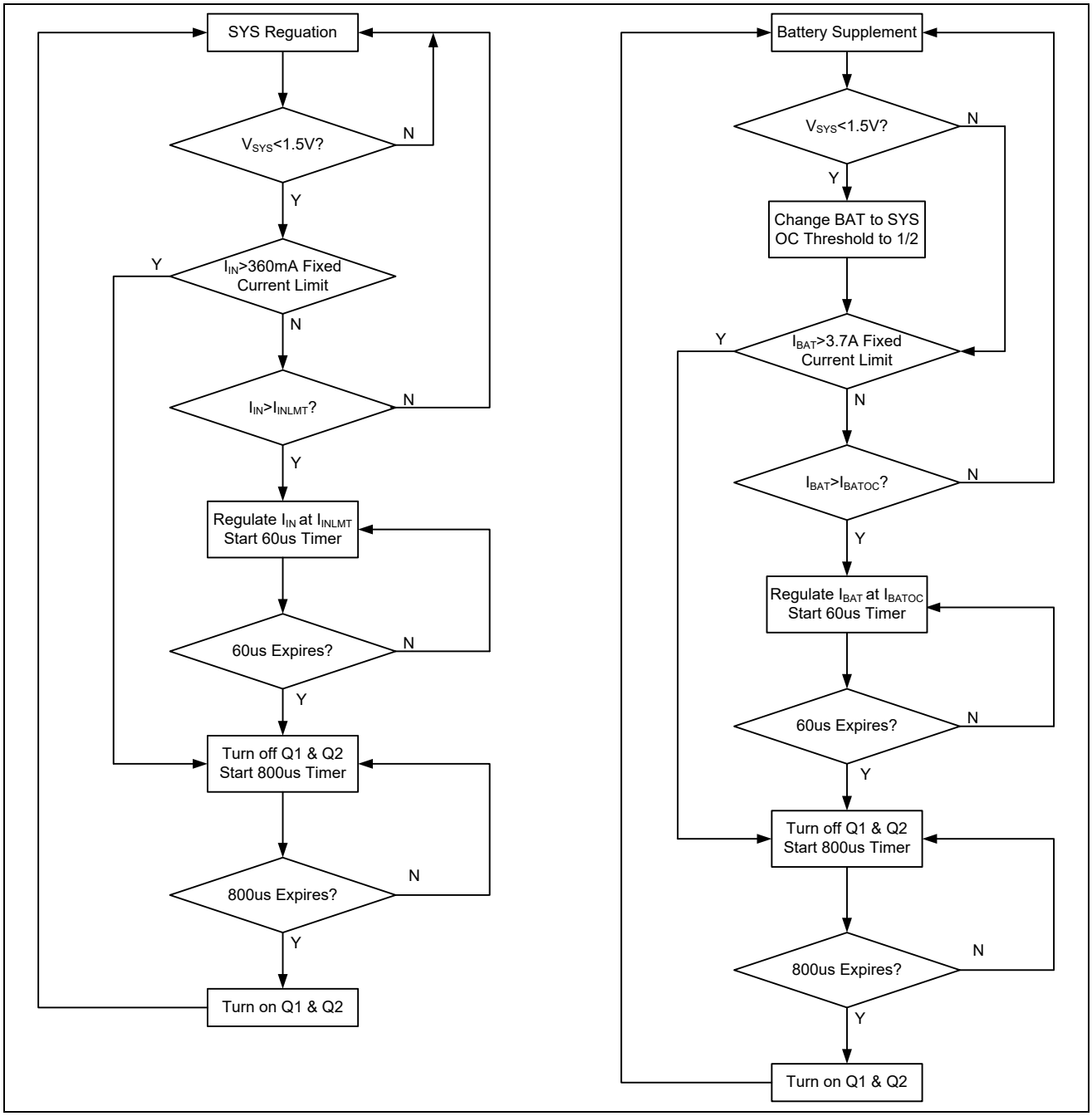



Figure 7. System Short-Circuit Protection

### Interrupt to Host (INT)

The IC has an alert mechanism which can output an interrupt signal via INT to notify the system of the operation by outputting a 256μs low-state INT pulse. All of below events can trigger the INT output:

- Input Good Source detected
- UVLO or OVP for IN Port or $V_{IN}$<$V_{BAT}$+200mV
- Charge Completed
- Any faults in Reg08(Watchdog time fault, Input fault, Thermal fault, Battery OVP fault, Safety time fault, NTC fault)

When any fault occurs, the IC sends out an INT pulse and latches the fault state in Reg08. After the IC exits the fault state, the fault bit could be released to 0 after the host reads Reg08. So the Reg08 register is not a real-time monitoring, if we want to get the chip's real-time working status, we should read the Reg08 for twice, and the data read the second time is the real-time working status of the chip.

The NTC fault is not latched and always reports the current thermistor conditions.

Note that the INT needs the external pull up resistor for its open-drain connection. Suggest the resistance not lower than 100kΩ.

If we set Reg0A[5]=0, the INT interrupt output will be closed.

### Battery Disconnection Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system:
Case A: to prevent excessive capacity discharge during the device is in shipping or storage.
Case B: allow the system power reset

The ET9562 provides both shipping mode and system reset mode for different application requirements.

**1). Shipping Mode:**

**Entering the Shipping mode:** The register bit (BATFET_EN), Reg06 Bit[5], controls the IC to enter the shipping mode.

During the normal operation, the battery MOSFET is turned on and this bit is 0. If this bit is set to 1 through $I^2C$, the battery MOSFET is turned off, and the ET9562 enters shipping mode. The BATFET_EN bit is reset to 0 automatically after the battery MOSFET is turned off(refer to Figure 8).

When VIN is in place, we enter the shipping mode, the SYS will not be closed, and the chip will enter the shipping mode after the VIN removed.

Before entering the shipping mode, we pull down the INT, the shipping mode instruction should be input after INT wake up time(50ms/2s), or it will not enter the shipping mode. When we enter the shipping mode in this condition, the internal clock is waked up by the low INT, the current of BAT will be higher.

**Exiting shipping mode:** The IC can exit the shipping mode by pulling INT down or a valid VIN power on.
1.1) When the IC is in the shipping mode and only the Battery is present, pulling INT down by pushing KEY1 (see the "TYPICAL APPLICATION CIRCUIT" ) could wake the ET9562 up from shipping mode. (refer to Table 2 and Figure 8)

If we set Reg0A[4]=0, the INT exiting shipping mode and SYS reset function will be closed.

| | INT Signal | IC Exists the Shipping Mode |
|---|---|---|
| Case1(int_exit_ship_tset=0), Reg0A Bit1 | One negedge of INT and INT Keep Low level>50ms | At Once |
| Case2(int_exit_ship_tset=1), Reg0A Bit1 | One negedge of INT and INT Keep Low level >2s | At Once |

Table 2. Exit Shipping mode with BAT present only

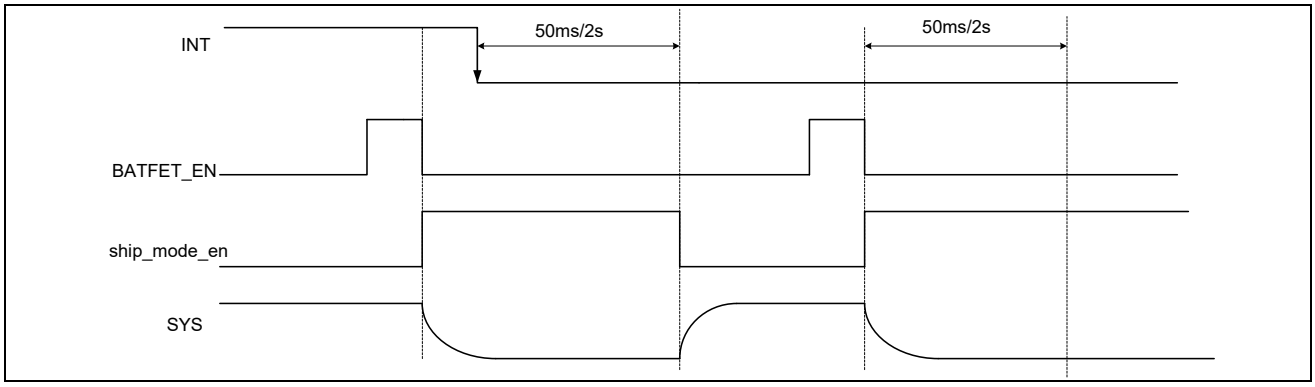



Figure 8. Enter Shipping mode and Exit Shipping mode by INT Low Level

1.2) When the IC is in the shipping mode and a valid VIN powers on, the ET9562 could be woken up too. After effective VIN voltage is preset, the ET9562 could be woken up from the shipping mode by the IN Power Good signal(refer to Table 3 and Figure 9).

VIN voltage effective condition：

- $V_{IN}>V_{IN\_UVP}$
- $V_{IN}<V_{IN\_OVP}$
- $V_{IN}>V_{BAT}$+200mV

| | IN Signal(Power Good Signal) | IC Exists the Shipping Mode |
|---|---|---|
| Case1(in_exit_ship_tset=0), Reg0A Bit0 | One posedge of IN Power Good and Keep Power Good Signal>50ms | At Once |
| Case2(in_exit_ship_tset=1), Reg0A Bit0 | One posedge of IN Power Good and IN Keep Power Good Signal >2s | At Once |

Table 3. Exit Shipping mode with VIN powers on

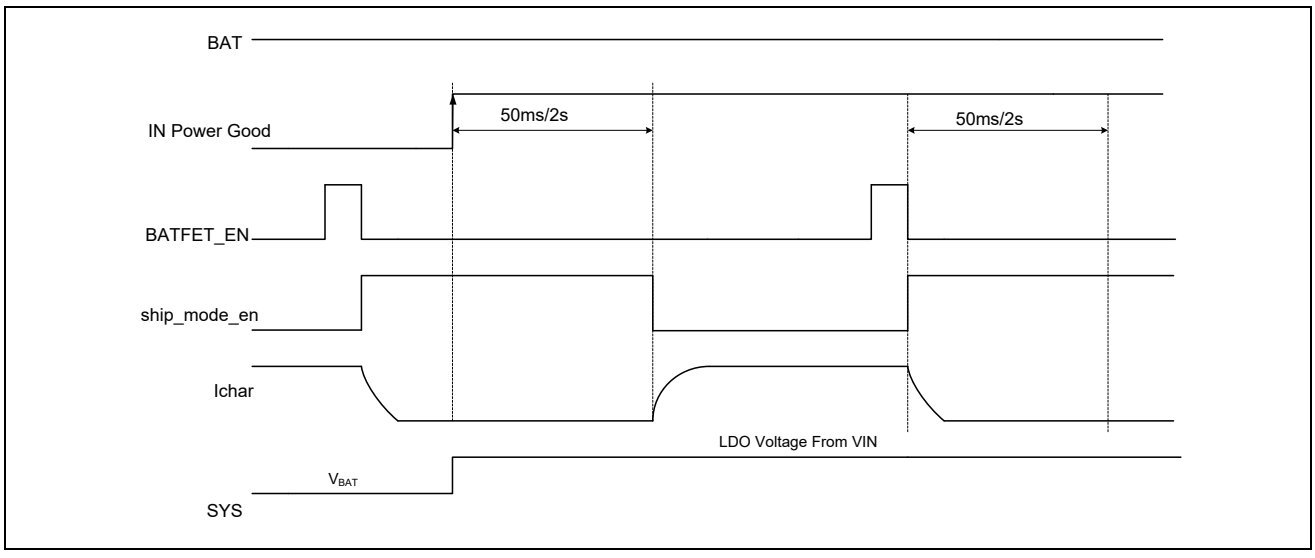



Figure 9. Enter Shipping mode and Exit Shipping mode by IN Good Signal

**2). Reset Mode**

The IC can use INT or Watchdog Overflow Signal to cut off the path from the IN to the system and battery to the system when system reset is needed.

Once the logic at INT is set to low for more than 8s/16s(Reg0A bit3) or watchdog time is overflow, the battery is disconnected from the system by turning off the LDO MOSFET and the battery MOSFET. At the same time SYS will be discharged by internal discharge circuit.

If we set Reg0A[4]=0, the INT exiting shipping mode and SYS reset function will be closed.

The off state lasts for 2s/4s(Reg0A bit2) for INT(keep low for more than 8s/16s), and only 4s for Watchdog Overflow Signal, then the LDO MOSFET and the battery MOSFET are turned on automatically, and the system is powered again. During the 2s/4s off period, INT pin voltage level could be high or low. The IC can reset the system by controlling INT (see Figure 10).

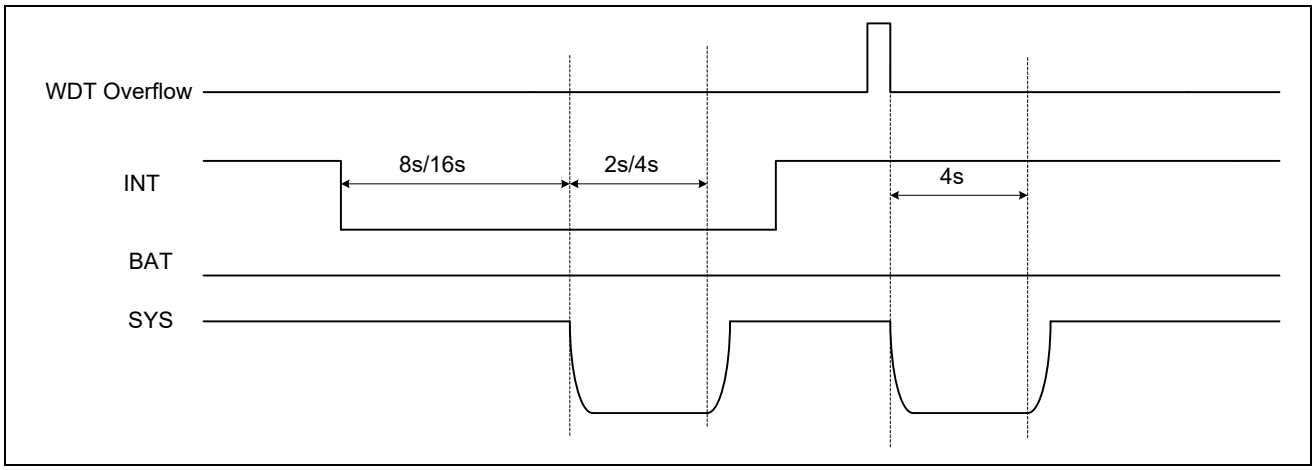



Figure 10. System Reset Function Operation Profile

## I²C REGISTER MAP

**Chip Address：1001000b (7bit) =** 48H

NOTE: 10010000b (8bit) = 90H(Writing Register mode)/10010001 (8bit) =91H(Reading Register Mode)

**Input Source Control Register/Address: 00H (Default: 1001 1111b)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Input Voltage Regulation | | | | |
| Bit 7 | IN_VSET[3] | 1b: 640mV | Read/write | Offset: 3.88V<br>Range:3.88V-5.08V<br>Default:4.60V(1001b) |
| Bit 6 | IN_VSET[2] | 1b: 320mV | | |
| Bit 5 | IN_VSET [1] | 1b: 160mV | | |
| Bit 4 | IN_VSET [0] | 1b: 80mV | | |
| Input Current Limit | | | | |
| Bit 3 | IN_ILIMT_SET[3] | 1b: 320mA | Read/write | Offset: 80mA<br>Range: 80mA-680mA<br>Default:680mA(1111b) |
| Bit 2 | IN_ILIMT_SET[2] | 1b: 160 mA | | |
| Bit 1 | IN_ILIMT_SET[1] | 1b: 80 mA | | |
| Bit 0 | IN_ILIMT_SET[0] | 1b: 40 mA | | |

**Power-On Configuration Register/Address: 01H (Default: 0010 0100b)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | REG_RST | 0b: keep current setting<br>1b: reset all the register | Read/write | Keep current setting(0b) |
| Bit 6 | WDT_RST | 0b: normal<br>1b: reset watchdog timer | Read/write | Normal(0b) |
| Bit 5 | LDO_EN (1) | 0b: disable LDO<br>1b: enable LDO | Read/write | enable(1b) |
| Bit 4 | LDO_MODE_SEL | 0b: LDO mode<br>1b: Switch mode | Read/write | LDO mode(0b) |
| Charger Configuration | | | | |
| Bit 3 | CHAR_EN | 0b: charge disabled<br>1b: charge enabled | Read/write | Charge Disabled (0b) |
| Battery UVLO Threshold | | | | |
| Bit 2 | BAT_UVLO_SET[2] | 1b: 0.4V | Read/write | Offset: 2.4V<br>Range: 2.4V-3.1V<br>Default: 2.8V (100b) |
| Bit 1 | BAT_UVLO_SET[1] | 1b: 0.2V | | |
| Bit 0 | BAT_UVLO_SET[0] | 1b: 0.1V | | |

***Note1***. This bit only controls the on and off of the LDO MOSFET.

**Charge Current Control Register/Address: 02H (Default: 0001 1110b)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | | Read/write | Reserved |
| Bit 6 | Reserved | | Read/write | Reserved |
| Charge Current Setting | | | | |
| Bit 5 | CHAR_ISET [5] | 1b: 256mA | Read/write | Offset: 8mA<br>Range: 8mA -512mA<br>Default:248mA(011110) |
| Bit 4 | CHAR_ISET [4] | 1b: 128mA | | |
| Bit 3 | CHAR_ISET [3] | 1b: 64mA | | |
| Bit 2 | CHAR_ISET [2] | 1b: 32mA | | |
| Bit 1 | CHAR_ISET [1] | 1b: 16mA | | |
| Bit 0 | CHAR_ISET [0] | 1b: 8mA | | |

**Discharge Current Limit/Address: 03H (Default: 0001 0011b)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | | Read/write | Reserved |
| Bit 6 | Reserved | | Read/write | Reserved |
| Bit 5 | Reserved | | Read/write | Reserved |
| BAT to SYS Discharge Current Limit (Note: Bit[4:0] can be set 11010~11111 and clamp to 2.67A) | | | | |
| Bit 4 | BATTOSYS_ISET [4] | 1b: 1600mA | Read/write | Offset: 170mA<br>Range: 170mA~2.67A<br>Valid range:<br>00001b ~11001b<br>Default: 2070mA(10011b) |
| Bit 3 | BATTOSYS_ISET [3] | 1b: 800mA | | |
| Bit 2 | BATTOSYS_ISET [2] | 1b: 400mA | | |
| Bit 1 | BATTOSYS_ISET [1] | 1b: 200mA | | |
| Bit 0 | BATTOSYS_ISET [0] | 1b: 100mA | | |

**Charge Voltage Control Register/Address: 04H (Default: 1010 0011b)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Battery Regulation Voltage | | | | |
| Bit 7 | BATREG_VSET[5] | 1b: 480mV | Read/write | Offset: 3.60V<br>Range: 3.60V~4.545V<br>Default: 4.2V<br>(101000b) |
| Bit 6 | BATREG_VSET[4] | 1b: 240mV | | |
| Bit 5 | BATREG_VSET[3] | 1b: 120mV | | |
| Bit 4 | BATREG_VSET[2] | 1b: 60mV | | |
| Bit 3 | BATREG_VSET[1] | 1b: 30mV | | |
| Bit 2 | BATREG_VSET[0] | 1b: 15mV | | |
| Trickle Charge Threshold | | | | |
| Bit 1 | TRICKLE_CHAR_VSET | 0b: 2.8V<br>1b: 3.0V | Read/write | 3.0V (1b) |
| Battery Recharge Threshold (below BATREG_VSET) | | | | |
| Bit 0 | BAT_RCHAR_VSET | 0b: 100mV<br>1b: 200mV | Read/write | 200mV (1b) |

**Charge Termination/Timer Control Register/Address: 05H (Default: 0111 1010b)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | WDT_WKMD | 0b: Watchdog Timer can only work in charge state<br>1b: Watchdog Timer can work in charge and discharge state | Read/write | Work in charge state(0b) |
| Termination Setting (the termination is allowed or not) | | | | |
| Bit 6 | BF_EN | 0b: disable<br>1b: enable | Read/write | Enabled(1b) |
| $I^2C$ Watchdog Timer Limit | | | | |
| Bit 5 | WDT_TSET[1] | 00b: disable timer<br>01b: 40s<br>10b: 80s<br>11b: 160s | Read/write | Enable timer(11b) |
| Bit 4 | WDT_TSET[0] | | | |
| Safety Timer Setting | | | | |
| Bit 3 | SAFET_EN | 0b: disable<br>1b: enable | Read/write | Enable timer (1b) |
| Constant Current Charge Timer | | | | |
| Bit 2 | CONSC_TSET[1] | 00b: 3hrs<br>01b: 5hrs<br>10b: 8hrs<br>11b: 12hrs | Read/write | 5hrs (01b) |
| Bit 1 | CONSC_TSET[0] | | | |
| Termination Timer Control<br>(when TERMI_TEN is enabled, the IC will not suspend the charge current after charge termination) | | | | |
| Bit 0 | TERMI_TEN | 0b: disable<br>1b: enable | Read/write | Disable(0b) |

**Miscellaneous Operation Control Register/Address: 06H (Default: 0100 1111b)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | | Read/write | Read/write |
| Bit 6 | SAFET_2X_EN | 0b: disable 2X extended safety timer during PPM<br>1b: enable 2X extended safety timer during PPM | Read/write | Enable (1b) |
| Bit 5 | BATFET_EN (2) | 0b: enable<br>1b: turn off | Read/write | Enable(0b) |
| Bit 4 | Reserved | - | Read only | Reserved |
| Bit 3 | NTC_EN | 0b: disable<br>1b: enable | Read/write | Enable(1b) |
| Bit 2 | PCB_OTP_EN | 0b: disable<br>1b: enable | Read/write | Enable(1b) |
| Thermal Regulation Threshold | | | | |
| Bit 1 | THERMALT_SET[1] | 00b: 60°C<br>01b: 80°C<br>10b: 100°C<br>11b: 120°C | Read/write | 120°C (11b) |
| Bit 0 | THERMALT_SET[0] | | | |

***Note2***. This bit controls the on and off of the battery MOSFET, including the charging and discharging.

**System Status Register/Address: 07H (Default: 0000 0000b)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | - | Read only | Reserved |
| Revision | | | | |
| Bit 6 | Reserved | - | Read only | Reserved |
| Bit 5 | Reserved | | | |
| Bit 4 | CHAR_STATUS [1] | 00b: not charging<br>01b: trickle charge<br>10b: charge<br>11b: charge done | Read only | Not charging (00b) |
| Bit 3 | CHAR_STATUS [0] | | | |
| Bit 2 | PPM_EN | 0b: no PPM<br>1b: In PPM | Read only | No PPM (0b)<br>(no power-path management happens) |
| Bit 1 | IN_POWER_GOOD | 0b: in power good<br>1b: in power fail | Read only | In power good (0b) |
| Bit 0 | THERM_STR | 0b: no thermal regulation<br>1b: in thermal regulation | Read only | Normal (0b) |

***Note3***. The 07H register is a real-time monitoring and the fault state is not latched.

**Fault Register/Address: 08H (Default: 0000 0000)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | | Read only | Reserved |
| Bit 6 | WDT_FAULT | 0b: normal<br>1b: watchdog timer expiration | Read only | Normal (0b) |
| Bit 5 | VIN_FAULT | 0b: normal<br>1b: input fault (OVP or UVP of IN Voltage) | Read only | Normal (0b) |
| Bit 4 | THEM_SD | 0b: normal<br>1b: thermal shutdown | Read only | Normal (0b) |
| Bit 3 | BAT_FAULT | 0b: normal<br>1b: battery OVP | Read only | Normal (0b) |
| Bit 2 | SAFET_FAULT | 0b: normal<br>1b: safety timer expiration | Read only | Normal (0b) |
| Bit 1 | NTCH_FAULT | 0b: normal<br>1b: NTC hot | Read only | Normal (0b) |
| Bit 0 | NTCL_FAULT | 0b: normal<br>1b: NTC cold | Read only | Normal (0b) |

***Note4***.WDT_FAULT is cleared after the Reg01[6]=1 and the host should read the Reg08.
VIN_FAULT、THEM_SD、BAT_FAULT、SAFET_FAULT are cleared after the host reads the Reg08
NTC_FAULT is not latched and always reports the current thermistor conditions.

**System output voltage / Pre-Charge/Termination Current /Address: 09H (Default: 0011 1001b)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | | Read only | Reserved |
| System Output Voltage Regulation | | | | |
| Bit 6 | SYS_VSET[3] | 1b: 400mV | Read/write | Offset: 4.25V<br>Range: 4.25V-5.0V<br>Default: 4.6V (0111b) |
| Bit 5 | SYS_VSET[2] | 1b: 200mV | | |
| Bit 4 | SYS_VSET[1] | 1b: 100mV | | |
| Bit 3 | SYS_VSET[0] | 1b: 50mV | | |
| Trickle Current /termination current (Note: Bit[2:0] can not be set to 010 when CHAR_ISET⩾264mA) | | | | |
| Bit 2 | TRICKLE_CHAR_ISET[2] | 000b: 1mA<br>001b: 2mA<br>010b: 4mA<br>011b: 10mA<br>100b: 16mA<br>101b: 22mA<br>110b: 28mA<br>111b: 34mA | Read/write | Range: 1mA-34mA<br>Default: 2mA (001b) |
| Bit 1 | TRICKLE_CHAR_ISET[1] | | | |
| Bit 0 | TRICKLE_CHAR_ISET[0] | | | |

**Debounce Time for SYS Reset and Exit Shipmode /Address: 0AH (Default: 0011 1110)**

| Bit | Symbol | Description | Read/Write | Default |
|---|---|---|---|---|
| Bit 7 | Reserved | | | Reserved |
| Bit 6 | Reserved | | | Reserved |
| Bit 5 | INT_OUTEN | INT Port Output Function Enable Signal(low level to mask all interrupt output function)<br>0b: Disable 1b:Enable | Read/write | Enable(1b) |
| Bit 4 | INT_ILOW_FUN_EN | INT Port Input Low Level Function Enable Signal(low level to mask INT Port Exiting Shipping mode and Producing SYS Reset)<br>0b: Disable 1b: Enable | Read/write | Enable(1b) |
| Bit 3 | INT_RESET_TSET | INT Port Low Level Time Setting for Producing Reset Signal in SYS Port<br>0b:8s 1b:16s | Read/write | 16s(1b) |
| Bit 2 | SYS_RESET_TSET | SYS Port Keeping Low Reset Level Time Setting when Watchdog Overflow or INT Port Keep 8/16s Low Level<br>0b:2s 1b:4s | Read/write | 4s(1b) |
| Bit 1 | INT_EXIT_SHIP_TSET | INT Port Low Level Time Setting for Exit Shipping mode<br>0b:50ms 1b:2s | Read/write | 2s(1b) |
| Bit 0 | IN_ EXIT_SHIP_TSET | IN Port Power Good Time Setting for Exit Shipping mode<br>0b:50ms 1b:2s | Read/write | 50ms(0b) |

## Serial Port Interface ($I^2C$)

### Bus Interface

Baseband Processor can transmit data with ET9562 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

### Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

### Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

### Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

### Acknowledge

During the writing mode, ET9562 will send a low level response signal with one period width to the SDA port. During the reading mode, ET9562 will not send response signal and the host will send a high response signal one period width to the SDA.

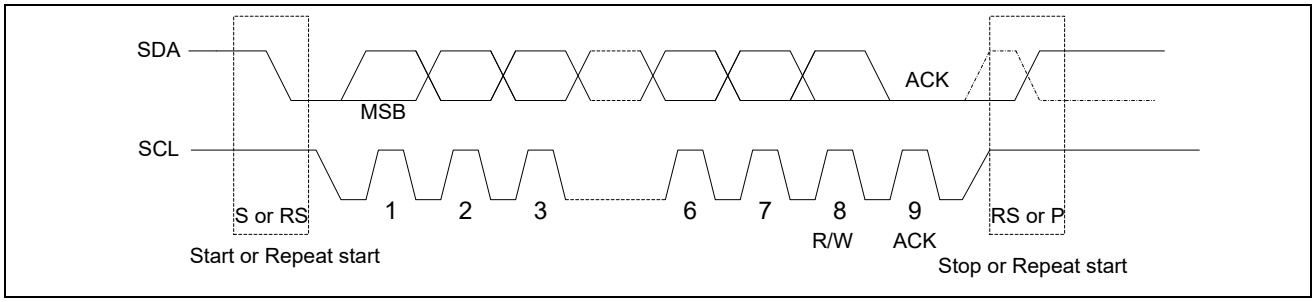



Figure 11. $I^2C$ write mode

- ACK=Acknowledge
- MSB=Most Significant Bit
- S=Start Conditions
- RS=Restart Conditions
- P=Stop Conditions
- Fastest Transmission Speed =400KBITS/S
- Restart: SDA-level turnover as expressed by the dashed line waveform

**Chip Address：** 10010000b(Writing Register mode) / 10010001b(Reading Register Mode)

## I²C Writing Command Register Interface Protocol (continuous):

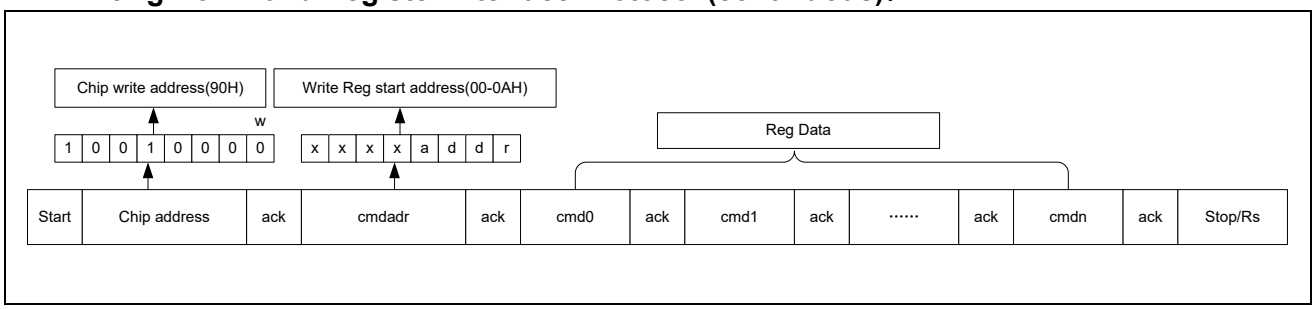



Figure 12. I²C Writing Command Register(continuous)

- Start=Start Conditions
- Chip address=Write register address =1001000+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(xxxx + REG's 4bit addr)
- ack=Acknowledge
- Reg data 0 = cmd0(Command data0)
- ack=Acknowledge
- ……
- Reg data n =cmdn(Command datan)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

## I²C Writing Command Register Interface Protocol (single):

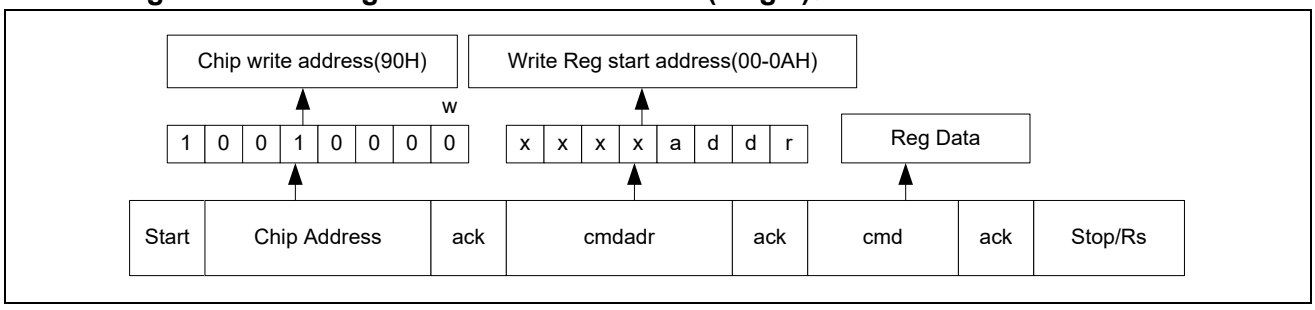



Figure 13. I²C Writing Command Register(single)

- Start=Start Conditions
- Chip address =Write register address=1001000+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(xxxx + REG's 4bit addr)
- ack=Acknowledge
- Reg data= cmd(Command data)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

## I²C Reading Command Register Interface Protocol:

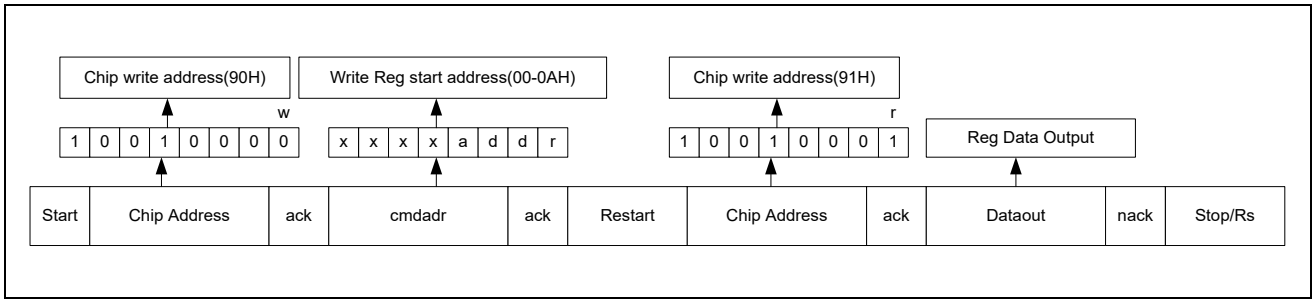



Figure 14. I²C Reading Command Register

- Start=Start Conditions
- Chip address =Write register address=1001000+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(xxxx + REG's 4bit addr)
- ack=Acknowledge
- Restart=Restart condition
- Chip address Read register address=1001000+1(r)b
- ack=Acknowledge
- Dataout=Register data output
- nack=No Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Characteristic | | Range | | Unit |
|---|---|---|---|---|
| VIN, Supply Input Voltage | | -0.3~24 | | V |
| Other Pins | | -0.3~6.0 | | V |
| Maximum Continuous Current of IN to BAT | | <1.0 | | A |
| Maximum Continuous Current of IN to SYS | | <1.5 | | A |
| Maximum Continuous Current of BAT to SYS | | <3.0 | | A |
| Power Dissipation at $T_A$= +70°C | | <1.5 | | W |
| Storage Junction Temperature | | -60~150 | | °C |
| Thermal Resistance | | 55 | | °C /W |
| Operating Temperature Range | | -40~85 | | °C |
| Soldering Temperature (reflow) | | <+260 | | °C |
| Junction Temperature | | <+150 | | °C |
| Electrostatic Discharge Capability | Human Body Model | All Pins | >2.0 | kV |
| | Charged Device Model | All Pins | >1.0 | kV |

## Electrical Characteristics

Unless otherwise noted, typical values are at $V_{IN}$=5V, $V_{BAT}$=4V, $T_A$=25°C.

| Symbol | Parameters | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supply | | | | | | |
| $V_{IN}$ | Input voltage | | | | 20 | V |
| $V_{IN}$ | Input operation voltage | | 4.35 | 5 | 5.5 | V |
| $I_{IN1}$ | Supply current at IN, charge enable | $V_{IN}$=5.5V, $I_{CHG}$=0A, $I_{SYS}$=0A,charge enable,BAT=4.3V | | 550 | 700 | uA |
| $I_{IN2}$ | Supply current at IN, charge disable | $V_{IN}$=5.5V, $I_{CHG}$=0A, $I_{SYS}$=0A, charge disable, BAT=4.3V | | 450 | 600 | uA |
| $I_{IN3}$ | Supply current at IN, LDO disable | $V_{IN}$=5.5V, $I_{CHG}$=0A, $I_{SYS}$=0A, LDO disable, BAT=4.3V | | 350 | 500 | uA |
| $I_{BAT}$ | Supply current at BAT | $V_{IN}$=0V, $I_{SYS}$=0A, $V_{BAT}$=4.35V, disable PCB OTP function, do not include the current from external NTC resistor | | 15 | 18 | uA |
| | | $V_{IN}$=0V, $I_{SYS}$=0A, $V_{BAT}$=4.35V, enable PCB OTP function, do not include the current from external NTC resistor, watchdog is not available in discharge mode | | 22 | 25 | uA |
| | | $V_{IN}$=0V, $I_{SYS}$=0A, $V_{BAT}$=4.35V, enable PCB OTP function, do not include the current from external NTC resistor, watchdog is available in discharge mode | | 25 | 30 | uA |
| | | $V_{SYS}$=$V_{IN}$=0V, $I_{SYS}$=0A, $V_{BAT}$=4.35V, Set disconnect mode. | | 1.5 | 2 | uA |
| $V_{IN\_OVP}$ | Input over-voltage protect threshold | Input rising threshold | 5.85 | 6.0 | 6.15 | V |
| | OVP threshold hysteresis | Input Voltage Falling | | 350 | | mV |
| $V_{UV\_IN}$ | Input under-voltage threshold | Input rising threshold | 3.8 | 3.9 | 4.0 | V |
| | Input UVLO hysteresis | | | 170 | | mV |

## Electrical Characteristics(Continued)

Unless otherwise noted, typical values are at $V_{IN}$=5V, $V_{BAT}$=4V, $T_A$=25°C.

| Symbol | Parameters | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{UV\_BAT}$ | Battery under-voltage threshold | Battery voltage falling. Reg01[2:0]=100b | 2.6 | 2.8 | 3.0 | V |
| | Battery UVLO range | | 2.4 | | 3.1 | V |
| | Battery UVLO hysteresis | | | 210 | | mV |
| $V_{BAT\_OVP}$ | Battery over-voltage protect threshold | Battery voltage rising, higher than $V_{BATREG\_VSET}$ | | 130 | | mV |
| | | Battery voltage falling, higher than $V_{BATREG\_VSET}$ | | 70 | | mV |
| Power Path Management | | | | | | |
| $V_{SYS\_REG}$ | Regulated system output voltage | $V_{IN}$=5.5V, $I_{SYS}$=10mA, $I_{CHG}$=0A Reg09[6:3]=0111b, default | 4.50 | 4.60 | 4.70 | V |
| | System output voltage range | | 4.25 | | 5.0 | V |
| $I_{IN\_LIM}$ | Input current limit | Default Reg00[3:0]=1111b | 600 | 640 | 680 | mA |
| | Input current limit range | | 80 | | 680 | mA |
| $V_{IN\_REG}$ | Input voltage regulation threshold | Default Reg00[7:4]=1001b | 4.45 | 4.60 | 4.75 | V |
| | Input voltage regulation range | | 3.88 | | 5.08 | V |
| $V_{SYS}$ | System output voltage | Charging mode, $V_{IN}$=5.5V, $V_{BAT}$=3.7V, default Reg09[6:3]=0111b | 4.50 | 4.60 | 4.70 | V |
| | | Battery supply mode, $V_{BAT}$=3.7V, $I_{BAT}$=100mA | 3.6 | | | V |
| | | $V_{IN}$<$V_{UV\_IN}$ and $V_{BAT}$<$V_{UV\_BAT}$ | | 0 | | V |
| $R_{ON\_SYS}$ | IN to SYS switch on resistance | $V_{SYS}$=4.6V, $I_{SYS}$=100mA | | 150 | 250 | mΩ |
| $R_{ON\_BAT}$ | BAT to SYS switch on resistance | $V_{IN}$<2V, $V_{BAT}$=3.5V, $I_{SYS}$=100mA | | 100 | 150 | mΩ |
| $I_{BAT\_MAX}$ | BAT to SYS current limit | Reg03[4:0]=10011b | 1770 | 2070(5) | 2370 | mA |
| | BAT to SYS current limit range | | 170 | | 2670(5) | mA |
| $I_{BAT\_LEK}$ | BAT to SYS leakage current | $V_{BAT}$=4.5V, $V_{IN}$=$V_{SYS}$=0V, Disconnect mode. | | | 1 | uA |

## Electrical Characteristics(Continued)

Unless otherwise noted, typical values are at $V_{IN}$=5V, $V_{BAT}$=4V, $T_A$=25°C.

| Symbol | Parameters | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SYS\_LEK}$ | SYS to BAT leakage current | $V_{SYS}$=5.0V, $V_{IN}$=4.5V, $V_{BAT}$=0V | | | 1 | uA |
| $T_{INT}$ | BAT discharge function controlled by INT | INT pull-low lasting time to turn off the battery discharge function | | 16 | | s |
| | | Battery MOSFET lasts for the off time duration before auto-on | | 4 | | s |
| Battery Charger | | | | | | |
| $V_{BAT\_REG}$ | Battery voltage regulation range | Programmed by $I^2C$ $V_{SYS\_REG}$>$V_{BAT\_REG}$+200mV | 3.600 | | 4.545 | V |
| $V_{BAT}$ | Default battery regulation voltage | Reg04[7:2]=101000b | 4.175 | 4.200 | 4.225 | V |
| $I_{CHG}$ | Battery charge current range | $V_{IN}$=5V, $V_{BAT}$=3.8V step=8mA | 8 | | 512 | mA |
| | Default charge current | $V_{IN}$=5V, $V_{BAT}$=3.8V Reg02[5:0]=011110b | 235 | 248 | 261 | mA |
| | Charge current | $V_{IN}$=5V, $V_{BAT}$=3.8V Reg02[5:0]=001010b | 83 | 88 | 93 | mA |
| | | $V_{IN}$=5V, $V_{BAT}$=3.8V Reg02[5:0]=000000b | 7 | 8 | 9 | mA |
| | Charging current thermal foldback threshold | Junction Temperature Regulation Reg06[1:0]=11b | | 120[(5)] | | °C |
| $I_{TC}$ | Trickle current range | Programmed range Reg09H[2:0] | 1 | | 34 | mA |
| $I_{BF}$ | End of charge current threshold | $I_{CHG}$≤256mA, $I_{TC\_SETTING}$=2mA Reg02bit[5]=0b | 1 | 2 | 3 | mA |
| | | $I_{CHG}$≤256mA, $I_{TC\_SETTING}$=22mA Reg02bit[5]=0b | 18 | 22 | 26 | mA |
| | | $I_{CHG}$≥264mA, $I_{TC\_SETTING}$=2mA Reg02bit[5]=1b | 2 | 4 | 6 | mA |
| | | $I_{CHG}$≥264mA, $I_{TC\_SETTING}$=22mA Reg02bit[5]=1b | 39 | 44 | 49 | mA |
| $V_{BAT\_LOW}$ | Trickle charge threshold voltage | $V_{BAT}$ rising, set 3.0V | 2.8 | 3.0 | 3.2 | V |
| | Trickle voltage hysteresis | | | 60 | | mV |

## Electrical Characteristics(Continued)

Unless otherwise noted, typical values are at $V_{IN}$=5V, $V_{BAT}$=4V, $T_A$=25°C.

| Symbol | Parameters | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{RECHG}$ | Recharge threshold below $V_{BAT\_REG}$ | Reg04[0]=0b | 70 | 100 | 130 | mV |
| | | Reg04[0]=1b | 160 | 200 | 240 | mV |
| Thermal Protection | | | | | | |
| | Thermal shutdown rising threshold | | | 150(5) | | °C |
| | OTP Threshold Hysteresis | | | 20(5) | | °C |
| $I_{NTC}$ | NTC output current | NTC=3.0V | | 500 | | nA |
| $V_{COLD}$ | NTC cold temp rising threshold | As a percentage of $V_{DD}$ | 63 | 65 | 67 | % |
| | NTC cold temp rising threshold hysteresis | | | 60 | | mV |
| $V_{HOT}$ | NTC hot temp falling threshold | As a percentage of $V_{DD}$ | 31 | 33 | 35 | % |
| | NTC hot temp falling threshold hysteresis | | | 70 | | mV |
| $V_{HOT\_PCB}$ | NTC hot temp falling threshold for PCB OTP | As a percentage of $V_{DD}$ | 30 | 32 | 34 | % |
| | NTC hot temp falling threshold hysteresis for PCB OTP | | | 85 | | mV |
| Logic I/O Characteristics | | | | | | |
| $V_{IL}$ | Low Logic voltage threshold | | | | 0.4 | V |
| $V_{IH}$ | High Logic voltage threshold | | 1.3 | | | V |
| Digital Clock and Watchdog Timer | | | | | | |
| $F_{DIG}$ | Digital clock | | | 32 | | kHz |
| $t_{WDT}$ | Watchdog Timer | Reg05[5:4]=11b | | 160 | | s |

***Note5***. Guaranteed by design and characterization. Not a FT item.

## I²C mode Timing

| Symbol | Parameters | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{SCL}$ | SCL Clock Frequency | 0 | - | 400 | kHz |
| $t_{BUF}$ | Bus Free Time Between a STOP and START Condition | 1.3 | - | - | μs |
| $t_{HD:STA}$ | Hold Time(Repeated) START Condition | 0.6 | - | - | μs |
| $t_{LOW}$ | Low Period of SCL Clock | 1.3 | - | - | μs |
| $t_{HIGH}$ | HIGH Period of SCL Clock | 0.6 | - | - | μs |
| $t_{SU:STA}$ | Setup Time for a Repeated START Condition | 0.6 | - | - | μs |
| $t_{HD:DAT}$ | Data Hold Time | - | - | 0.9 | μs |
| $t_{SU:DAT}$ | Data Setup Time | 100 | - | - | ns |
| $t_R$ | Data Hold Time2 | - | 20+0.1Cb[(6)] | 300 | ns |
| $t_F$ | Data Hold Time2 | - | 20+0.1Cb[(6)] | 300 | ns |
| $t_{SU:STO}$ | Setup Time for STOP Condition | 0.6 | - | - | μs |

***Note6***. Cb=total capacitance of one bus line in PF.

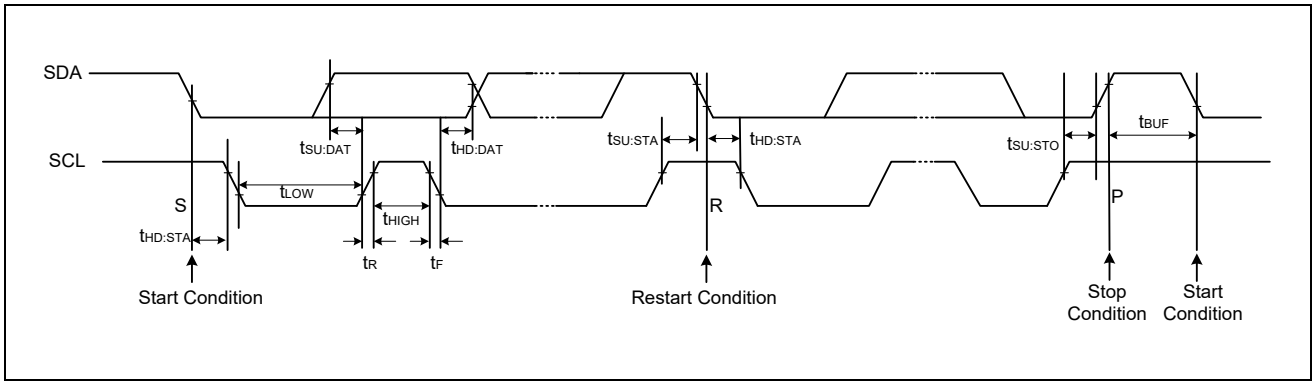
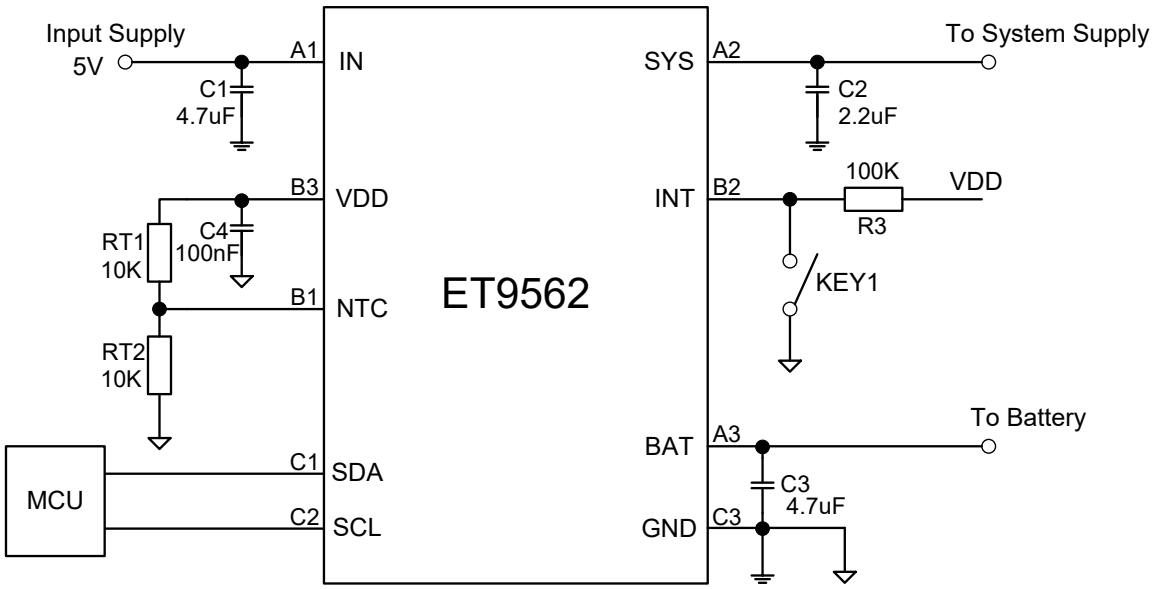



Figure 15. I²C mode Timing Diagram

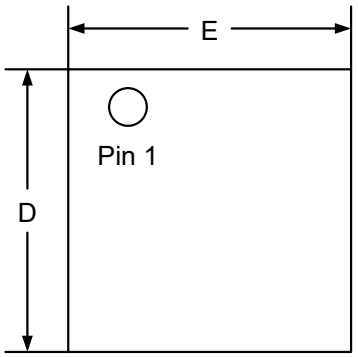
## Typical Application Circuits



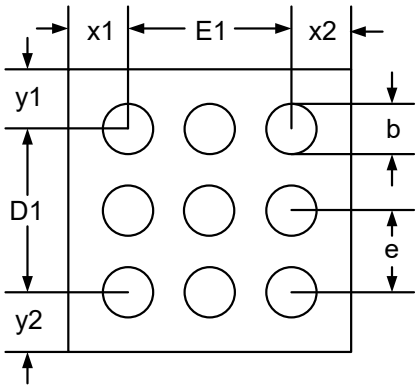

***Note****. This electric circuit only supplies for reference.

## Package Dimension

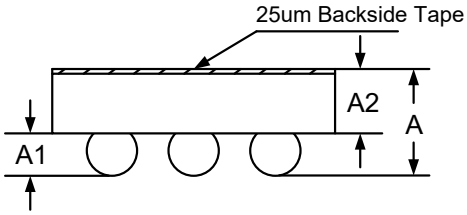
CSP9




TOP VIEW
(MARK SIDE)




BOTTEM VIEW
(BALL SIDE)

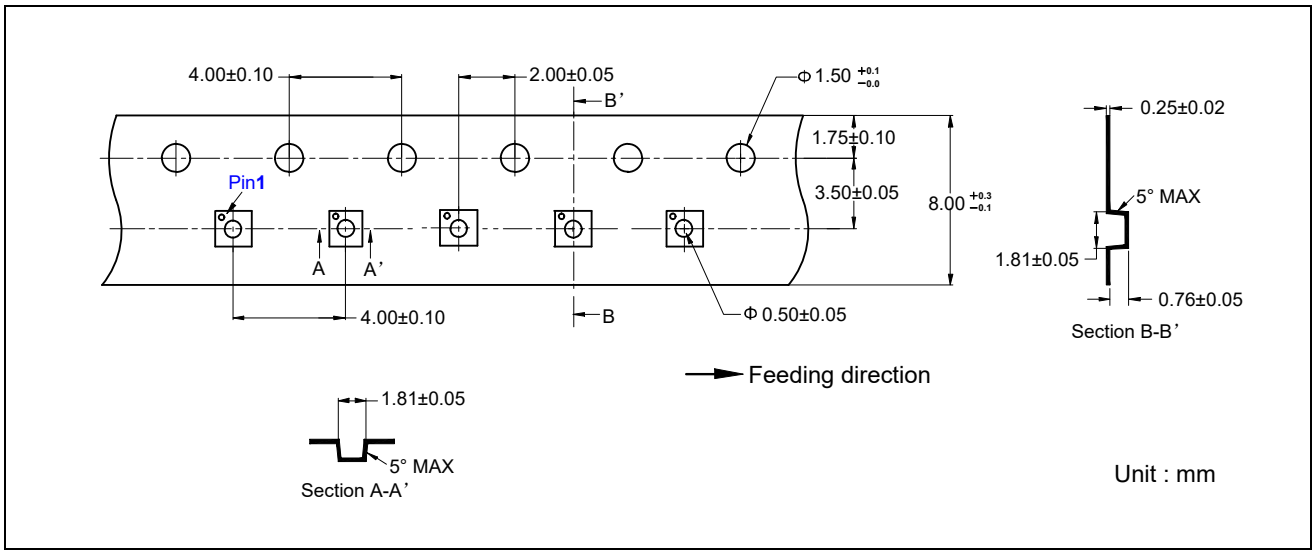



SIDE VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.580 | 0.625 | 0.670 |
| A1 | 0.220 | 0.245 | 0.270 |
| A2 | 0.355 | 0.380 | 0.405 |
| D | 1.660 | 1.690 | 1.720 |
| D1 | | 1.000 REF | |
| E | 1.660 | 1.690 | 1.720 |
| E1 | | 1.000 REF | |
| b | 0.285 | 0.310 | 0.335 |
| e | | 0.500 REF | |
| x1 | | 0.345 REF | |
| x2 | | 0.345 REF | |
| y1 | | 0.345 REF | |
| y2 | | 0.345 REF | |

## Tape Information



## Revision History and Checking Table

| Version | Date | Revision Item | Modifier | Function & Spec Checking | Package & Tape Checking |
|---|---|---|---|---|---|
| 1.0 | 2018-12-18 | Preliminary Version | Yang Zhen | Yang Zhen | Zhu Jun Li |
| 1.1 | 2019-4-29 | Detail Description | Sun Si Bing | Sun Si Bing | Zhu Jun Li |
| 1.2 | 2019-8-15 | 1.Add in_power_good and char finish interrupt signal; 2.change CHAR_EN from 1b(enable) to 0b(disable) 3.change TRICKLE_CHAR_ISET[2:0] from 101b(22mA) to 001b(2mA) 4.change IN_ EXIT_SHIP_TSET form 1b(2s) to 0b(50ms); 5.Add INT port input and output function enable control bit; 6.Change Exit shipping mode method (add signal edge and timer judgement) | Sun Si Bing | Sun Si Bing | Zhu Jun Li |
| 1.3 | 2019-12-04 | 1.Add SYS discharge and INT function description. 2.Modify $I_{BAT}$ parameter in electrical characteristics | Xia Yong Jie | Xia Yong Jie | Zhu Jun Li |
| 1.4 | 2020-2-13 | Add $I_{IN2}$、$I_{IN3}$ parameter | Xia Yong Jie | Xia Yong Jie | Zhu Jun Li |
| 1.5 | 2020-3-10 | Add 90mA, 10mA charge current parameter, adjust BAT to SYS current limit | Xia Yong Jie | Xia Yong Jie | Zhu Jun Li |
| 1.6 | 2020-06-16 | Update charge current step to 8mA | Xia Yong Jie | Xia Yong Jie | Zhu Jun Li |
| 1.7 | 2023-05-08 | 1.Update Typeset 2.Add termination current register and BAT to SYS discharge current Limit register note description | Yin Peng | Xia Yong Jie | Liu Jia Ying |
| 1.8 | 2023-10-23 | Add Marking | Shibo | Xia Yong Jie | Liu Jia Ying |
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