10MHz, RRIO, CMOS Operational Amplifier for Cost-Sensitive Systems

General Description

ET85602 is a dual low-voltage (1.8 V to 5.5 V) operational amplifier (op amp) with rail-to-rail input- and output-swing capabilities. The device is highly cost-effective solutions for applications where low-voltage operation, a small footprint, and high capacitive load drive are required. Although the capacitive load drive of the ET85602 is 100 pF, the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler. The op amp is designed specifically for low-voltage operation (1.8 V to 5.5 V).

ET85602 is specified for the extended industrial/automotive temperature range (-40°C to +125°C). It is available in SOP8 / MSOP8 / TSOT23-8 / DFN8(2×2) / DFN8(3×3) packages.

Features

- Rail-to-rail input and output
- Low input offset voltage: ±0.3 mV
- Unity-gain bandwidth: 10 MHz
- Low broadband noise: 10 nV/$\sqrt{Hz}$
- Low input bias current: ±1 pA
- Low quiescent current: 550 μA
- Unity-gain stable
- Internal RFI and EMI filter
- Operational supply voltage range 1.8 V to 5.5V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance
- Extended temperature range: -40°C to 125°C

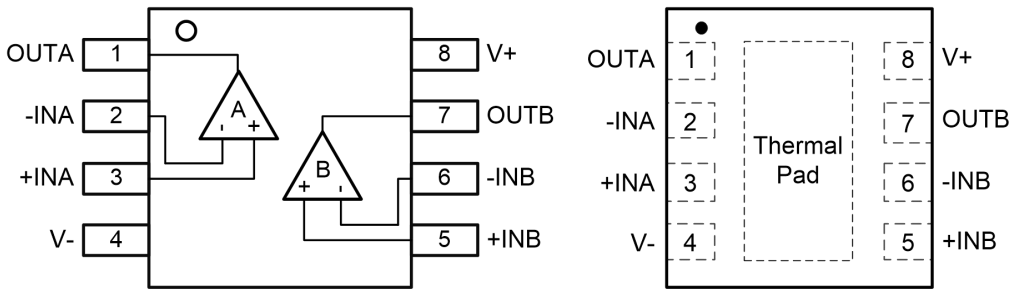
Applications

- Temperature sensors
- Smoke detectors
- Wearable devices
- Laptop computers
- Sensor signal conditioning
- Power modules
- Active filters
- Low-side current sensing

Device information

Part No.	Package	Packing Option	Marking	MSL
ET85602M	SOP8	Tape and Reel , 4k/Reel	85602 XXXXX	3
ET85602U	MSOP8	Tape and Reel , 4k/Reel	85602 XXXXX	3
ET85602E	TSOT23-8	Tape and Reel , 3k/Reel	802E XXXXX	3
ET85602Y1	DFN8(2×2)	Tape and Reel , 3k/Reel	802Y XXXXX	1
ET85602Y2	DFN8(3×3)	Tape and Reel , 3k/Reel	802Y XXXXX	3

Pin Configuration



SOP8/MSOP8/TSOT23-8 DFN8(2×2)/DFN8(3×3)

Top View

Pin Function

Pin Number	Symbol	Descriptions
1,7	OUT	Output
4	V-	Negative supply
3,5	+IN	Non-inverting input
2,6	-IN	Inverting input
8	V+	Positive supply
-	Thermal Pad	Connect thermal pad to V-

Functional Description

Rail-to-Rail Input

The input common-mode voltage range extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage.

Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the ET85602 delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are only stress ratings, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Symbol	Parameter	Value	Unit
V_S	Supply Voltage:(V+) - (V-)	0 to 6	V
V_{IC}	Common-mode Input Voltage(1)	(V-)-0.5 to (V+)+0.5	V
V_{ID}	Differential Input Voltage(1)	(V+) - (V-)+0.2	V
I_{IN}	Signal input terminals Current(1)	-10 to +10	mA
I_{SC}	Output short-circuit current(2)	Continuous	mA
V_{ESD}	ESD (Human Body Model)	±2500	V
	ESD (Charged Device Model)	±1000	V
T_{STG}	Storage Temperature Range	-65 to +150	°C
$T_{J(MAX)}$	Max Junction Temperature Range	+150	°C

Note1: Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.

Note2: Short-circuit to ground, one amplifier per package.

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	SOP8	Thermal Characteristics, Thermal Resistance, Junction-to-Air	160	°C/W
	MSOP8		200	°C/W
	TSOT23-8		185	°C/W
	DFN8(2×2)		80	°C/W
	DFN8(3×3)		45	°C/W

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_S	Supply Voltage: (V+) - (V-)	1.8(±0.9) ~ 5.5(±2.75)	V
T_A	Operating Temperature Range	-40 ~ +125	°C

Electrical Characteristics

V_S = (V+) – (V-) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V), T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{CM} = V_{OUT} = V_S/2 (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.3	±2	mV
		V_S = 5 V, T_A = -40°C to 125°C			±2.5	
$\Delta V_{OS}/\Delta T$	Input offset voltage vs temperature	V_S = 5 V, T_A = -40°C to 125°C		±0.53		µV/°C
PSRR	Input offset voltage vs power supply	V_S = 1.8 to 5.5 V, V_{CM} = (V-)		±7	±80	µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 1.8 V to 5.5 V	(V-)-0.1		(V+)+0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V-) - 0.1 V < V_{CM}< (V+) - 1.4 V, T_A = –40°C to 125°C	70	103		dB
		V_S = 5.5 V, VCM = –0.1 V to 5.6 V, T_A = -40°C to 125°C	57	87		
		V_S = 1.8 V, (V–) – 0.1 V < VCM < (V+) – 1.4 V, T_A = -40°C to 125°C		88		
		V_S = 1.8 V, VCM = –0.1 V to 1.9 V, T_A = -40°C to 125°C		81		
INPUT BIAS CURRENT						
I_B	Input bias current	V_S = 5 V		±1		pA
I_{OS}	Input offset current			±1		pA
NOISE						
E_n	Input voltage noise (peak to peak)	f = 0.1 Hz to 10 Hz, V_S = 5 V		4.77		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz, V_S = 5 V		16		nV/√Hz
		f = 10 kHz, V_S = 5 V		10		
i_n	Input current noise density[3]	f = 1 kHz, V_S = 5 V		23		fA/√Hz
INPUT CAPACITANCE						
C_{ID}	Differential[3]			2		pF
C_{IC}	Common-mode[3]			4		pF

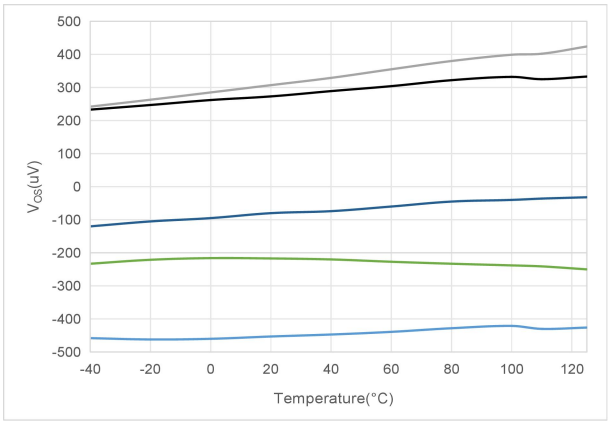
Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, R_L = 10 kΩ (V-) + 0.04 V < V_O< (V+) - 0.04 V		100		dB
		V_S = 5.5 V, R_L = 10 kΩ (V-) + 0.1 V < V_O< (V+) - 0.1 V	104	130		
		V_S = 1.8 V, R_L = 2 kΩ (V-) + 0.06 V < V_O< (V+) - 0.06 V		100		
		V_S = 5.5 V, R_L = 2 kΩ (V-) + 0.15 V < V_O< (V+) – 0.15 V		130		
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V_S = 5 V, G =+1		10		MHz
φ_m	Phase margin	V_S = 5 V, G =+1		55		°
SR	Slew rate	V_S = 5 V, G =+1		6		V/μs
t_S	Settling time(3)	To 0.1%, V_S = 5 V, 2V step, G = +1, C_L = 100 pF		0.5		μs
		To 0.01%, V_S = 5 V, 2V step, G = +1, C_L = 100 pF		1		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.2		μs
THD+N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz,		0.0008		%
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ			20	mV
		V_S = 5.5 V, R_L = 2 kΩ			60	
I_{SC}	Short-circuit current	V_S = 5 V		±50		mA
Z_O	Open-loop output impedance(3)	V_S = 5 V, f = 10MHz		100		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5 V		550	750	μA
		I_O = 0 mA, V_S = 5.5 V, T_A = -40°C to 125°C			800	

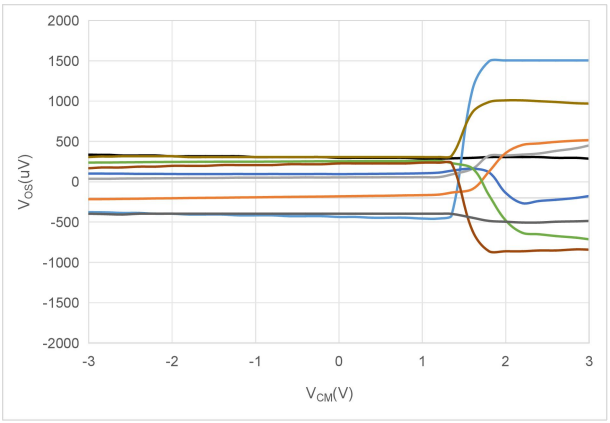
Note3: Guaranteed by design.

Typical Characteristics

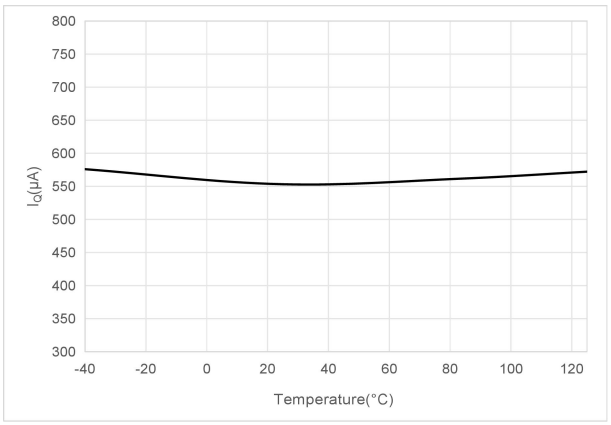
V_S = 5.5 V(±2.75V), V_{CM} = V_{OUT} = V_S/2, and R_L = 10kΩ connected to V_S/2,T_A = 25°C (unless otherwise noted)



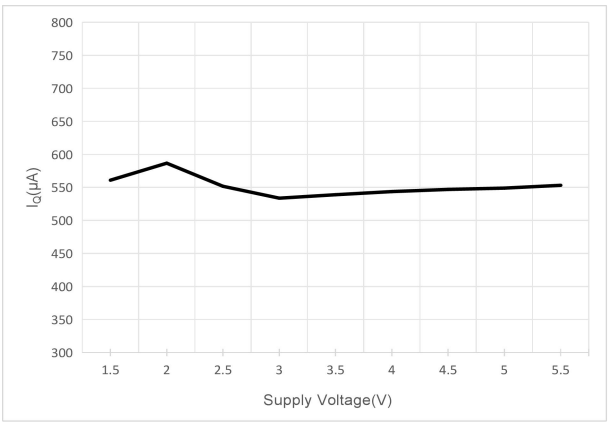
Offset Voltage vs Temperature



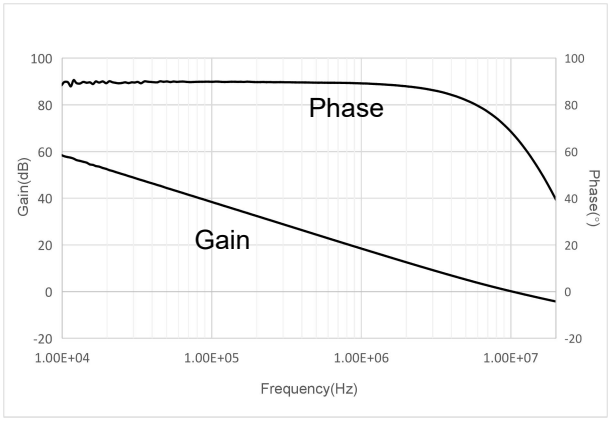
Offset Voltage vs Common-Mode Voltage



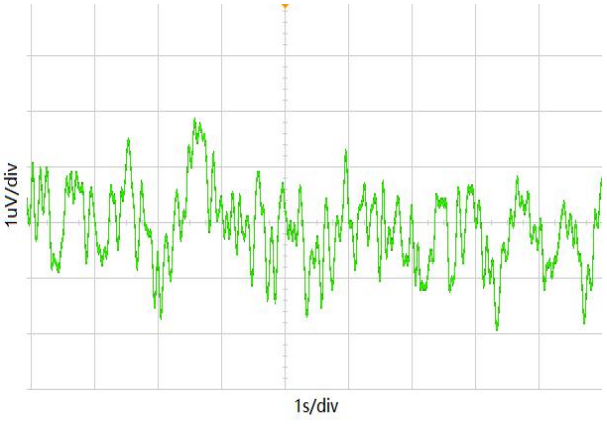
Quiescent Current vs Temperature



Quiescent Current vs Supply Voltage

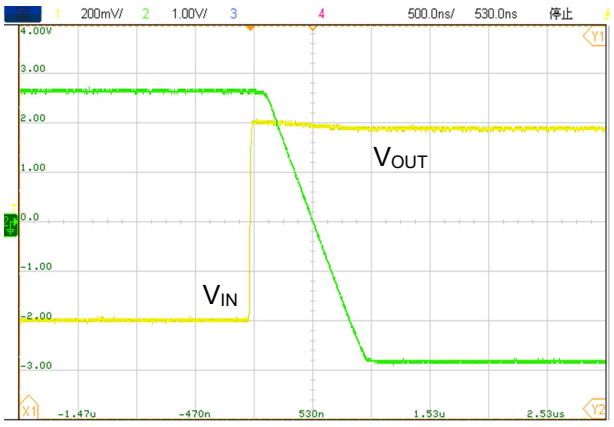


Open-Loop Gain and Phase vs Frequency



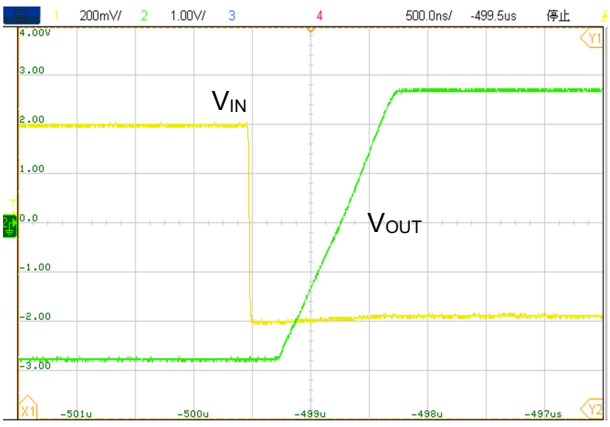
0.1 Hz to 10 Hz Noise

Typical Characteristics (Continued)



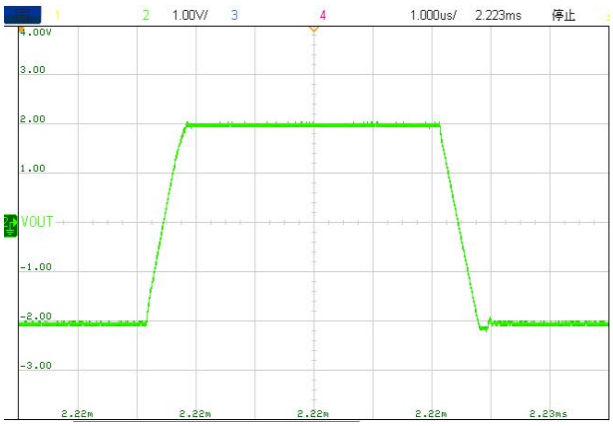
Positive Overload Recovery

(G = -10)



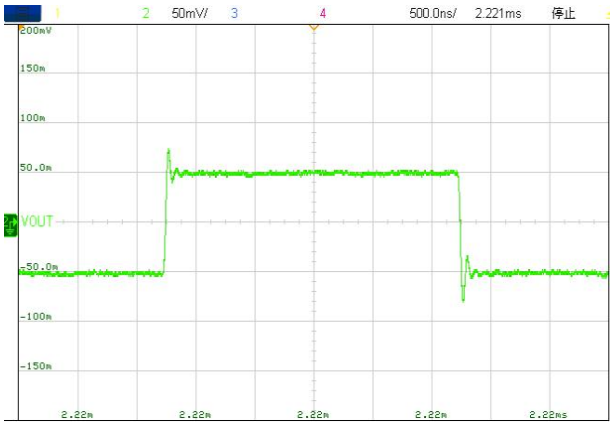
Negative Overload Recovery

(G = -10)



Large-Signal Step Response

(G = +1)



Small-Signal Step Response(100 mV)

(G = +1,R_L = 10 kΩ,C_L = 100 pF)

Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

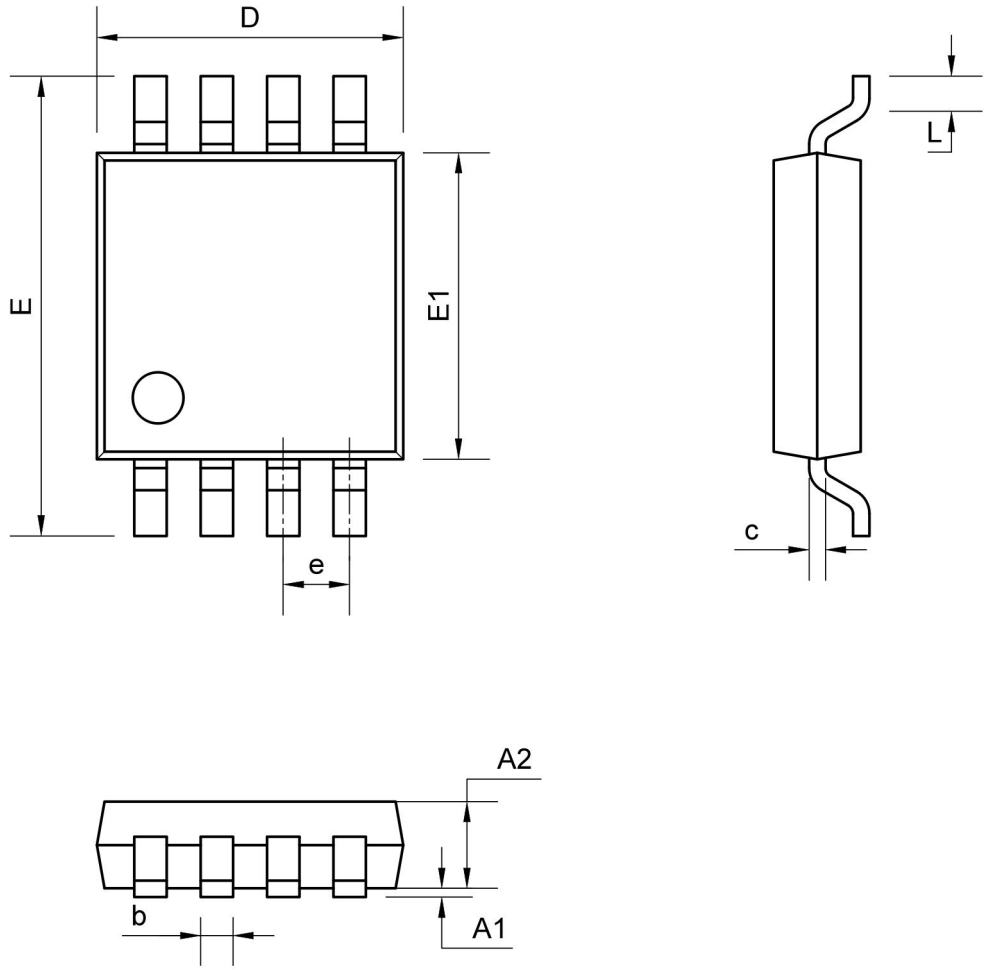
Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.

To reduce parasitic coupling, run the input traces as far away from the supply lines and digital signal as possible.Low-ESR, 0.1 μF ceramic bypass capacitors must be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single supply applications.

Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

Package Dimension

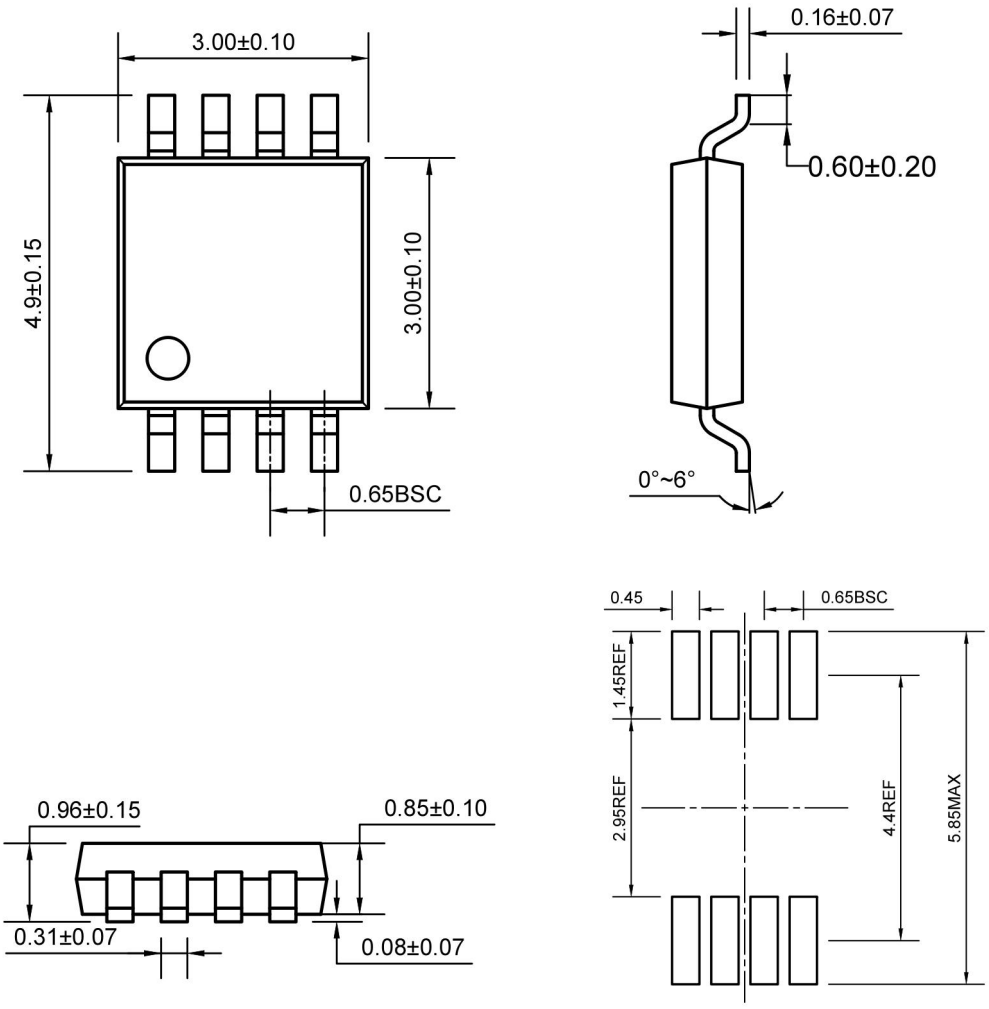
SOP8



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A1	0.15	—	0.22
A2	1.40	1.55	1.50
b		0.40 BSC	
c	0.20	—	0.25
D	4.85	4.90	4.95
E	5.99	6.04	6.09
E1	3.85	3.90	3.95
e		1.27 BSC	
L	0.50	0.60	0.70

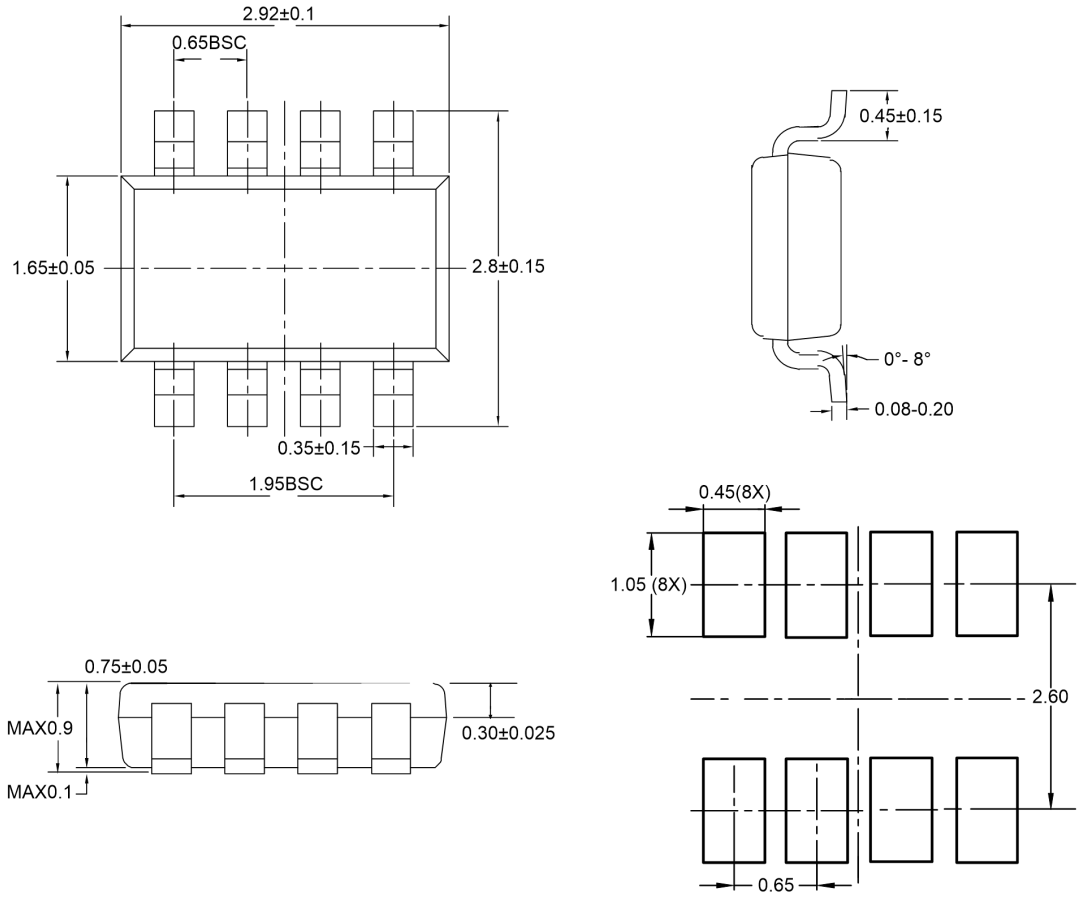
MSOP8



Recommended Land Pattern

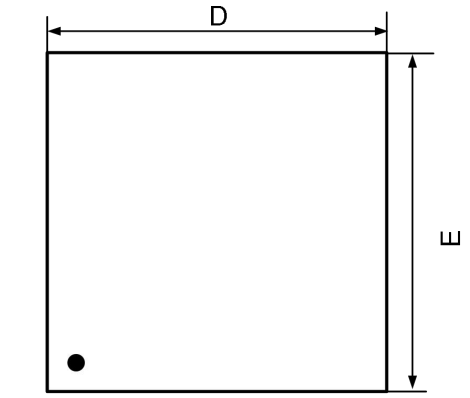
Unit: mm

TSOT23-8

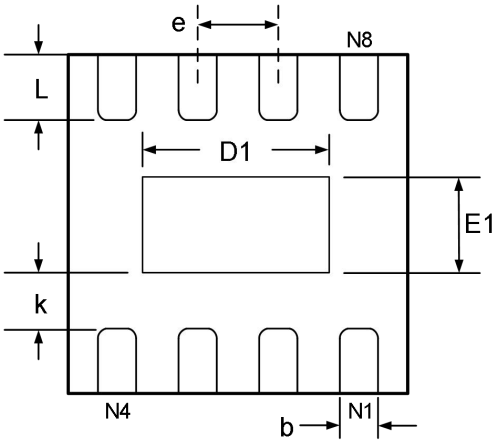


Recommended Land Pattern

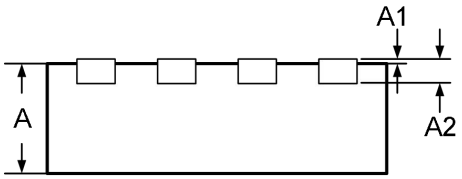
DFN8(2×2)



TOP VIEW



BOTTOM VIEW

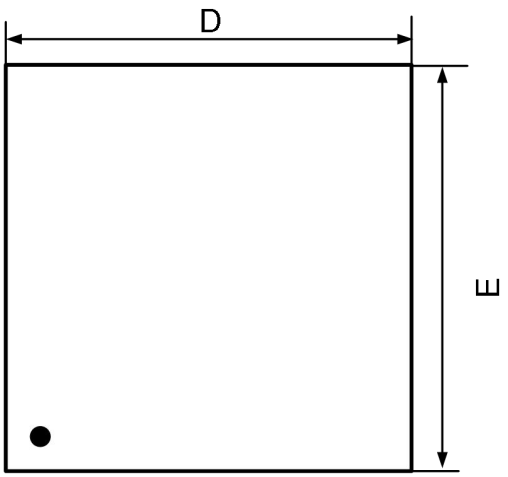


SIDE VIEW

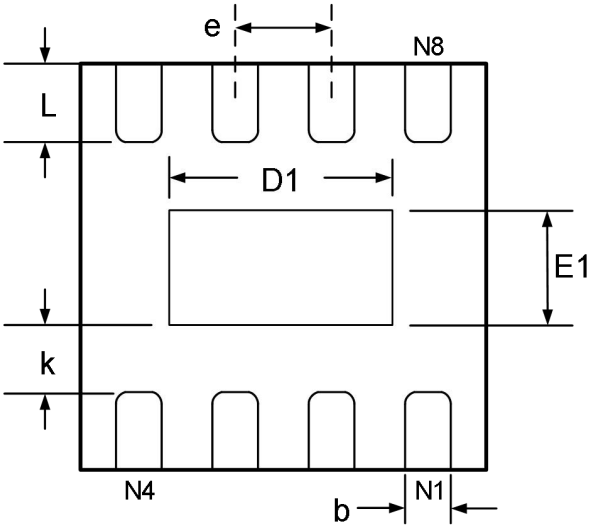
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203 REF	
D	1.90	2.00	2.10
D1	1.10	1.20	1.30
E	1.90	2.00	2.10
E1	0.50	0.60	0.70
k		0.35 REF	
b	0.18	0.23	0.28
e		0.50 BSC	
L	0.275	0.35	0.425

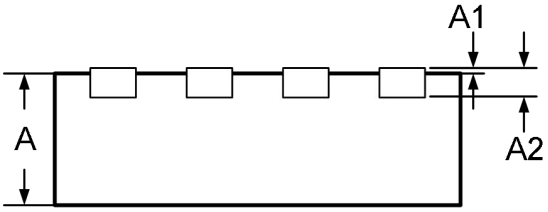
DFN8(3×3)



TOP VIEW



BOTTOM VIEW



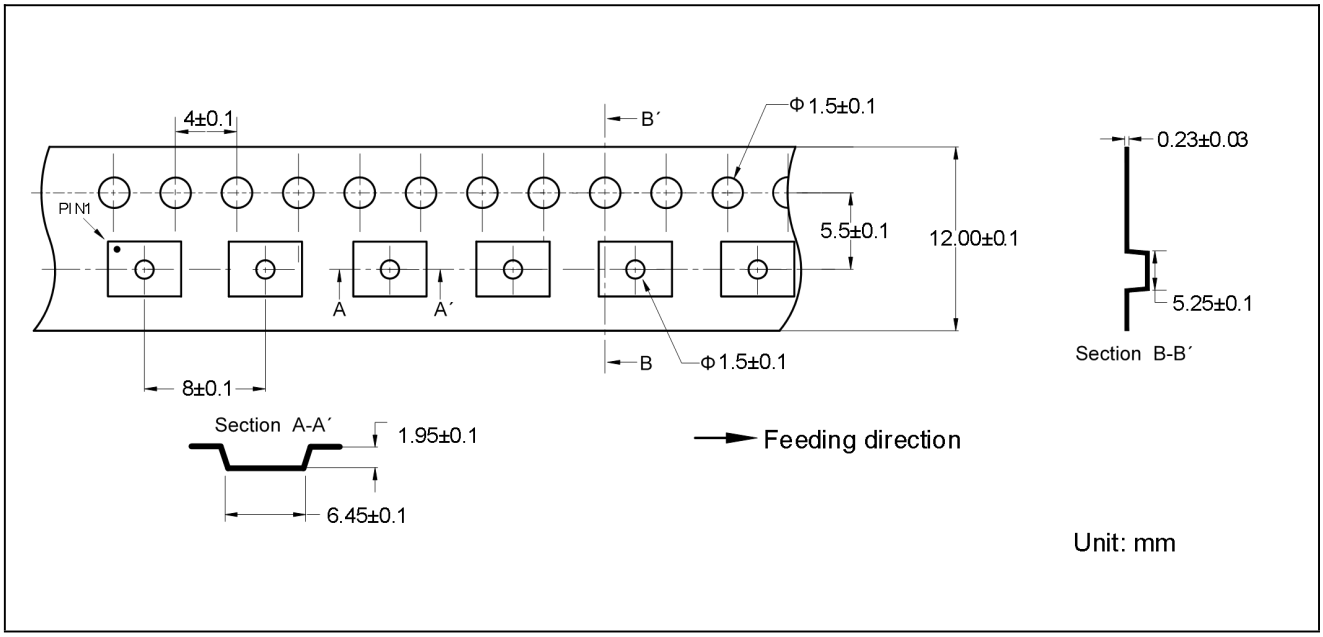
SIDE VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

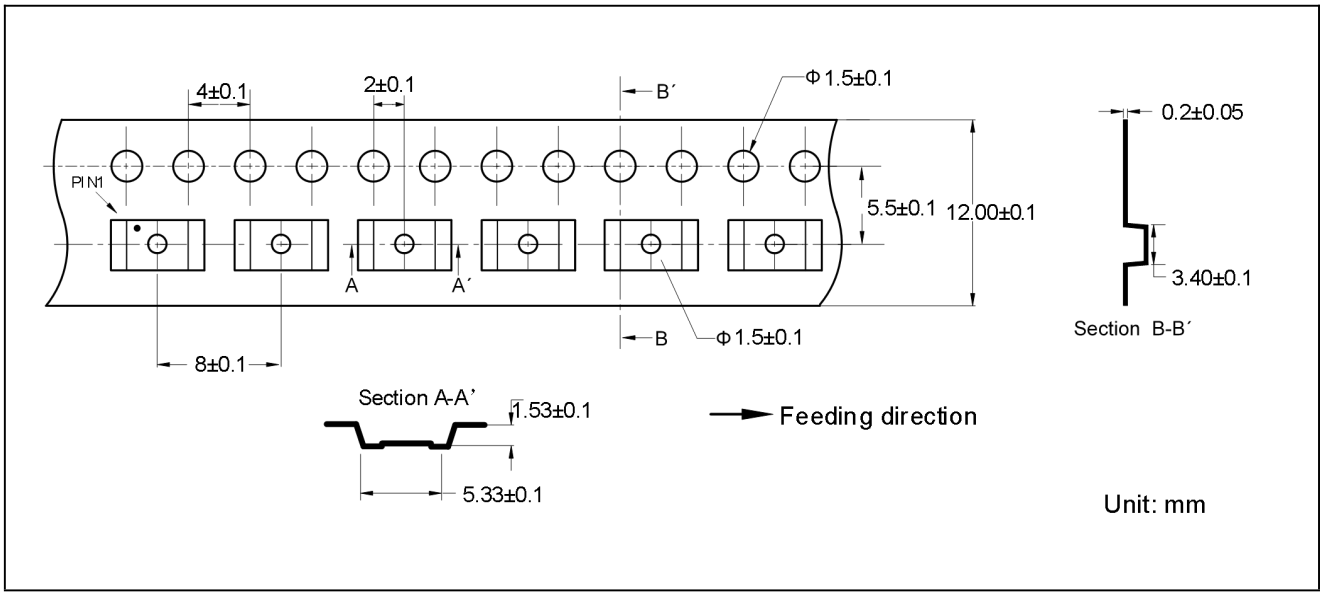
SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203 REF	
D	2.90	3.00	3.10
D1	1.60	1.70	1.80
E	2.90	3.00	3.10
E1	2.30	2.40	2.50
k		0.35 REF	
b	0.15	0.20	0.25
e		0.50 BSC	
L	0.325	0.40	0.475

Tape Information

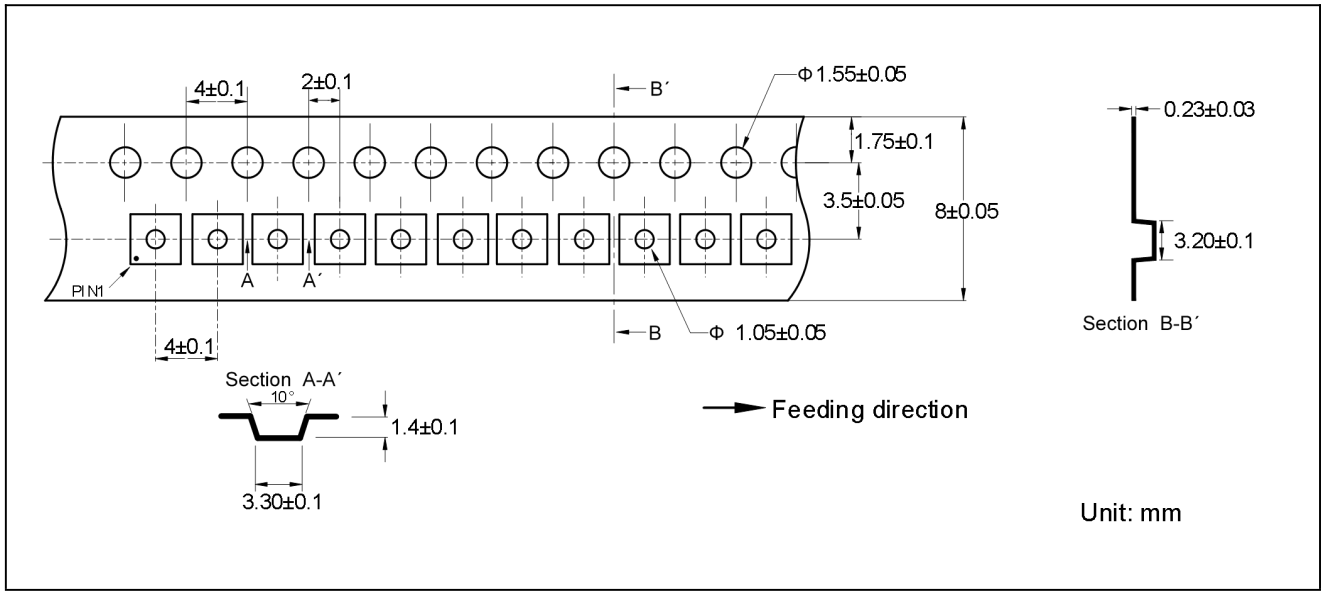
SOP8



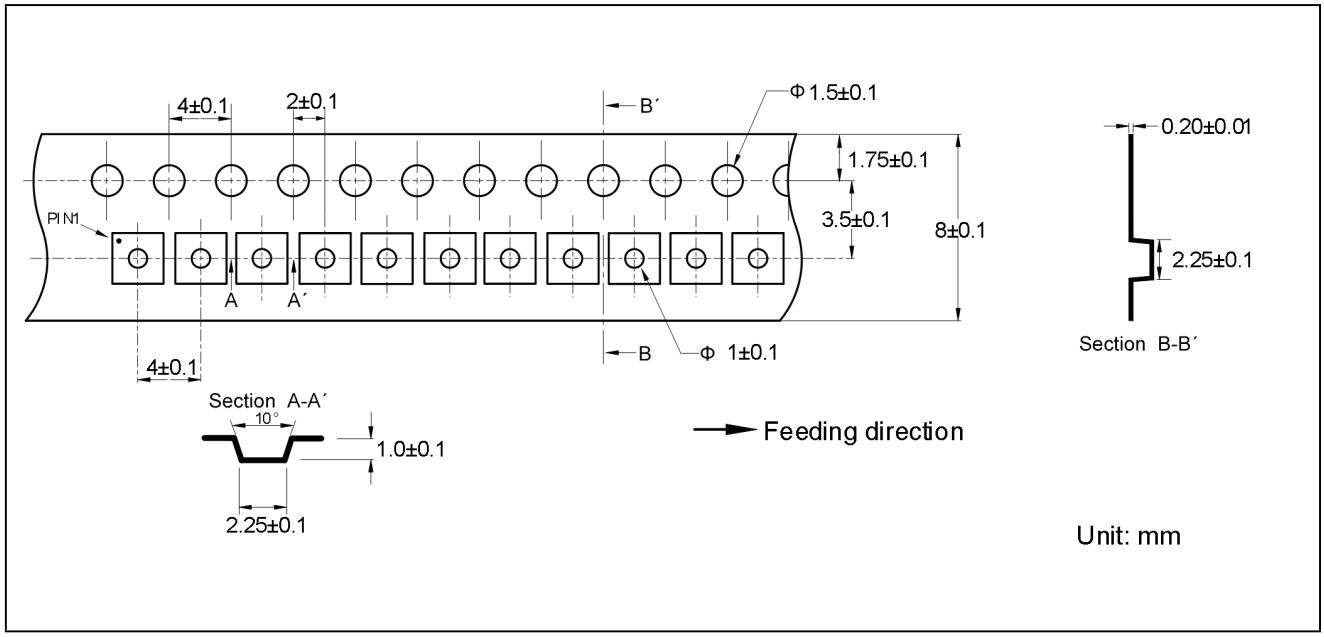
MSOP8



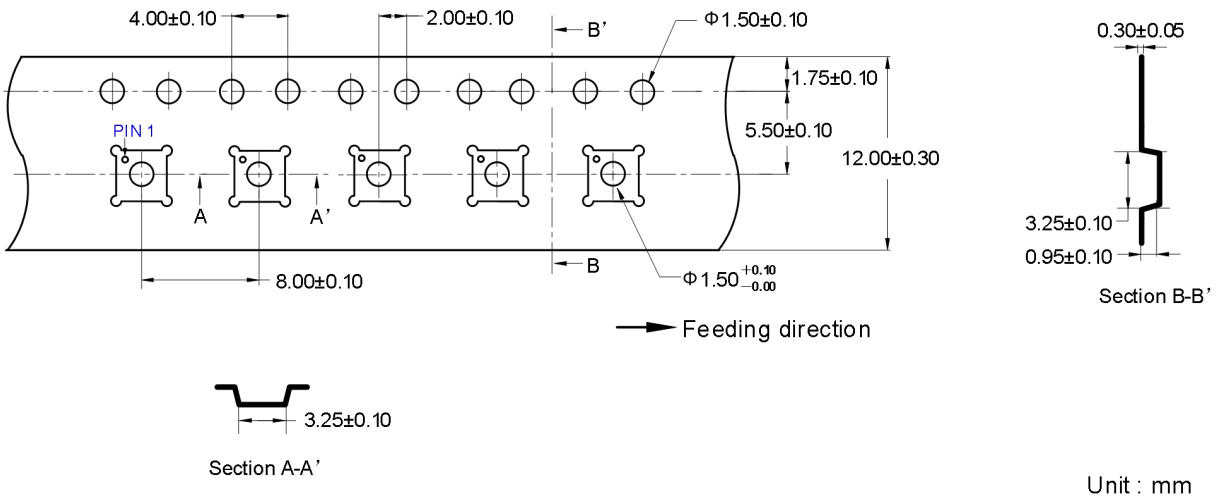
TSOT23-8



DFN8(2×2)



DFN8(3×3)



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2023-04-21	Preliminary Version	Huyt	Wanggp	Liujy
1.0	2023-08-31	Original Version	Huyt	Chenh	Liujy
1.1	2023-9-27	Naming updates	Shibo	Wanggp	Liujy
1.2	2023-10-19	Add TSOT23-8	Shibo	Wanggp	Liujy
1.3	2025-03-28	Update Typical Characteristics	Huyt	Tangyx	Liujy
1.4	2025-04-11	Update MSL Grade	Huyt	Tangyx	Liujy
1.5	2025-12-19	Update Packing Option	Huyt	Chenh	Liujy
1.6	2026-03-20	Add DFN8(2×2),DFN8(3×3)	Huyt	Chenh	Liujy