5.5V Input, 9A, Synchronous Step-Up Converter with Output Disconnect and I2C Control

General Description

The ET8290 is a high-efficiency, synchronous, current-mode, step-up converter with output disconnection. For ET8290, the output voltage can be programmed by I^2C from 3.5V to 5V with 0.1V step.

The ET8290 starts up from an input voltage as low as 1.9V, while providing inrush current limiting and output short-circuit protection. The integrated P-channel synchronous rectifier improves efficiency and eliminates the need for an external Schottky diode. This P-channel disconnects the output from the input during shutdown.

The 1.0MHz switching frequency allows small external components, while the internal compensation and soft-start minimize external component count. The ET8290 provides a compact solution for a 5V output, 3.1A load requirement, using a supply voltage down to 2.8V.

The ET8290 is available in QFN14 package.

Features

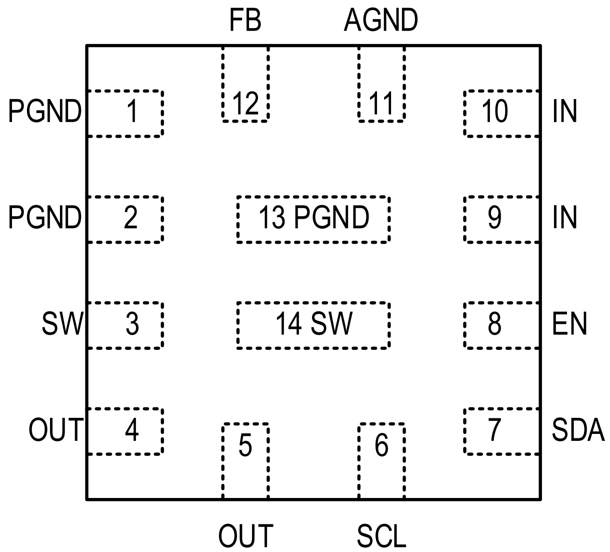
- Up to 98% Efficiency
- 1.9V to 5.5V Input Range
- Output Programmed by I^2C, Ranges from 3.5V to 5V with 0.1V Step
- Internal Synchronous Rectifier
- 1.0MHz Fixed Switching Frequency
- 9A Typical Switch Current Limit
- 43uA Quiescent Current
- High Efficiency over Full Load Range
- Internal Soft-start and Compensation
- True Output Load Disconnect from Input
- OCP, SCP, OVP and OTP Protection
- Part No. and Package

Part No.	Package	MSL
ET8290	QFN14 (2mm×2mm)	1

Application

- Battery-Powered Products
- Power Banks, Juice Packs, Battery Back-up Units
- USB Power Supply
- Consumer Electronic Accessories

Pin Configuration

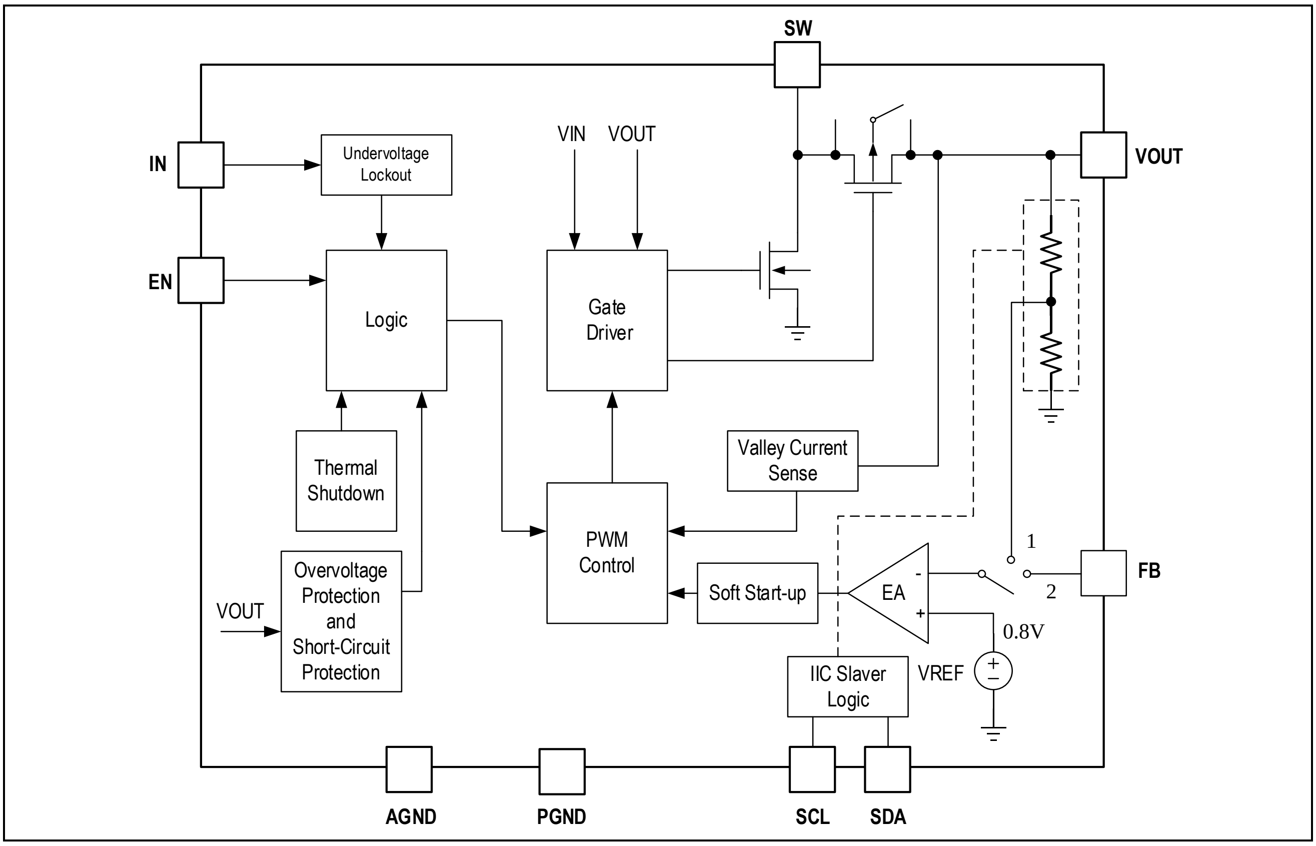


Top View

Pin Function

Pin Name	Pin No.	Description
1, 2,13	PGND	Power Ground.
3, 14	SW	Power Switch Output. SW is the connection node of the internal NMOS switch and synchronous switch. Connect the power inductor between SW and input power. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage spikes.
4, 5	OUT	Output Pin. OUT is the drain of the Internal Synchronous Rectifier MOSFET. Bias is derived from OUT when V_{OUT} is higher than V_{IN}. PCB trace length from OUT to the output filter capacitor(s) should be as short and wide as possible. OUT is completely disconnected from IN when EN is low due to the output disconnect feature.
6	SCL	I^2C Serial Clock.
7	SDA	I^2C Serial Data.
8	EN	Chip Enable Control Input.
9, 10	IN	Power Supply Input. The startup bias is derived from IN. Must be locally bypassed. Once OUT exceeds IN, bias comes from OUT. Thus, once started, operation is completely independent from IN. Pin 9 and 10 must be connected for using.
11	AGND	Analog Signal Ground.
12	FB	Test Pin, it must be left floating.

Block Diagram



Functional Description

Overview

The ET8290 is a 1MHz, synchronous step-up converter with true output disconnecting. The device features fixed-frequency current mode PWM controls for excellent line and load regulation. Internal soft-start and loop compensation simplifies the design process and minimizes external components. The internal low R_{DSON} MOSFETs, combined with frequency stretching operation, enables the device to maintain high efficiency over a wide load current range.

Start-Up

When the IC is enabled and the voltage on the IN pin exceeds V_{UVLO_IN-R}, the ET8290 starts up in the linear charge period. During this linear charge period, the PMOS rectifier turns on until the output capacitor is charged to V_{IN}. The PMOS current is limited to 0.2A when V_{OUT} is below 0.4V to avoid inrush current. While the output ramps up, the PMOS current limit also increases. This circuit also helps to limit the output current under short circuit conditions. Once the output is charged to V_{IN}, the linear charge period elapses and the ET8290 starts switching in normal closed loop operation.

In normal operation, works in boost mode when V_O is higher than V_{IN}+0.1V with 9A typical peak current limit.

Once the output voltage exceeds the input voltage, the ET8290 powers its internal circuits from V_{OUT} instead of V_{IN}.

Soft-Start

The ET8290 provides soft-start by charging an internal capacitor with a current source. This soft start voltage continues to rise, following the FB voltage, during the linear charge period. Once the linear charge period elapses, and the voltage on this capacitor is charged. The soft start capacitor is discharged completely in the event of a commanded shutdown, thermal shutdown or short circuit at the output.

Device Enable

Operation is enabled when the EN pin is switched high and placed into shutdown mode when low. In shutdown mode, the regulator stops switching and all internal control circuitry is off. The load is isolated from the input.

Power-Save Mode

The ET8290 will automatically enter power save mode (PSM) when the load decreases and resume PWM mode when the load increases. When the device goes into PSM, it lowers the switching frequency saving switching and driver losses, and switches to pulse skip mode if the load continues to decrease.

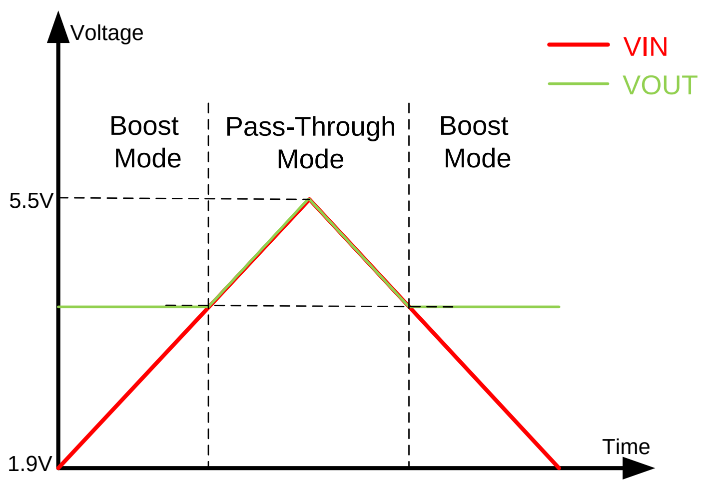
Pass-Through Mode

The ET8290 features Pass-Through Mode when input voltage is higher than output voltage.

In the Pass-Through operation, the boost converter stops switching. The rectifying PMOS constantly turns on and low side switch constantly turns off. The output voltage is the input voltage minus the voltage drop across the dc resistance (DCR) of the inductor and the on-resistance of the rectifying PMOS.

The ET8290 exits Pass-Through Mode and goes back to Boost Mode when input voltage is lower than output voltage.

There is Schematic diagram of Boost Mode and Pass-Through Mode switching:



In the Boost mode(V_{IN}<V_{OUT_SET}), and the boost converter switching, the ET8290 features reverse current blocking capability, which prevents voltages higher than V_{OUT_SET} from leaking back to the VIN pin. However, in Pass-Through mode, VOUT does not have reverse current blocking functionality.

Output Disconnect

The ET8290 is designed to allow true output disconnect by eliminating body diode conduction of the internal PMOS rectifier. This allows V_{OUT} to go to zero volts during shutdown, or isolate and maintain an external bias on V_{OUT}. It also allows for inrush current limit at start-up, minimizing surge current seen by the input supply. To obtain the advantage of output disconnect, there must not be an external Schottky diode connected between the switch pin and V_{OUT}.

Over Load and Short Circuit Protection

When an overload or a short circuit occurs, the output voltage will drop. If V_{OUT} drops below V_{IN}, The lower the output voltage reaches, the smaller the output current is. When the VOUT pin is short to ground, and the output voltage becomes less than 0.4 V, the output current is limited to approximate 200mA. Once the short circuit is released the ET8290 goes through the soft start-up again to the regulated output voltage.

Over Voltage Protection

If V_{OUT} is higher than 5.8V, boost switching stops. This prevents over-voltage from damaging the internal power MOSFET. When the output drops below 5.7V, the device resumes switching automatically.

Thermal Shutdown

The device contains an internal temperature monitor. The switches turn off if the die temperature exceeds 150°C. The device will resume normal operation below 130°C.

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

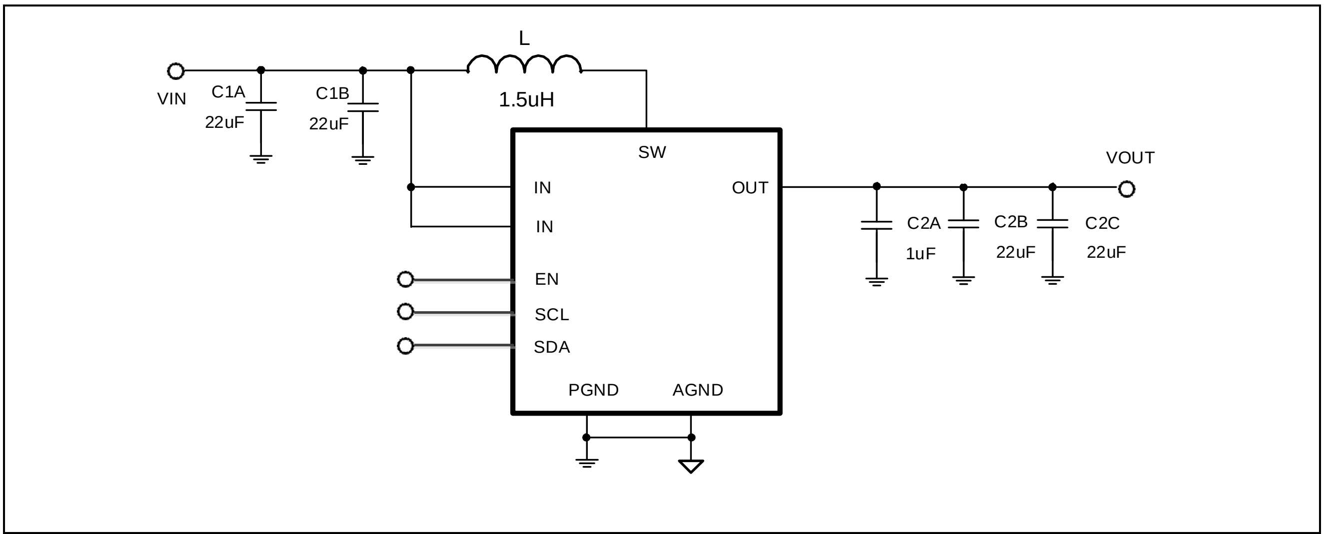
Symbol	Parameters	Min	Max	Unit
V_{OS}	SW	-0.3	6.5	V
	All Other Pins	-0.3	6.5	V
V_{ESD}	Human Body Model (JEDEC JS-001)		±3000	V
	Charged Device Model (JESD22-C101)		±1000	V
T_J	Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature	-65	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameters	MIN	MAX	Unit
V_{IN}	Supply Input Voltage Range	1.9	5.5	V
V_{OUT}	Output Voltage Range	3.5	5.0	
T_J	Operating Junction Temperature	-40	125	°C
T_A	Ambient Temperature	-40	85	°C

Application Circuit



Recommended External Components

Component	Value	Size	Vendor
L	1.5uH	7040	744311150 (Wurth)
C1A、C1B	2*22uF / 16V	1210	CS3225X5R226K160NRL (SAMWHA)
C2A	1uF / 10V	0402	CL05B104KO5NNNC (SAMSUNG)
C2B、C2C	2*22uF / 16V	1210	CS3225X5R226K160NRL (SAMWHA)

Electrical Characteristics

V_{IN} = V_{EN} =3.3V, V_{OUT} = 5V, T_A= -40°C to 85°C, typical values are tested at T_A =25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Voltage Range						
Start Operating Input Voltage	V_{IN}		1.9		5.5	V
Quiescent Current	I_{Q_NS}	V_{EN}=V_{IN}=3.3V, V_{OUT}=5V, no load Measured on OUT pin, T_A=25°C		43	57	µA
		V_{EN}=V_{IN}=3.3V, V_{OUT}=5V, no load Measured on IN pin		0.3		µA
Shutdown Current	I_{SD}	V_{EN}=V_{OUT}=0V, Measured on IN pin, T_A=25°C		0.1	1	µA
IN UVLO Rising Threshold	$V_{UVLO\ INR}$	V_{IN} Rising T_A=25°C	1.6	1.7	1.8	V
IN UVLO Falling Threshold	$V_{UVLO\ INF}$	V_{IN} Falling, V_{OUT}=5V		425		mV
Step-up Converter						
Operation Frequency	F_{SW}	T_A=25°C	0.8	1	1.1	MHz
		-40°C≤T_A≤85°C	0.7	1	1.2	
NMOS On-Resistance	R_{NDSON}			16		mΩ
NMOS Leakage Current	I_{NLK}	V_{SW}=5V		100		nA
PMOS On-Resistance	R_{PDSON}			21		mΩ
PMOS Leakage Current	I_{PLK}	V_{SW}=5V, V_{OUT}=0V		0.1		µA
Maximum Duty Cycle	D_{MAX} (1)		90	95		%
Linear Charge Current Limit	I_{CH_LIMIT}	V_{OUT}≤0.4V		0.2		A
PMOS Valley Current Limit	I_{LIMIT2}	Duty=44%, V_{IN}=2.8V, V_{OUT} =5V		9.0		A
Logic Interface						
High-Level Voltage	V_{ENH}		1.2			V
Low-Level Voltage	V_{ENL}				0.35	V
Input Current	I_{EN}	Connect to V_{IN}		10		nA
Protection						
Thermal Shutdown	T_{SHDN} (1)			150		°C
Over Temperature Hysteresis	T_{HYS} (1)			20		°C

Note1: Not production tested, design assurance.

Typical Characteristics

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5uH, T_A = 25°C, unless otherwise noted.

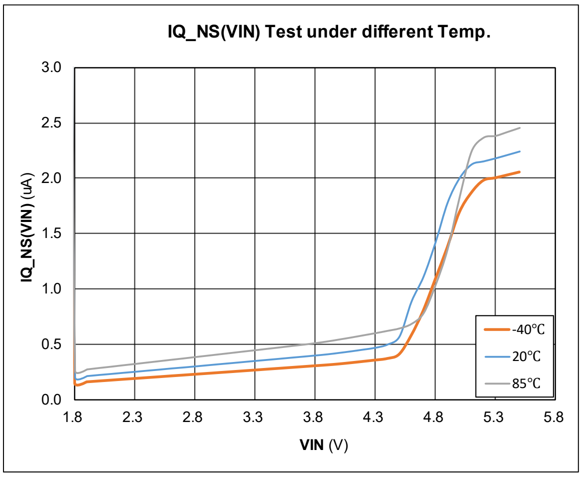


Figure 1. Quiescent Current (VIN) vs. VIN

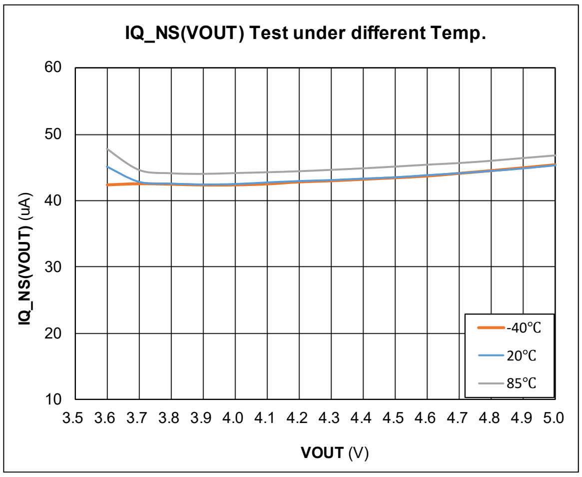


Figure 2. Quiescent Current (VOUT) vs. VOUT

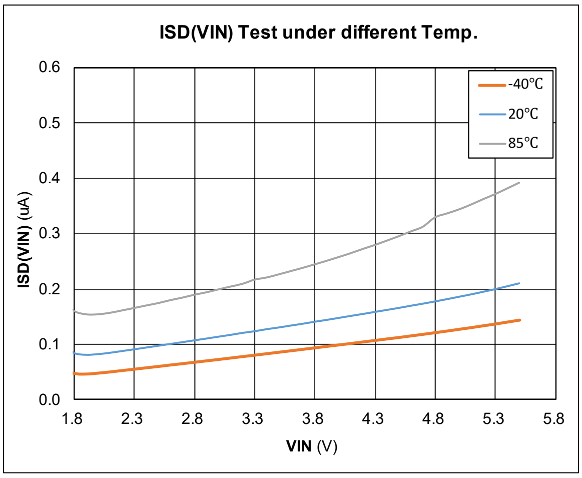


Figure 3. Shutdown Current vs. VIN

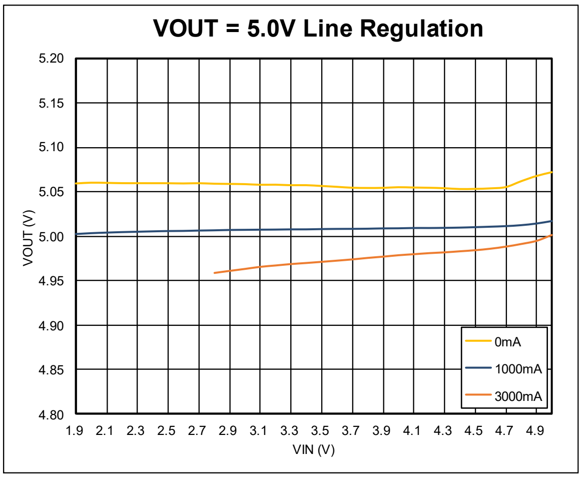


Figure 4. Line Regulation

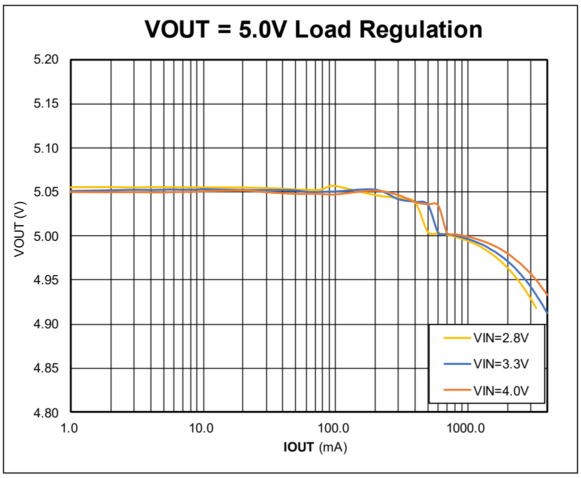


Figure 5. Load Regulation

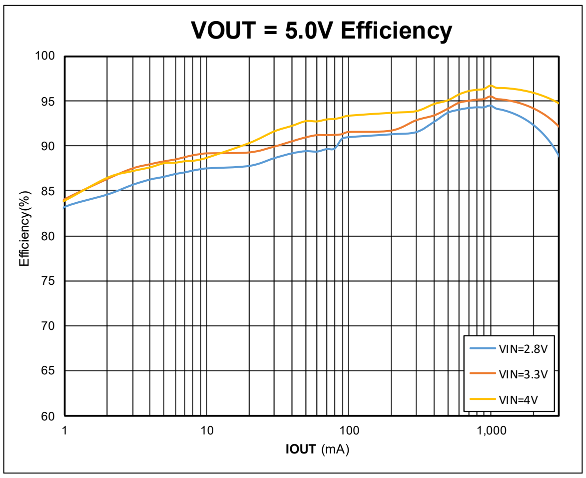


Figure 6. Efficiency vs. Load Current

Typical Characteristics (continued)

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5uH, T_A = 25℃, unless otherwise noted.

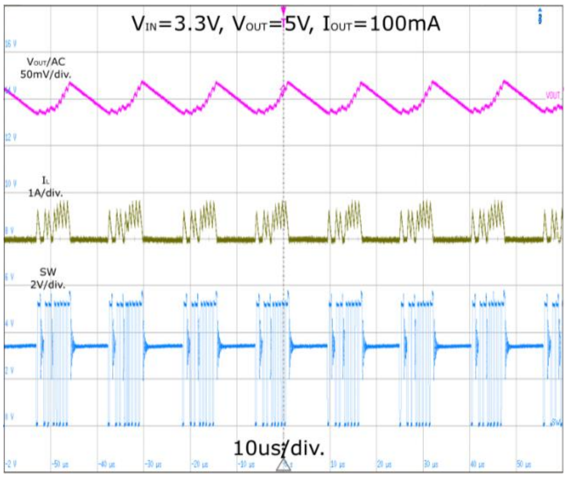


Figure 7. Output Voltage Ripple with Light Load

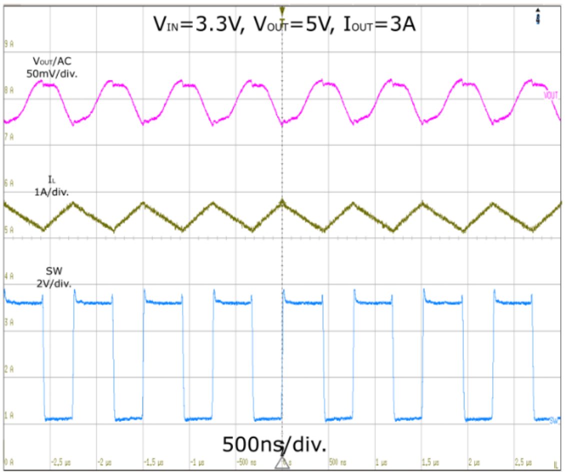


Figure 8. Output Voltage Ripple with Heavy Load

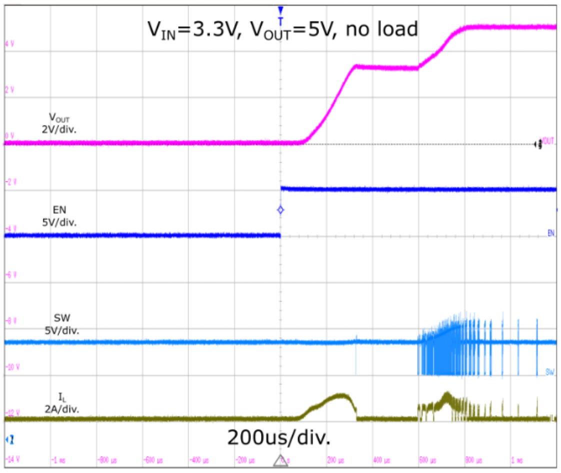


Figure 9. EN Startup with no Load

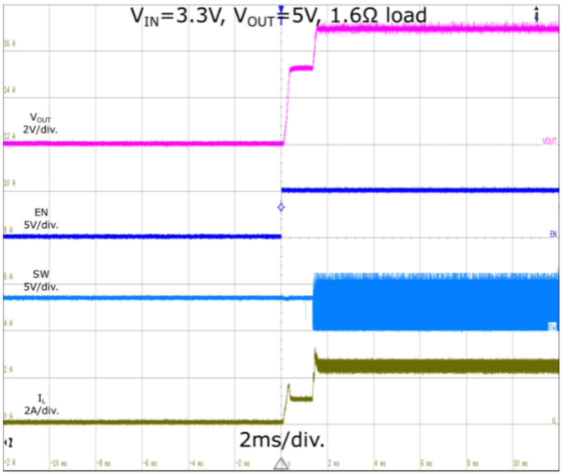


Figure 10. EN Startup with Heavy Load

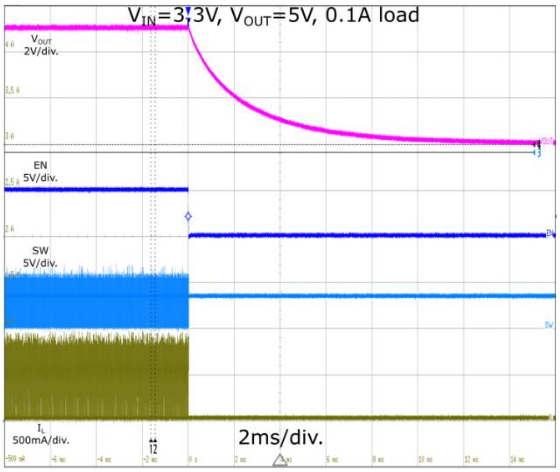


Figure 11. EN Shutdown with no Load

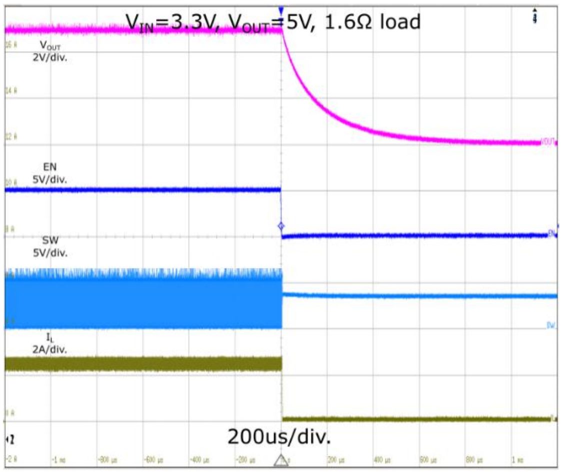


Figure 12. EN Shutdown with Heavy Load

Typical Characteristics (continued)

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5uH, T_A = 25℃, unless otherwise noted.

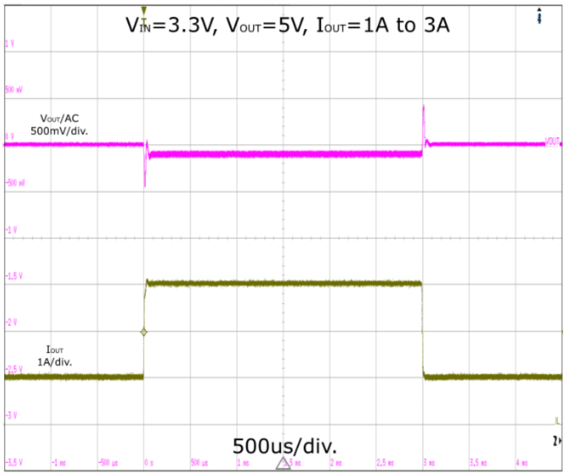


Figure 13. Load Transient

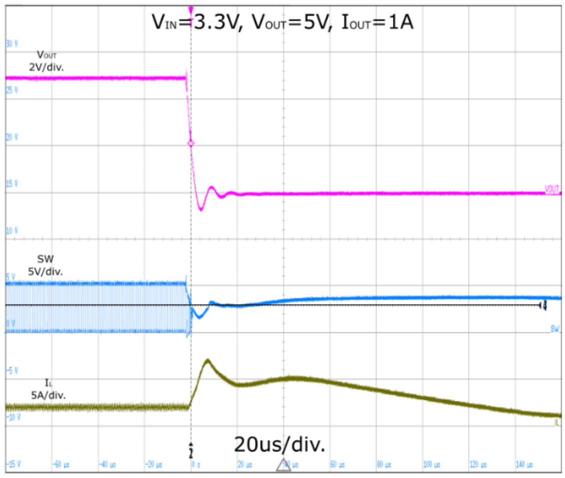


Figure 14. Short Circuit Entry

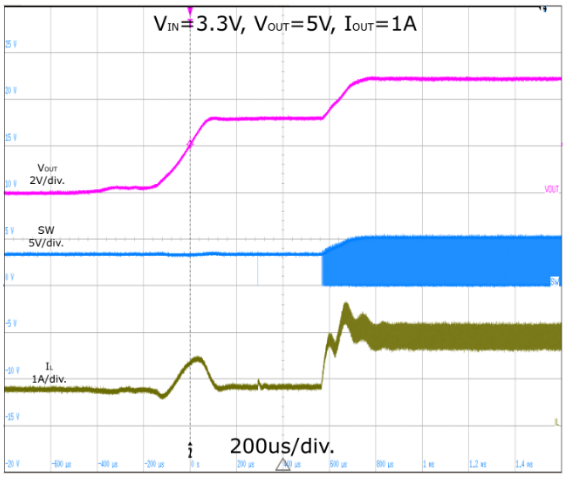


Figure 15. Short Circuit Recovery

Programming

Serial Interface Description

I2C Interface

Baseband Processor can transmit data with ET8290 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is high, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

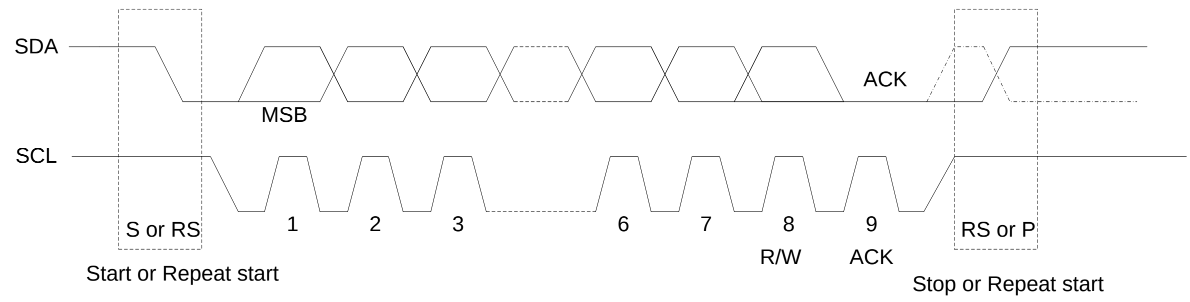
When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET8290 will send a low level response signal with one period width to the SDA port. During the reading mode, ET8290 will not send response signal and the host will send a high response signal one period width to the SDA.



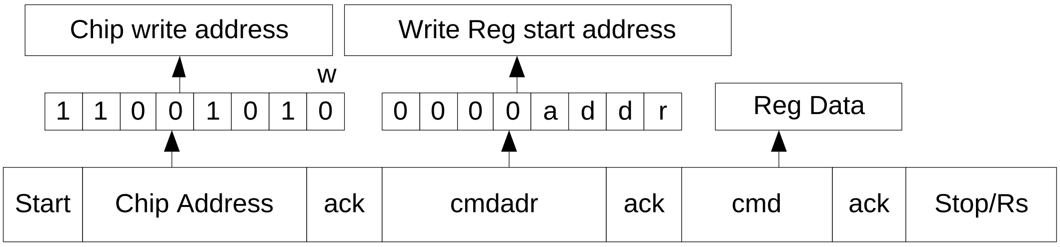
I²C write mode

- ACK=Acknowledge
- MSB=Most Significant Bit
- S=Start Conditions
- RS=Restart Conditions
- P=Stop Conditions
- Restart: SDA-level turnover as expressed by the dashed line waveform

7bit Address for chips

Chip Name	7bit Address
ET8290	1100101b

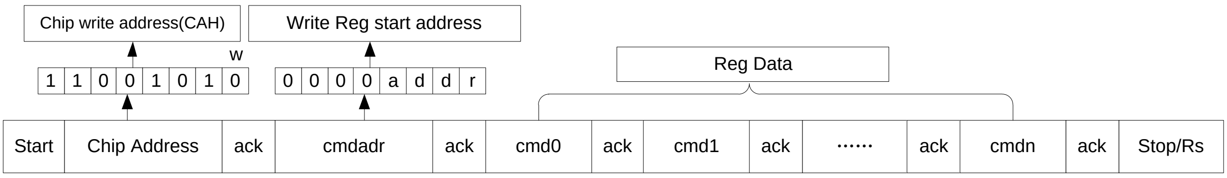
I2C Writing Command Register Interface Protocol (single):



I²C Writing Command Register (single)

- Start=Start Conditions
- Chip address=Write register address =1100101+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(4'd0+REG's 4bit address)
- ack=Acknowledge
- Reg data = cmd(Command data)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

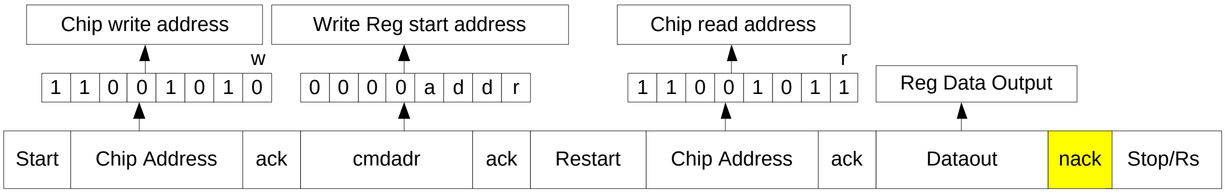
I2C Writing Command Register Interface Protocol (continuous):



I²C Writing Command Register (continuous)

- Start=Start Conditions
- Chip address=Write register address =1100101+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(4'd0+REG's 4bit address)
- ack=Acknowledge
- Reg data 0 = cmd0(Command data0)
- ack=Acknowledge
- ……………
- Reg data n =cmdn(Command datan)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

I2C Reading Command Register Interface Protocol (single):



I²C Reading Command Register (single)

- Start=Start Conditions
- Chip address =Write register address=1100101+0(w)b
- ack=Acknowledge from ET8290
- Write Reg start address byte = cmdadr(4'd0 + REG's 4bit address)
- ack=Acknowledge from ET8290
- Restart=Restart condition
- Chip address Read register address=1100101+1(r)b
- ack=Acknowledge from ET8290
- Dataout=Register data output
- nack=No Acknowledge from Host
- Stop/Rs=Stop Condition/Restart Condition

Register Map

Register Name	Address	R/W	Description	Default
CONTROL	0x00	R/W	Control Register	0x87
STATUS	0x01	R	Status Register	0x80
DEVID	0x02	R	DEVID Register	0x8E
VOUT_SET	0x03	R/W	VOUT Setting Register	0x00

Register Description

CONTROL Register Address: 0x00 (Default: 10000111b)

Bit	Symbol	Description		Read/Write	Default
Bit 7	BST_EN	Device enable bits. 0: Disable the device. 1: Device Enable.		R/W	1
Bit 6	BST_DISCHG	VOUT discharge function enable bit. 0: When the regulator is disabled, VOUT is not discharged. 1: When the regulator is disabled, VOUT discharges through an internal pull-down resistor.		R/W	0
Bit 5	BST_PWM	Device mode of operation bits. 0: PFM with automatic transition into PWM operation. 1: Forced PWM operation.		R/W	0
Bit 4	BST_FB_RES_SEL	Device FB port resistor select bits. 0: Internal resistor in FB port.(Fixed value) 1: External resistor in FB port.		R/W	0
Bit [3:2]	BST_UP_SR	Output Voltage Rising DVS Step Setting Control		R/W	01
		00	100mv/2us		
		01	100mv/4us		
		10	100mv/8us		
		11	100mv/16us		
Bit[1:0]	BST_DN_SR	Output Voltage Falling DVS Step Setting Control		R/W	11
		00	100mv/2us		
		01	100mv/4us		
		10	100mv/8us		
		11	100mv/16us		

STATUS Register Address: 0x01 (Default: 1000 0000b)

Bit	Symbol	Description	Read/Write	Default
Bit 7	PGOOD	Power Good status bit. 0: indicates the output voltage is out of regulation. 1: Indicates the output voltage is within its nominal range.	R	1
Bit 6	VIN_UVLO	VIN UVLO status bit. 0: No VIN UVLO 1: Vin UVLO is triggered	R	0
Bit 5	VOUT_OVP	VOUT OVP status bit. 0: NO VOUT OVP 1: VOUT OVP is triggered	R	0
Bit 4	TSD	Thermal shutdown status bit. 0: Normal operation. 1: Thermal shutdown is triggered	R	0
Bit[3:0]	RESERVED	Reserved	R	0

Device ID Register Address: 0x02 (Default: 1000 1110b)

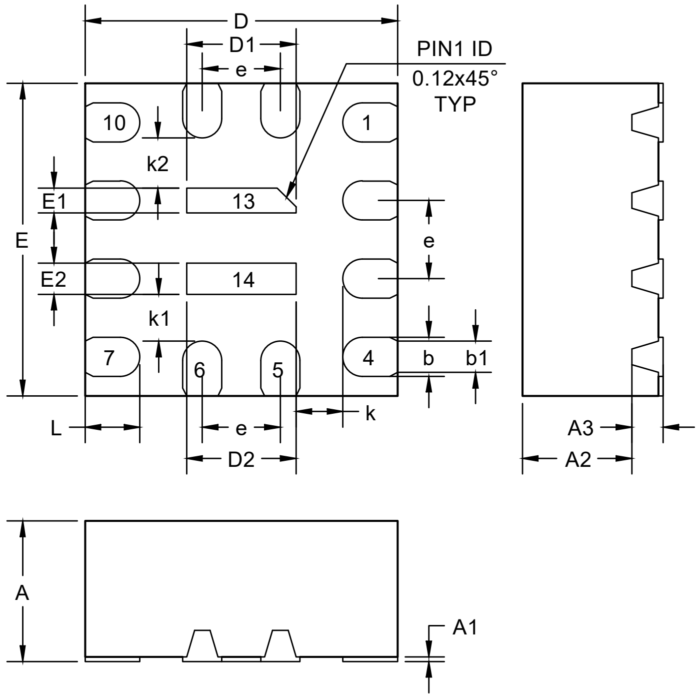
Bit	Symbol	Description	Read/Write	Default
Bit[7:4]	DEV_VER	Device version.	R	1000
Bit[3:0]	Manufacturer	Device identity.	R	1110

VOUT Register Address: 0x03 (Default: 0000 0000b)

Bit	Symbol	Description	Read/Write	Default
Bit [7:4]	RESERVED	Reserved	R	0000
Bit[3:0]	VOUT_SET	These bits set the output voltage Output voltage = 3.5+ (VOUT_SET[3 :0] × 0.1) V (By default, VOUT= 3.5 V, maximum value is 5V)	R/W	0000

Package Dimension

QFN14

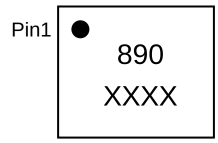


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.2	0.25	0.3
b1	0.18 REF		
D	2 BSC		
E	2 BSC		
D1	0.65	0.7	0.75
E1	0.11	0.16	0.21
D2	0.65	0.7	0.75
E2	0.15	0.2	0.25
e	0.5 BSC		
L	0.3	0.35	0.4
k	0.3 REF		
k1	0.3 REF		
K2	0.32 REF		

Marking



890 - Part Number

XXXX - Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.1	2022-11-5	Preliminary Version	Shi Bo	Xielh	Liujy
1.0	2024-03-8	Official Version	Chenlj	Chenlj	Liujy
1.1	2024-07-05	Update Package Dimension	Liuc	Liuc	Liujy
1.2	2024-10-25	Update Fsw, EC table, Package	Chenlj	wuhs	Liujy
1.3	2024-11-10	Update Block Diagram and Marking	Chenlj	Gexj	Liujy
1.4	2025-12-27	Update Pass-Through Mode Functional Description	Liuc	Gexj	Liujy