

8-Bit Dual Supply Translating Transceiver with Configurable Voltage Translation; 3-State

General Description

The ET74LVCH8T245 is an 8-bit, dual supply transceiver that enables bidirectional level translation. It features two 8-bit input-output ports (An and Bn), a direction control input (DIR), an output enable input (\overline{OE}) and dual supply pins (VCC(A) and VCC(B)). Both VCC(A) and VCC(B) can be supplied at any voltage between 1.2V and 5.5V making the device suitable for translating between any of the low voltage nodes (1.2V, 1.8V, 2.5V, 3.3V, 3.6V, 4.5V, 5V and 5.5V). Pins An, \overline{OE} and DIR are referenced to VCC(A) and pins Bn are referenced to VCC(B). A HIGH on DIR allows transmission from An to Bn and a LOW on DIR allows transmission from Bn to An. The output enable input (\overline{OE}) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either VCC(A) or VCC(B) are at GND level, both An and Bn outputs are in the high-impedance OFF-state. The bus-hold circuitry on the powered-up side always stays active.

The ET74LVCH8T245 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

Features

- Wide Supply Voltage Range:
 - V_{CC(A)}: 1.2V to 5.5V
 - V_{CC(B)}: 1.2V to 5.5V
- Fully Configurable Dual-Rail Design
- Maximum Data Rates:
 - 420Mbit/s (3.3V to 5.0V Translation)
 - 210Mbit/s (Translate to 3.3V)
 - 140Mbit/s (Translate to 2.5V)
 - 75Mbit/s (Translate to 1.8V)
 - 60Mbit/s (Translate to 1.5V)
- Bus Hold on Data Inputs
- I_{OFF} Circuitry Provides Partial Power-down Mode Operation
- Ambient Temperature Range of -40°C to 125°C
- ESD Protection Complies with JEDEC Standard
 - HBM: ±4000V Pass (JEDEC JS-001)
 - CDM: ±1500V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±100mA Per JEDEC JESD78F

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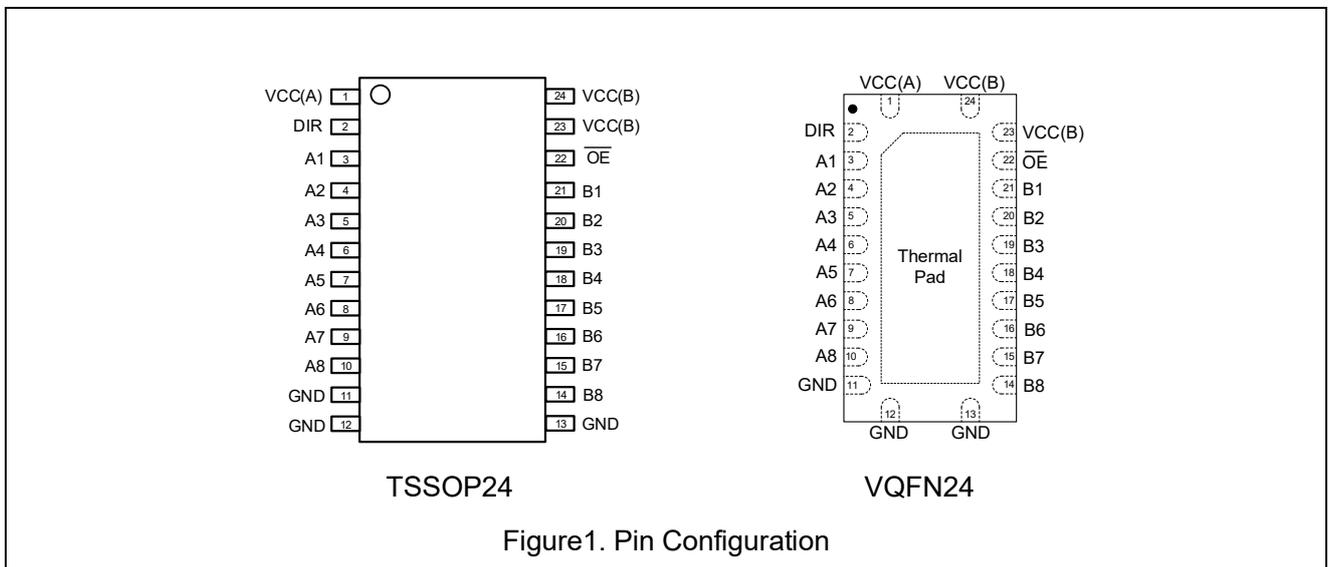
- Part No. and Package Information

Part No.	Package	MSL
ET74LVCH8T245Y	VQFN24 (3.50mm × 5.50mm)	3
ET74LVCH8T245V	TSSOP24 (7.80mm × 4.40mm)	3

Applications

- Personal Electronic
- Industrial Equipment
- Enterprise Infrastructure
- Telecom Equipment

Pin Configuration



Pin Function

Pin Name	Pin		I/O	Description
	TSSOP24	VQFN24		
VCC(A)	1	1	-	Supply Voltage Pin of A Side
VCC(B)	23,24	23,24	-	Supply Voltage Pin of B Side
DIR	2	2	I	Direction-control Signal. Referenced to VCC(A)
\overline{OE}	22	22	I	3-state Output-mode Enables. Pull \overline{OE} high to place all outputs in 3-state Mode. Referenced to VCC(A)
A1~A8	3~10	3~10	I/O	Input/Output A1~A8. Referenced to VCC(A)
B1~B8	14~21	14~21	I/O	Input/Output B1~B8. Referenced to VCC(B)
GND	11,12,13	11,12,13	-	Ground

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Functional Diagram

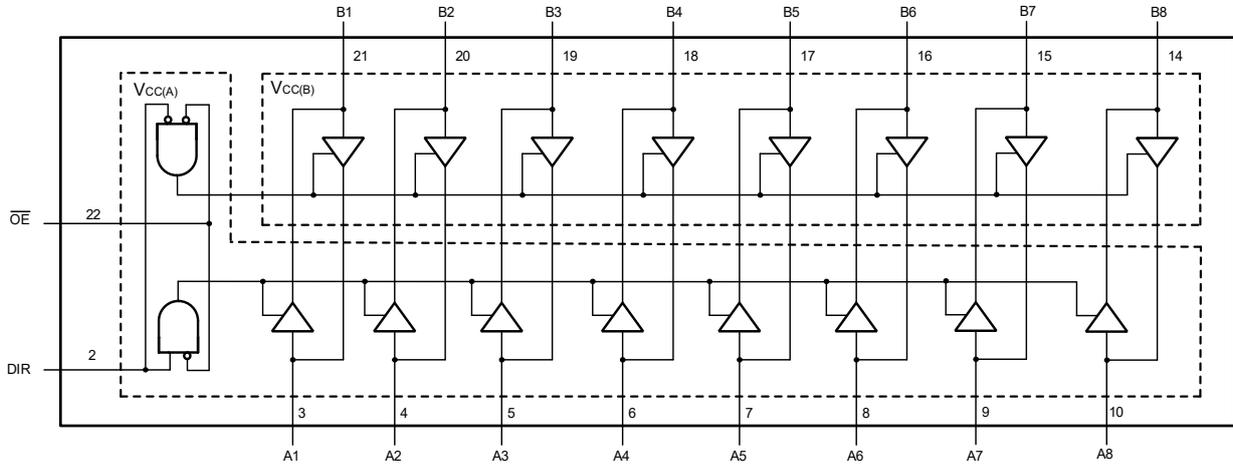


Figure2. Logic Symbol

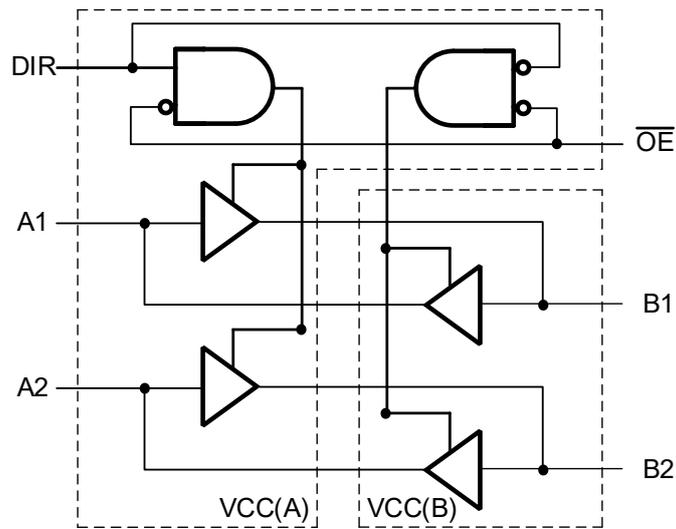


Figure3. Logic Diagram

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Functional Description

Table 1. Function table⁽¹⁾

Supply Voltage	Input		Input/Output	
V _{CC(A)} , V _{CC(B)}	$\overline{\text{OE}}$ ⁽²⁾	DIR ⁽²⁾	An ⁽²⁾	Bn ⁽²⁾
1.2V to 5.5V	L	L	An = Bn	Input
1.2V to 5.5V	L	H	Input	Bn = An
1.2V to 5.5V	H	X	Hi-Z	Hi-Z
GND ⁽³⁾	X	X	Hi-Z	Hi-Z

Note1: H = High Voltage Level; L = Low Voltage Level; X = Don't Care; Z = High-impedance OFF-state.

Note2: The An, DIR and $\overline{\text{OE}}$ input circuit is referenced to V_{CC(A)}; The Bn input circuit is referenced to V_{CC(B)}.

Note3: If at least one of V_{CC(A)} or V_{CC(B)} is at GND level, the device goes into suspend mode.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC(A)}	Supply Voltage A Side (VCC(A) Pin)		-0.5~6.5	V
V _{CC(B)}	Supply Voltage B Side (VCC(B) Pin)		-0.5~6.5	V
I _{IK}	Input Clamping Current	V _I < 0V	-50	mA
V _I	Input Voltage ⁽⁴⁾		-0.5~6.5	V
I _{OK}	Output Clamping Current	V _O < 0V	-50	mA
V _O	Output Voltage	Active Mode ⁽⁵⁾	-0.5~V _{CCO} + 0.5	V
		Suspend or 3-state Mode	-0.5~6.5	V
I _O	Output Current	V _O = 0V to V _{CC}	±50	mA
I _{CC}	Supply Current	Per VCC(A) or VCC(B) Pin	100	mA
I _{GND}	Ground Current	Per GND Pin	-100	mA
T _{STG}	Storage Temperature		-65 to 150	°C
T _{LEAD}	Lead Temperature (Soldering, 10 sec)		260	°C
P _D	Power Dissipation	T _A = 25°C	500	mW
T _J	Operating Junction Range		-40 to 150	°C
V _{ESD}	Human Body Mode ⁽⁶⁾		±4000	V
	Charged Device Mode ⁽⁷⁾		±1500	V
I _{LU}	Latch-up Current ⁽⁸⁾		±100	mA

Note4: I/O absolute maximum rating must be observed.

Note5: V_{CCO} is the supply voltage associated with the output port.

Note6: HBM tested per JEDEC JS-001.

Note7: CDM tested per JEDEC JS-002.

Note8: Latch up Current Maximum Rating tested per JEDEC JESD78F.

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Recommended Operating Conditions

Symbol	Parameter	Conditions	Rating	Unit
$V_{CC(A)}$	Supply Voltage A Side (VCC(A) Pin)		1.2~5.5	V
$V_{CC(B)}$	Supply Voltage B Side (VCC(B) Pin)		1.2~5.5	V
V_I	Input Voltage		0~5.5	V
V_O	Output Voltage	Active Mode	0~ V_{CC0}	V
		Suspend or 3-state	0~5.5	V
T_A	Operating Ambient Temperature		-40 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CCI} = 1.2V$ to 5.5V ⁽⁹⁾	5	ns/V

Note9: V_{CCI} is the supply voltage associated with the input port.

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Electrical Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

V_{CCI} is the supply voltage associated with the data input port; V_{CCO} is the supply voltage associated with the output port.

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$			Unit
			Min	Typ	Max	
V_{OH}	High-Level Output Voltage	$V_I = V_{IH}$ or V_{IL} ; $I_O = -3\text{mA}$; $V_{CC(A)} = V_{CC(B)} = 1.2\text{V}$		1.09		V
V_{OL}	Low-Level Output Voltage	$V_I = V_{IH}$ or V_{IL} ; $I_O = 3\text{mA}$; $V_{CC(A)} = V_{CC(B)} = 1.2\text{V}$		0.07		V
I_I	Input Leakage Current	DIR, \overline{OE} Input; $V_I = 0\text{V}$ or 5.5V ; $V_{CC(A)} = V_{CC(B)} = 1.2\text{V}\sim 5.5\text{V}$			± 1	μA
$I_{BHL}^{(10)}$	Bus hold LOW current	A or B Port; $V_I = 0.42\text{V}$; $V_{CC(A)} = V_{CC(B)} = 1.2\text{V}$		26		μA
$I_{BHH}^{(10)}$	Bus hold HIGH current	A or B Port; $V_I = 0.78\text{V}$; $V_{CC(A)} = V_{CC(B)} = 1.2\text{V}$		-24		μA
$I_{BHLO}^{(10)}$ (11)	Bus hold LOW overdrive current	$V_{CC(A)} = V_{CC(B)} = 1.2\text{V}$		27		μA
$I_{BHHO}^{(10)}$ (11)	Bus hold HIGH overdrive current	$V_{CC(A)} = V_{CC(B)} = 1.2\text{V}$		-26		μA
I_{OZ}	Off-State Output Current	A or B port; $V_O = 0\text{V}$ or V_{CCO} ; $V_{CC(A)} = V_{CC(B)} = 1.2\text{V}\sim 5.5\text{V}$			± 2.5	μA
		Suspend Mode A port; $V_O = 0\text{V}$ or V_{CCO} ; $V_{CC(A)} = 5.5\text{V}$; $V_{CC(B)} = 0\text{V}$			± 2.5	μA
		Suspend Mode B port; $V_O = 0\text{V}$ or V_{CCO} ; $V_{CC(A)} = 0\text{V}$; $V_{CC(B)} = 5.5\text{V}$			± 2.5	μA
I_{OFF}	Power-Off Leakage Current	A port; V_I or $V_O = 0\text{V}\sim 5.5\text{V}$; $V_{CC(A)} = 0\text{V}$; $V_{CC(B)} = 1.2\text{V}\sim 5.5\text{V}$			± 1	μA
		B port; V_I or $V_O = 0\text{V}\sim 5.5\text{V}$; $V_{CC(B)} = 0\text{V}$; $V_{CC(A)} = 1.2\text{V}\sim 5.5\text{V}$			± 1	μA
C_I	Input Capacitance	DIR, \overline{OE} Input; $V_I = 0\text{V}$ or 3.3V ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{V}$		2.2		pF
$C_{I/O}$	Input/Output Capacitance	A and B port; $V_O = 3.3\text{V}$ or 0V ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{V}$		6		pF

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DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	-40°C ≤ T _A ≤ 85°C		-40°C ≤ T _A ≤ 125°C		Unit
			Min	Max	Min	Max	
V _{IH}	High-Level Input Voltage	Data Input					
		V _{CCI} = 1.2V	0.8V _{CCI}		0.8V _{CCI}		V
		V _{CCI} = 1.4V~1.95V	0.65V _{CCI}		0.65V _{CCI}		V
		V _{CCI} = 2.3V~2.70V	1.7		1.7		V
		V _{CCI} = 3.0V~3.60V	2.0		2.0		V
		DIR, $\overline{\text{OE}}$ Input					
		V _{CC(A)} = 1.2V	0.8V _{CC(A)}		0.8V _{CC(A)}		V
		V _{CCI} = 1.4V~1.95V	0.65V _{CC(A)}		0.65V _{CC(A)}		V
		V _{CCI} = 2.3V~2.7V	1.7		1.7		V
		V _{CCI} = 3.0V~3.6V	2.0		2.0		V
		V _{CCI} = 4.5V~5.5V	0.7V _{CC(A)}		0.7V _{CC(A)}		V
V _{IL}	Low-Level Input Voltage	Data Input					
		V _{CCI} = 1.2V		0.2V _{CCI}		0.2V _{CCI}	V
		V _{CCI} = 1.4V~1.95V		0.35V _{CCI}		0.35V _{CCI}	V
		V _{CCI} = 2.3V~2.7V		0.7		0.7	V
		V _{CCI} = 3.0V~3.6V		0.8		0.8	V
		DIR, $\overline{\text{OE}}$ Input					
		V _{CC(A)} = 1.2V		0.2V _{CC(A)}		0.2V _{CC(A)}	V
		V _{CCI} = 1.4V~1.95V		0.35V _{CC(A)}		0.35V _{CC(A)}	V
		V _{CCI} = 2.3V~2.7V		0.7		0.7	V
		V _{CCI} = 3.0V~3.6V		0.8		0.8	V
		V _{CCI} = 4.5V~5.5V		0.3V _{CC(A)}		0.3V _{CC(A)}	V
V _{OH}	High-Level Output Voltage	V _I = V _{IH} or V _{IL}					
		I _O = -100μA; V _{CC(A)} = V _{CC(B)} = 1.2V~4.5V	V _{CCO} - 0.1		V _{CCO} - 0.1		V
		I _O = -6mA; V _{CC(A)} = V _{CC(B)} = 1.4V	1.0		1.0		V
		I _O = -8mA; V _{CC(A)} = V _{CC(B)} = 1.65V	1.2		1.2		V
		I _O = -12mA; V _{CC(A)} = V _{CC(B)} = 2.3V	1.9		1.9		V
		I _O = -24mA; V _{CC(A)} = V _{CC(B)} = 3.0V	2.4		2.4		V
		I _O = -32mA; V _{CC(A)} = V _{CC(B)} = 4.5V	3.8		3.8		V
V _{OL}	Low-Level Output Voltage	V _I = V _{IH} or V _{IL}					
		I _O = 100μA; V _{CC(A)} = V _{CC(B)} = 1.2V~4.5V		0.1		0.1	V
		I _O = 6mA; V _{CC(A)} = V _{CC(B)} = 1.4V		0.3		0.3	V
		I _O = 8mA; V _{CC(A)} = V _{CC(B)} = 1.65V		0.45		0.45	V
		I _O = 12mA; V _{CC(A)} = V _{CC(B)} = 2.3V		0.3		0.3	V
		I _O = 24mA; V _{CC(A)} = V _{CC(B)} = 3.0V		0.55		0.55	V
		I _O = 32mA; V _{CC(A)} = V _{CC(B)} = 4.5V		0.55		0.55	V

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DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	-40°C ≤ T _A ≤ 85°C		-40°C ≤ T _A ≤ 125°C		Unit
			Min	Max	Min	Max	
I _i	Input Leakage Current	DIR, \overline{OE} Input; V _I = V _{CC(A)} or GND; V _{CC(A)} = V _{CC(B)} = 1.2V~5.5V		±2		±10	μA
I _{BHL} ⁽¹⁰⁾	Bus Hold LOW Current	A or B Port					
		V _I = 0.49V; V _{CC(A)} = V _{CC(B)} = 1.4V	15		10		μA
		V _I = 0.58V; V _{CC(A)} = V _{CC(B)} = 1.65V	25		20		μA
		V _I = 0.70V; V _{CC(A)} = V _{CC(B)} = 2.3V	45		45		μA
		V _I = 0.80V; V _{CC(A)} = V _{CC(B)} = 3.0V	100		80		μA
		V _I = 1.35V; V _{CC(A)} = V _{CC(B)} = 4.5V	100		100		μA
I _{BHH} ⁽¹⁰⁾	Bus Hold HIGH Current	A or B Port					
		V _I = 0.91V; V _{CC(A)} = V _{CC(B)} = 1.4V	-15		-10		μA
		V _I = 1.07V; V _{CC(A)} = V _{CC(B)} = 1.65V	-25		-20		μA
		V _I = 1.60V; V _{CC(A)} = V _{CC(B)} = 2.3V	-45		-45		μA
		V _I = 2.00V; V _{CC(A)} = V _{CC(B)} = 3.0V	-100		-80		μA
		V _I = 3.15V; V _{CC(A)} = V _{CC(B)} = 4.5V	-100		-100		μA
I _{BHLO} ⁽¹⁰⁾ ⁽¹¹⁾	Bus Hold LOW Overdrive Current	A or B Port					
		V _{CC(A)} = V _{CC(B)} = 1.6V	125		125		μA
		V _{CC(A)} = V _{CC(B)} = 1.95V	200		200		μA
		V _{CC(A)} = V _{CC(B)} = 2.7V	300		300		μA
		V _{CC(A)} = V _{CC(B)} = 3.6V	500		500		μA
	V _{CC(A)} = V _{CC(B)} = 5.5V	900		900		μA	
I _{BHHO} ⁽¹⁰⁾ ⁽¹¹⁾	Bus Hold HIGH Overdrive Current	A or B Port					
		V _{CC(A)} = V _{CC(B)} = 1.6V	-125		-125		μA
		V _{CC(A)} = V _{CC(B)} = 1.95V	-200		-200		μA
		V _{CC(A)} = V _{CC(B)} = 2.7V	-300		-300		μA
		V _{CC(A)} = V _{CC(B)} = 3.6V	-500		-500		μA
	V _{CC(A)} = V _{CC(B)} = 5.5V	-900		-900		μA	

Note10: '+/-' represents the direction of the current.

Note11: I_{BHL}, I_{BHH} means the bus hold current; I_{BHLO}, I_{BHHO} means the minimum overdrive current to flip the level.

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DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	-40°C ≤ T _A ≤ 85°C		-40°C ≤ T _A ≤ 125°C		Unit
			Min	Max	Min	Max	
I _{oz}	Off-State Output Current	A or B Port; V _O = 0V or V _{CCO} ; V _{CC(A)} = V _{CC(B)} = 1.2V~5.5V		±2		±10	μA
		Suspend Mode A Port; V _O = 0V or V _{CCO} ; V _{CC(A)} = 5.5V; V _{CC(B)} = 0V		±2		±10	μA
		Suspend Mode B Port; V _O = 0V or V _{CCO} ; V _{CC(A)} = 0V; V _{CC(B)} = 5.5V		±2		±10	μA
I _{OFF}	Power-Off Leakage Current	A Port; V _I or V _O = 0V~5.5V; V _{CC(A)} = 0V; V _{CC(B)} = 1.2V~5.5V		±5		±35	μA
		B Port; V _I or V _O = 0V~5.5V; V _{CC(B)} = 0V; V _{CC(A)} = 1.2V~5.5V		±5		±35	μA
I _{CC}	Supply Current	A Port; V _I = 0V or V _{CCI} ; I _o = 0mA					
		V _{CC(A)} = 1.2V~5.5V; V _{CC(B)} = 1.2V~3.6V		10		12	μA
		V _{CC(A)} = 5.5V; V _{CC(B)} = 0V		10		12	μA
		V _{CC(A)} = 0V; V _{CC(B)} = 5.5V	-2		-8		μA
		B Port; V _I = 0V or V _{CCI} ; I _o = 0mA					
		V _{CC(A)} = 1.2V~5.5V; V _{CC(B)} = 1.2~5.5V		10		12	μA
		V _{CC(A)} = 5.5V; V _{CC(B)} = 0V		10		12	μA
		V _{CC(A)} = 0V; V _{CC(B)} = 5.5V	-2		-8		μA
		A Plus B Port (I _{CC(A)} + I _{CC(B)}); I _o = 0mA; V _I = 0V or V _{CCI} ; V _{CC(A)} = 1.2V~5.5V; V _{CC(B)} = 1.2V~5.5V		16		16	μA

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Dynamic Characteristics

Typical switching characteristics at $V_{CC(A)} = 1.2V$ and $T_A = 25^\circ C$ (unless otherwise noted)

Voltages are referenced to GND (ground = 0V); for test circuit see [Figure6](#); for wave forms see [Figure4](#) and [Figure5](#).

t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

Symbol	Parameter	Conditions	$V_{CC(B)}$				Unit
			1.2V	1.8V	3.3V	5.0V	
t_{pd}	Propagation Delay	An to Bn	11.0	7.4	5.7	5.4	ns
		Bn to An	11.0	9.5	8.9	8.9	ns
t_{dis}	Disable Time	\overline{OE} to An	9.5	9.5	9.5	9.5	ns
		\overline{OE} to Bn	10.2	7.8	7.3	6.4	ns
t_{en}	Enable Time	\overline{OE} to An	13.5	13.5	13.5	13.5	ns
		\overline{OE} to Bn	13.6	8.9	7.1	7.0	ns

Typical switching characteristics at $V_{CC(B)} = 1.2V$ and $T_A = 25^\circ C$ (unless otherwise noted)

Voltages are referenced to GND (ground = 0V); for test circuit see [Figure6](#); for wave forms see [Figure4](#) and [Figure5](#). t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

Symbol	Parameter	Conditions	$V_{CC(A)}$				Unit
			1.2V	1.8V	3.3V	5.0V	
t_{pd}	Propagation Delay	An to Bn	11.0	9.5	8.9	8.8	ns
		Bn to An	11.0	7.3	5.7	5.4	ns
t_{dis}	Disable Time	\overline{OE} to An	9.5	5.4	4.1	3.1	ns
		\overline{OE} to Bn	10.2	8.6	7.8	7.8	ns
t_{en}	Enable Time	\overline{OE} to An	13.5	6.9	3.8	3.2	ns
		\overline{OE} to Bn	13.6	12.0	11.4	11.4	ns

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Dynamic Characteristics(Continued)

Voltages are referenced to GND (ground = 0V), $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$				Unit
			1.8V	2.5V	3.3V	5.0V	
$C_{PD}^{(12)}$	Power Dissipation	A Port:(Direction A to B); B Port:(Direction B to A)	1	1	1	2	pF
	Capacitance	A Port:(Direction B to A); B Port:(Direction A to B)	13	13	13	13	pF

Note12: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = Input Frequency in MHz;

f_o = Output Frequency in MHz;

C_L = Output Load capacitance in pF;

V_{CC} = Supply Voltage in V;

N = Number of Inputs Switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of Outputs.

Note13: $f_i = 10\text{MHz}$; $V_I = \text{GND to } V_{CC}$; $t_r = t_f = 1\text{ns}$; $C_L = 0\text{pF}$; $R_L = \infty\Omega$.

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Dynamic Characteristics(Continued)

Voltages are referenced to GND (ground = 0V), $T_A = -40^{\circ}\text{C}\sim 85^{\circ}\text{C}$.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			$1.8\text{V} \pm 0.15\text{V}$		$3.3\text{V} \pm 0.3\text{V}$		$5\text{V} \pm 0.5\text{V}$		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 1.65\text{V to }1.95\text{V}$									
t_{pd}	Propagation Delay	An to Bn	0.5	17.7	0.5	7.2	1.4	7.0	ns
		Bn to An	0.5	17.7	0.5	15.5	1.8	15.1	ns
t_{dis}	Disable Time	$\overline{\text{OE}}$ to An	1.5	11.8	1.5	12.2	1.4	13.2	ns
		$\overline{\text{OE}}$ to Bn	2.4	18.5	1.7	17.1	1.3	9.6	ns
t_{en}	Enable Time	$\overline{\text{OE}}$ to An	0.4	10.8	0.4	10.8	0.4	11.7	ns
		$\overline{\text{OE}}$ to Bn	1.8	11.4	1.2	9.2	0.9	8.8	ns
$V_{CC(A)} = 3\text{V to }3.6\text{V}$									
t_{pd}	Propagation Delay	An to Bn	0.5	15.5	0.5	6.6	0.7	6.0	ns
		Bn to An	0.5	7.2	0.5	6.7	0.6	6.1	ns
t_{dis}	Disable Time	$\overline{\text{OE}}$ to An	1.6	9.2	1.6	9.2	1.6	13.2	ns
		$\overline{\text{OE}}$ to Bn	2.1	18.8	1.5	14.2	0.8	8.9	ns
t_{en}	Enable Time	$\overline{\text{OE}}$ to An	0.8	6.8	0.8	7.3	0.8	8.3	ns
		$\overline{\text{OE}}$ to Bn	1.8	10.2	1.1	7.6	0.9	7.5	ns
$V_{CC(A)} = 4.5\text{V to }5.5\text{V}$									
t_{pd}	Propagation Delay	An to Bn	1.8	15.1	0.7	5.1	0.5	4.8	ns
		Bn to An	1.4	7.0	0.7	5.0	0.5	4.8	ns
t_{dis}	Disable Time	$\overline{\text{OE}}$ to An	0.3	6.5	0.3	6.5	0.3	6.5	ns
		$\overline{\text{OE}}$ to Bn	2.0	16.8	1.4	10.7	0.7	9.6	ns
t_{en}	Enable Time	$\overline{\text{OE}}$ to An	0.7	6.8	0.7	6.8	0.7	6.8	ns
		$\overline{\text{OE}}$ to Bn	1.5	10.7	1.0	7.8	0.9	7.1	ns

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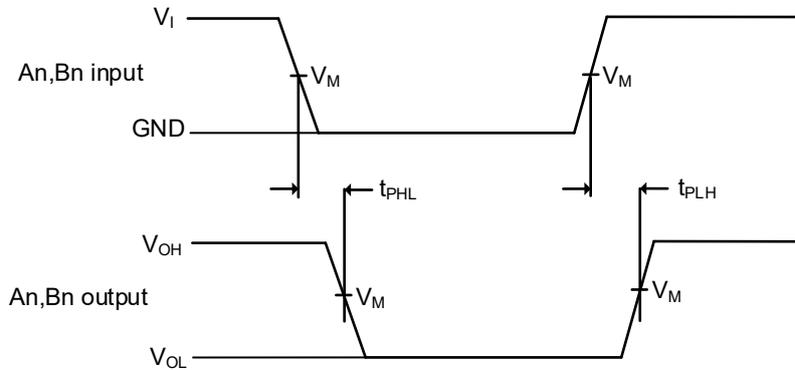
Dynamic Characteristics(Continued)

Voltages are referenced to GND (ground = 0V), $T_A = -40^{\circ}\text{C}\sim 125^{\circ}\text{C}$.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			$1.8\text{V} \pm 0.15\text{V}$		$3.3\text{V} \pm 0.3\text{V}$		$5\text{V} \pm 0.5\text{V}$		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 1.65\text{V to }1.95\text{V}$									
t_{pd}	Propagation Delay	An to Bn	0.5	19.5	0.5	8.0	1.2	7.7	ns
		Bn to An	0.5	19.5	0.5	17.1	1.6	16.7	ns
t_{dis}	Disable Time	$\overline{\text{OE}}$ to An	1.5	12.3	1.5	12.7	1.4	17.5	ns
		$\overline{\text{OE}}$ to Bn	2.4	19.0	1.7	17.6	1.3	10.1	ns
t_{en}	Enable Time	$\overline{\text{OE}}$ to An	0.4	11.3	0.4	11.3	0.4	12.5	ns
		$\overline{\text{OE}}$ to Bn	1.8	11.9	1.2	9.6	0.9	9.3	ns
$V_{CC(A)} = 3.0\text{V to }3.6\text{V}$									
t_{pd}	Propagation Delay	An to Bn	0.5	17.1	0.5	7.2	0.6	6.5	ns
		Bn to An	0.5	8.0	0.5	7.4	0.5	6.6	ns
t_{dis}	Disable Time	$\overline{\text{OE}}$ to An	1.6	9.7	1.6	9.7	1.6	14.7	ns
		$\overline{\text{OE}}$ to Bn	2.1	19.3	1.5	14.7	0.8	9.8	ns
t_{en}	Enable Time	$\overline{\text{OE}}$ to An	0.8	7.3	0.8	7.8	0.8	8.8	ns
		$\overline{\text{OE}}$ to Bn	1.8	10.7	1.1	8.1	0.9	8.5	ns
$V_{CC(A)} = 4.5\text{V to }5.5\text{V}$									
t_{pd}	Propagation Delay	An to Bn	1.6	16.7	0.6	6.2	0.4	6.0	ns
		Bn to An	1.2	7.7	0.6	6.1	0.4	6.0	ns
t_{dis}	Disable Time	$\overline{\text{OE}}$ to An	0.3	10.1	0.3	10.5	0.3	10.5	ns
		$\overline{\text{OE}}$ to Bn	2.0	17.5	1.4	12.3	0.7	11.3	ns
t_{en}	Enable Time	$\overline{\text{OE}}$ to An	0.7	8.3	0.7	8.3	0.7	8.3	ns
		$\overline{\text{OE}}$ to Bn	1.5	12.3	1.0	8.9	0.9	8.4	ns

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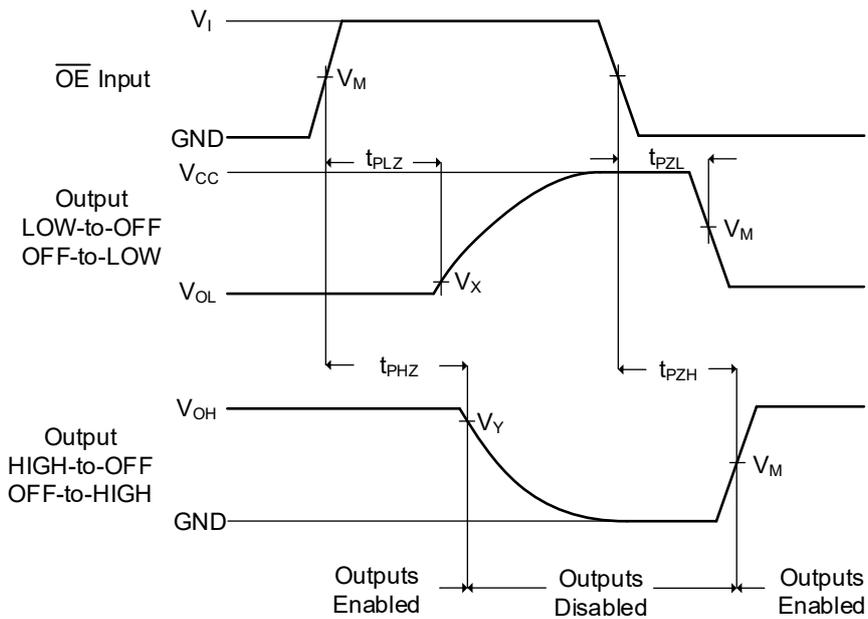
Test Circuit



Measurement points are given in [Table 2](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure4 The Data Input (nAn, nBn) to Output (nBn, nAn) Propagation Delay Times



Measurement points are given in [Table 2](#).

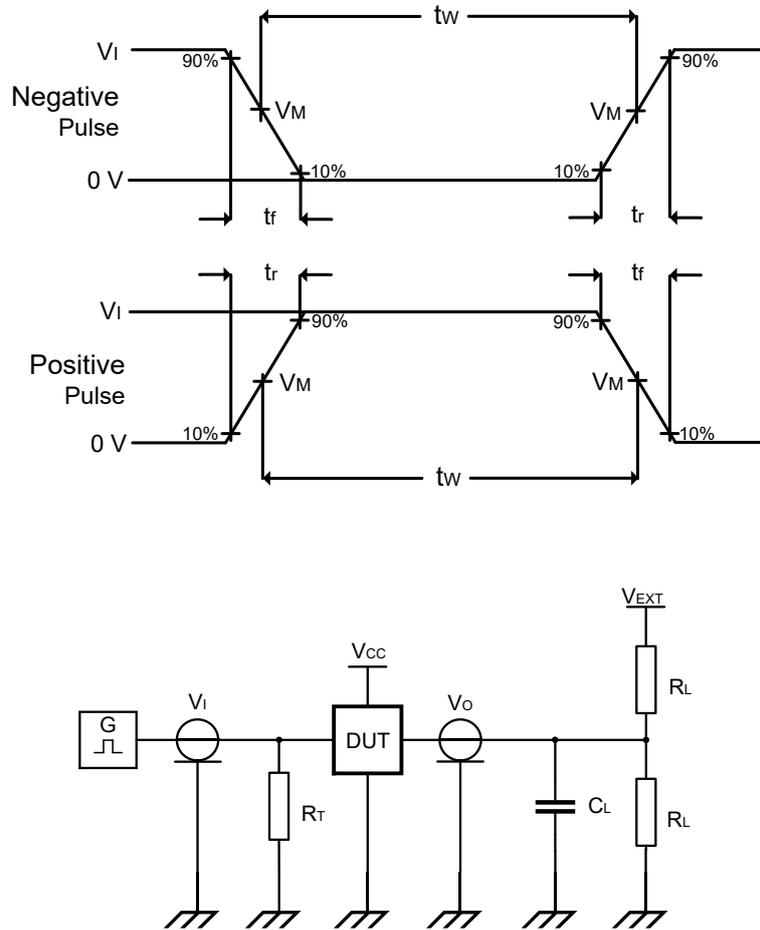
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure5. Enable and Disable Times

Table 2. Measurement Points

Supply Voltage	Input	Output		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
1.2V to 1.6V	$0.5 \times V_{CCI}$	$0.5 \times V_{CCO}$	$V_{OL} + 0.1V$	$V_{OH} - 0.1V$
1.65V to 2.7V	$0.5 \times V_{CCI}$	$0.5 \times V_{CCO}$	$V_{OL} + 0.15V$	$V_{OH} - 0.15V$
3.0V to 5.5V	$0.5 \times V_{CCI}$	$0.5 \times V_{CCO}$	$V_{OL} + 0.3V$	$V_{OH} - 0.3V$

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Measurement points are given in [Table 3](#).

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Figure6. Test Circuit for Measuring Switching Times

Table 3. Test Data

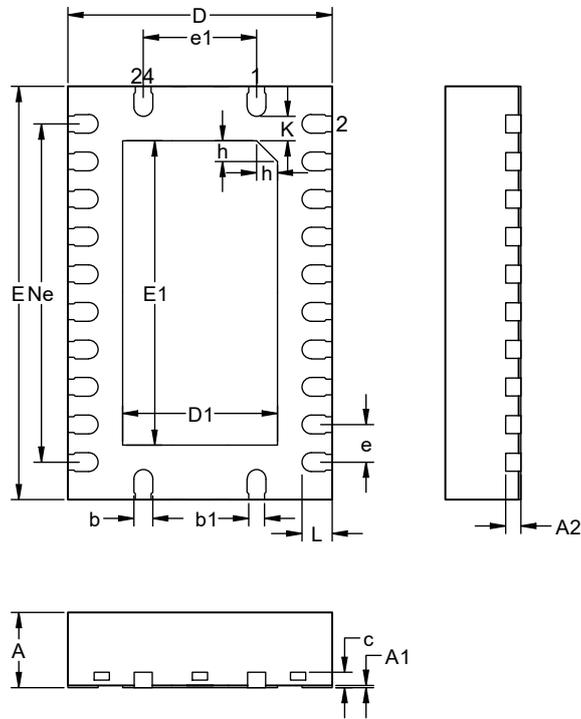
Supply Voltage	Input		Load		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	V_i	$\Delta t/\Delta V^{(14)}$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.2V to 5.5V	V_{CCI}	$\leq 1.0\text{ns/V}$	15pF	2k Ω	Open	GND	$2 \times V_{CCO}$

Note14: $dV/dt \geq 1.0 \text{ V/ns}$

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Package Dimension

VQFN24 (3.50mm × 5.50mm)



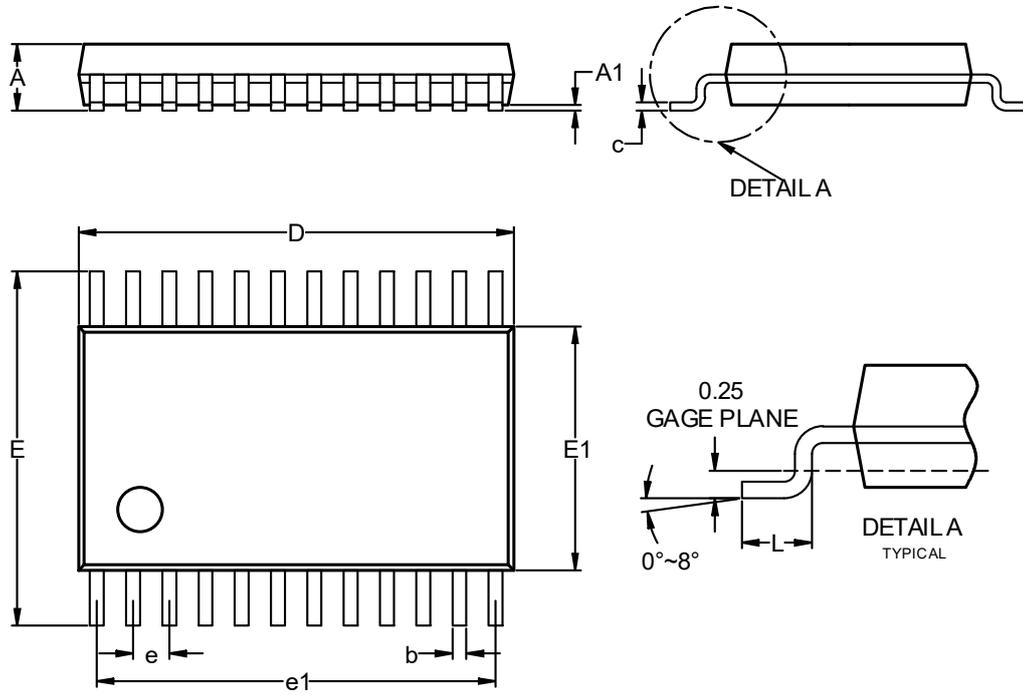
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
b1	0.180REF		
c	0.203REF		
D	3.40	3.50	3.60
D1	2.00	2.10	2.20
e	0.500BSC		
e1	1.500BSC		
Ne	4.500BSC		
E	5.40	5.50	5.60
E1	4.00	4.10	4.20
L	0.35	0.40	0.45
h	0.30	0.35	0.40
k	0.300REF		

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TSSOP24 (7.80mm × 4.40mm)



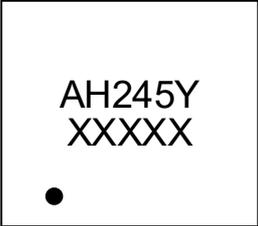
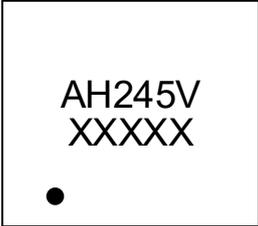
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
b	0.19	0.24	0.30
c	0.15TYP		
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
e1	7.15BSC		
L	0.50	-	0.75

ET74LVCH8T245

Marking Information

	
ET74LVCH8T245Y AH245Y = Part Number XXXXX = Tracking Number	ET74LVCH8T245V AH245V = Part Number XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-11-29	Official Version	Wang anran	Yang xiaoxu	Liu jiaying