32×4 LCD Controller and Driver

General Description

The ET6621 is a 128 patterns (32×4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the ET6621 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the interface between the MCU and the ET6621. The ET6621 contains a power down command to reduce power consumption.

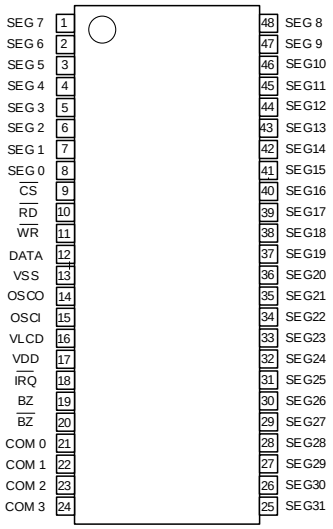
Features

- Operating voltage: 2.4V~5.2V
- Built-in 256kHz RC oscillator
- External 32.768kHz crystal or 256kHz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two select-able buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Built-in time base generator and WDT
- Time base or WDT overflow output
- 32×4 LCD driver, built-in 32×4 bit display RAM
- 3 or 4 wire serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage

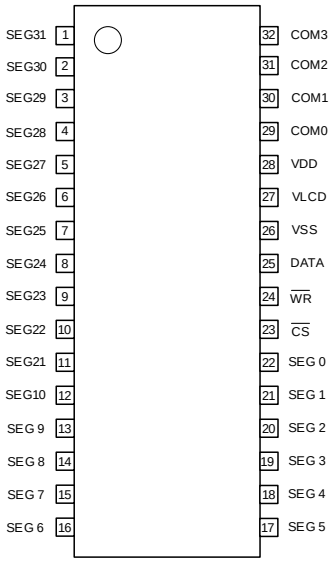
Part No. and package

Part No.	Package
ET6621S	SSOP48
ET6621S2	SSOP24
ET6621EM	SOP28
ET6621M	SOP32
ET6621Q	LQFP44
ET6621QH	LQFP44
ET6621QN	LQFP48
ET6621T	SOP24
ET6621TS	TSSOP20

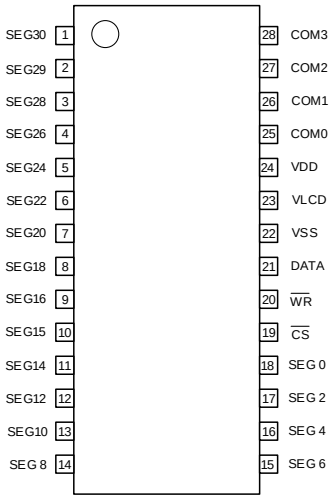
Pin Configuration



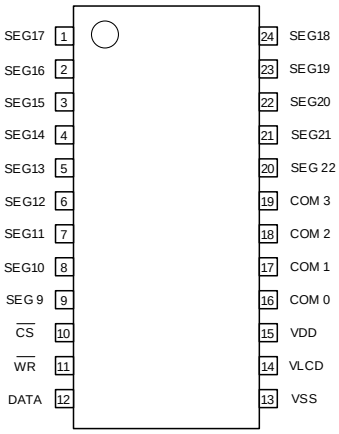
ET6621S(SSOP48)



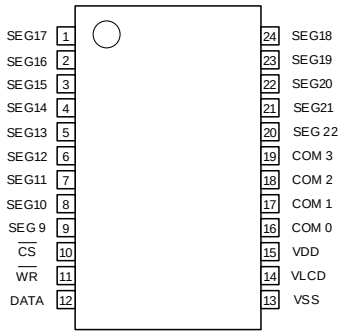
ET6621M(SOP32)



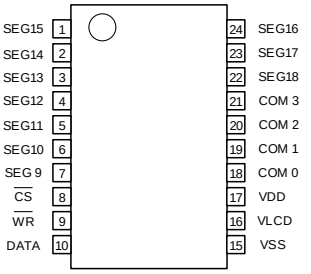
ET6621EM(SOP28)



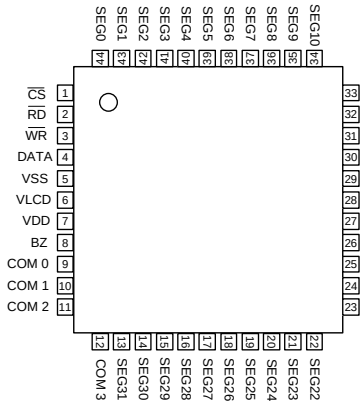
ET6621T(SOP24)



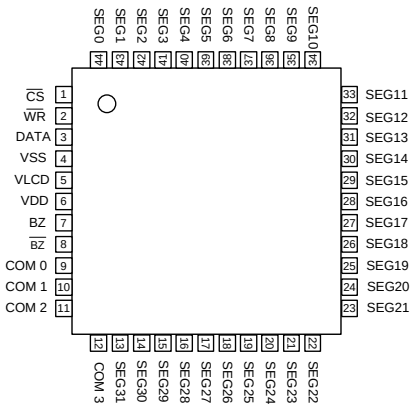
ET6621S2(SSOP24)



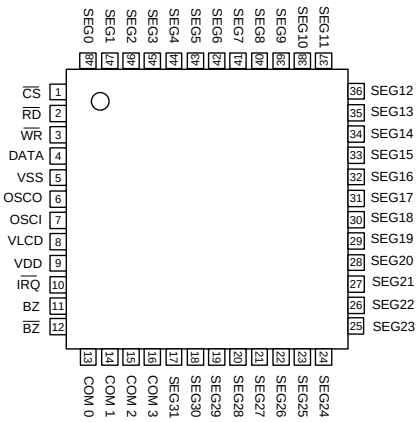
ET6621TS(TSSOP20)



ET6621QH(LQFP44)



ET6621Q(LQFP44)

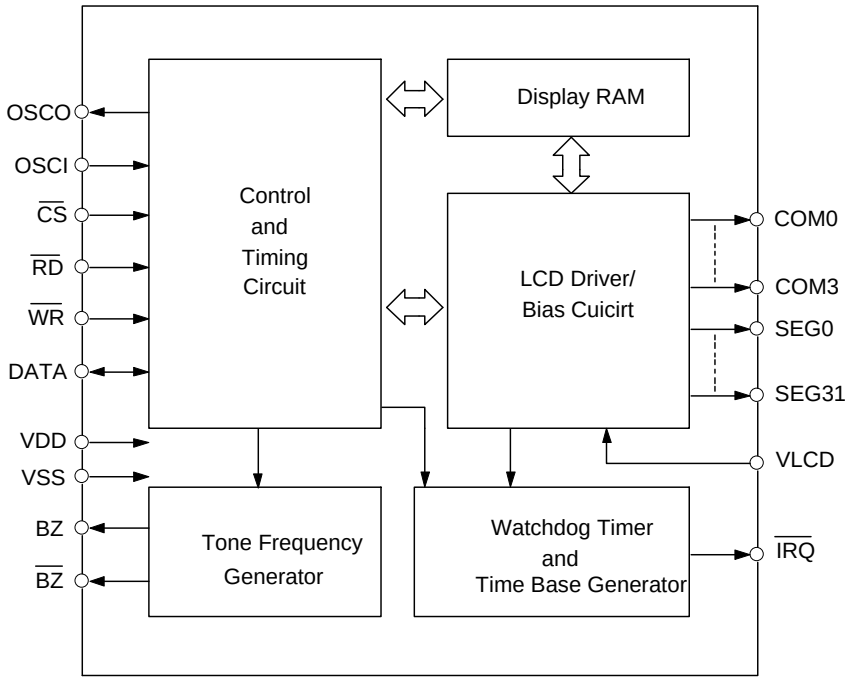


ET6621QN(LQFP48)

Pad Description

Pin No. (ET6621S)	Pin Name	I/O	Function
9	$\overline{CS}$	I	Chip selection input with pull-high resistor When the $\overline{CS}$ is logic high, the data and command read from or written to the ET6621 are disabled. The serial interface circuit is also reset. But if $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the ET6621 are all enabled.
10	$\overline{RD}$	I	READ clock input with pull-high resistor Data in the RAM of the ET6621 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
11	$\overline{WR}$	I	WRITE clock input with pull-high resistor Data on the DATA line are latched into the ET6621 on the rising edge of $\overline{WR}$ signal.
12	DATA	I/O	Serial data input/output with pull-high resistor.
13	VSS	—	Negative power supply, ground
15	OSCI	I	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
14	OSCO	O	
16	VLCD	I	LCD power input.
17	VDD	—	Positive power supply.
18	$\overline{IRQ}$	O	Time base or WDT overflow flag, NMOS open drain output.
19，20	$\overline{BZ}$, BZ	O	2kHz or 4kHz tone frequency output pair.
21～24	COM0～COM3	O	LCD common outputs.
1～8 25～48	SEG7～SEG0 SEG31～SEG8	O	LCD segment outputs.

Block Diagram



Functional Description

Display Memory — RAM

The static display memory (RAM) is organized into 32×4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern：

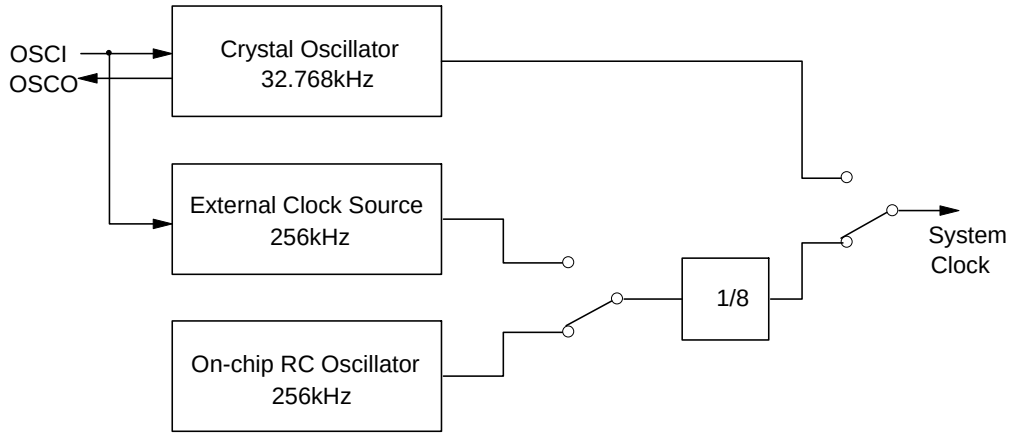
	COM3	COM2	COM1	COM0		
SEG0					0	Address 6 Bits （A5，A4┈A0）
SEG1					1	
SEG2					2	
SEG3					3	
┆					┆	
SEG31					31	
	D3	D2	D1	D0	Data\Addr	

System Oscillator

The ET6621 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its

function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, the ET6621 is at the SYS DIS state.



System Oscillator Configuration

Time Base and Watchdog Timer (WDT)

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The out puts of the time base generator and of the WDT time-out flag can be connected to the $\overline{IRQ}$ output by a command option. There are totally eight frequency sources avail able for the time base generator and the WDT clock. The frequency is calculated by the following equation：

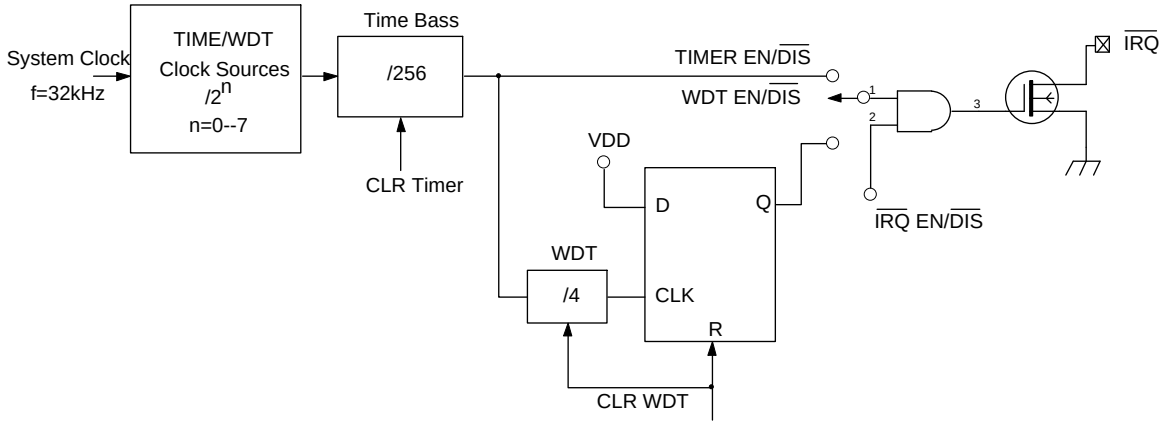
$$f_{WDT} = \frac{32kHz}{2^n}$$ (where the value of n ranges from 0 to 7 by command options).

The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (256kHz), or an external frequency of 256kHz.

If an on-chip oscillator (256kHz) or an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the $\overline{IRQ}$ pin). After the TIMER EN command is transferred, the WDT is disconnected from the $\overline{IRQ}$ pin, and the output of the time base generator is connected to the $\overline{IRQ}$ pin. The WDT can be cleared by executing the CLR WDT command and

the contents of the time base generator is cleared by executing the CLR WDT or the CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command respectively. Before executing the $\overline{IRQ}$ EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will stay at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued. After the $\overline{IRQ}$ output is disabled the $\overline{IRQ}$ pin will remain at the floating state. The $\overline{IRQ}$ output can be enabled or disabled by executing the $\overline{IRQ}$ EN or the $\overline{IRQ}$ DIS command, respectively. The $\overline{IRQ}$ EN makes the output of the time base generator or of the WDT time-out flag appear on the $\overline{IRQ}$ pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions.

On the other hand, if an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the ET6621 will continue working until system power fails or the external clock source is removed. After the system power on, the $\overline{IRQ}$ will be disabled.



Timer and WDT Configuration

Tone Output

A simple tone generator is implemented in the ET6621. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$, which are used to generate a single tone. By executing the TONE4K and TONE2K commands there are two tone frequency outputs select-able. The TONE4K and TONE2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone out puts, namely BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will remain at low level.

Name	Command Code	Function
Tone Off	0000-1000-X	Turn off the Tone Output
4k Tone	010X-XXXX-X	Turn on the Tone Output，The Frequency is 4kHz
2k Tone	0110-XXXX-X	Turn on the Tone Output，The Frequency is 2kHz

LCD Driver

The ET6621 is a 128 (32×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the ET6621 suitable for multiply LCD application. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

Name	Command Code	Function
LCD OFF	**100**00000010X	Turn Off LCD Outputs
LCD ON	**100**00000011X	Turn On LCD Outputs
BIAS&COM	**100**0010abXcX	c=0：1/2 bias
		c=1：1/3 bias
		ab=00：2 COMS
		ab=01：3 COMS
		ab=10：4 COMS

The bold form of 100,namely 1 0 0, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command, will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. Using the LCD related commands, the ET6621 can be compatible with most types of LCD panels.

Command Format

The ET6621 can be configured by the S/W setting. There are two mode commands to configure the ET6621 re sources and to transfer the LCD display data. The configuration mode of the ET6621 is called command mode, and its command mode ID is 1 0 0. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID：

Operation	Mode	ID
Read	Date	110
Write	Date	101
Read-Modify-Write	Date	101
Command	Command	100

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely 1 0 0, can be omitted. While the system is operating in the non-successive command or the non-successive ad dress data mode, the $\overline{CS}$ pin should be set to “1”and the previous operation mode will be reset also. Once the $\overline{CS}$ pin returns to “0”a new operation mode ID should be issued first.

Interfacing

Only four lines are required to interface with the ET6621. The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the ET6621.

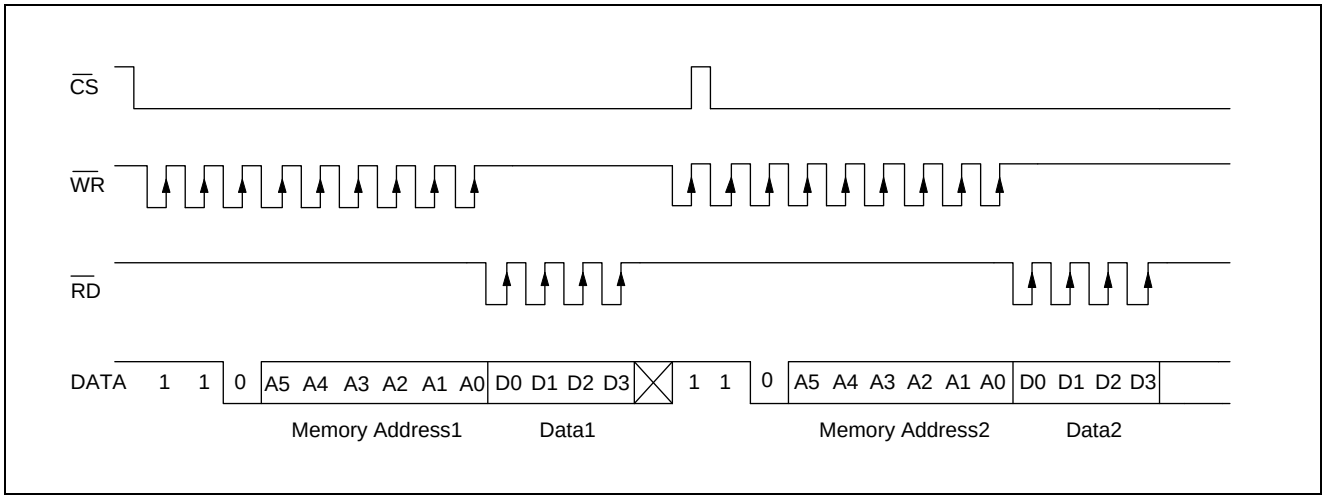
If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the ET6621 are first disabled and then initialized. Be fore issuing a mode command or mode switching, a high level pulse is

required to initialize the serial interface of the ET6621. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval be tween the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input.

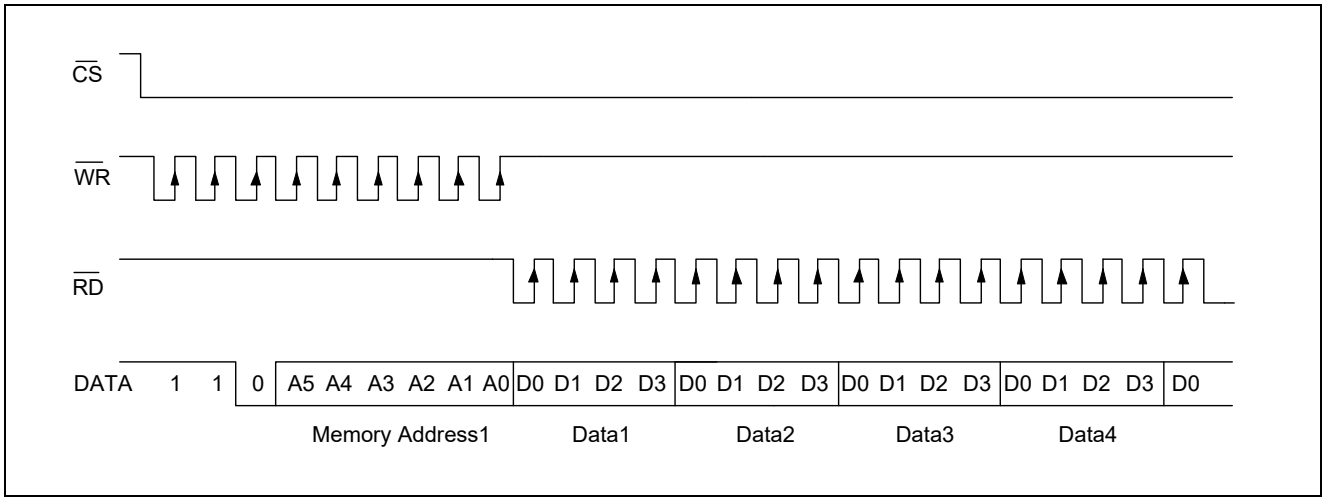
The data, address, and command on the DATA line are all clocked into the ET6621 on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the ET6621. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the $\overline{IRQ}$ pin of the ET6621.

Timing Diagrams

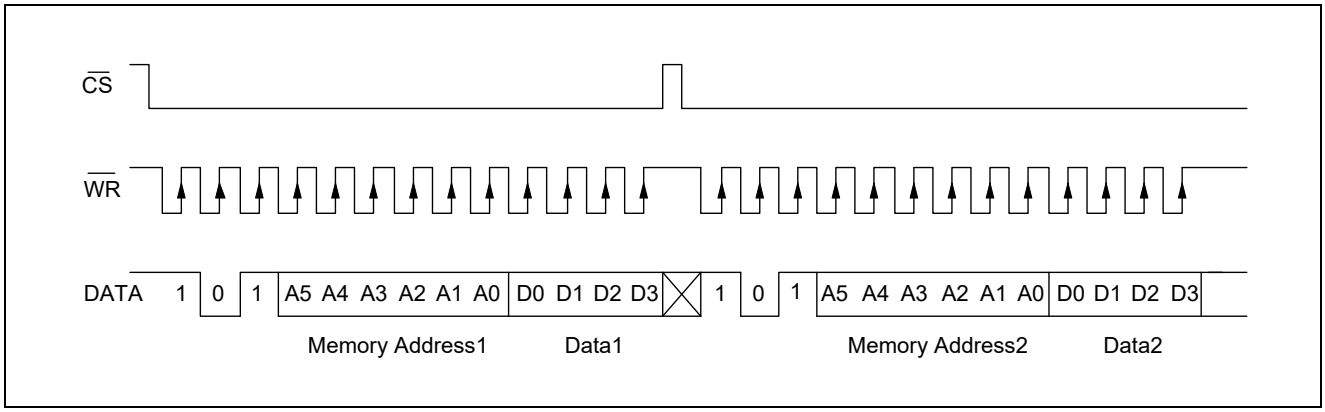
READ Mode (Command Code:110)



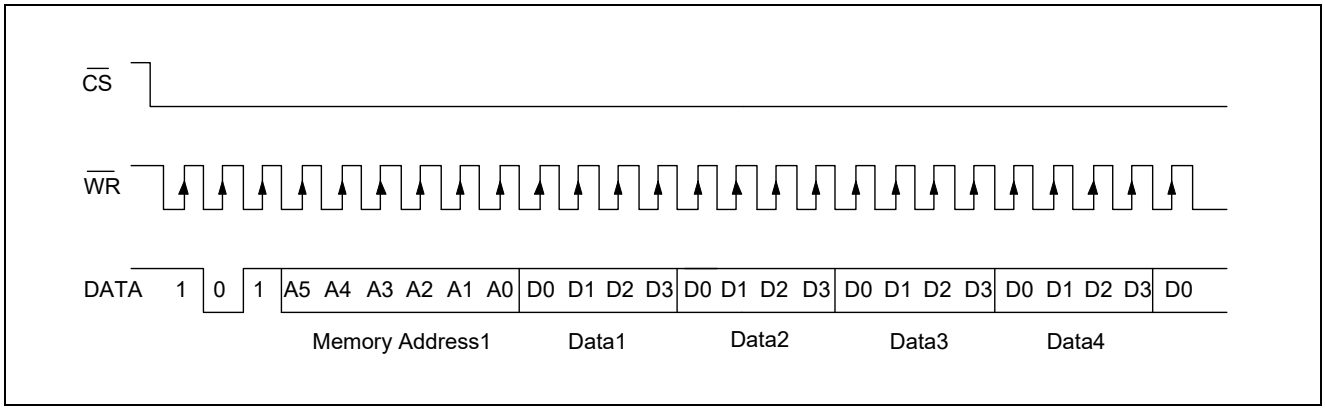
READ Mode (Successive Address Reading)



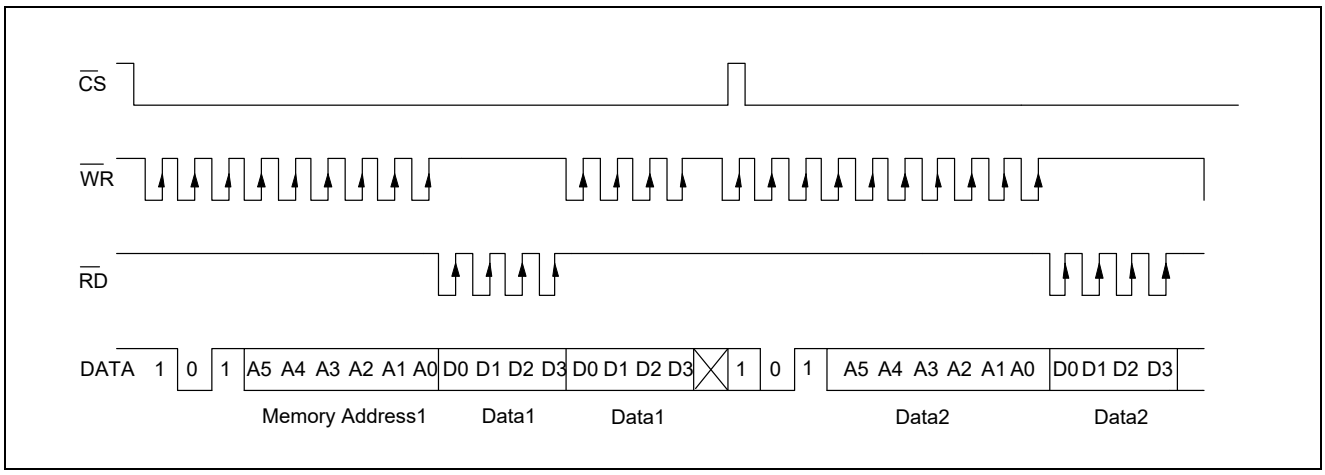
WRITE Mode (Command Code:101)



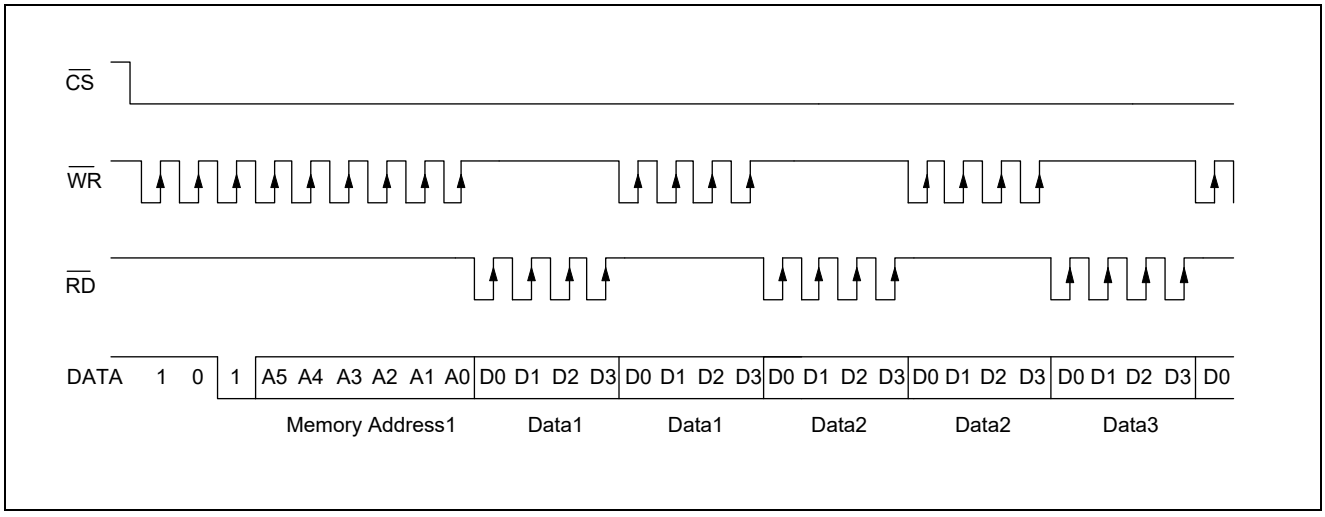
WRITE Mode (Successive Address Writing)



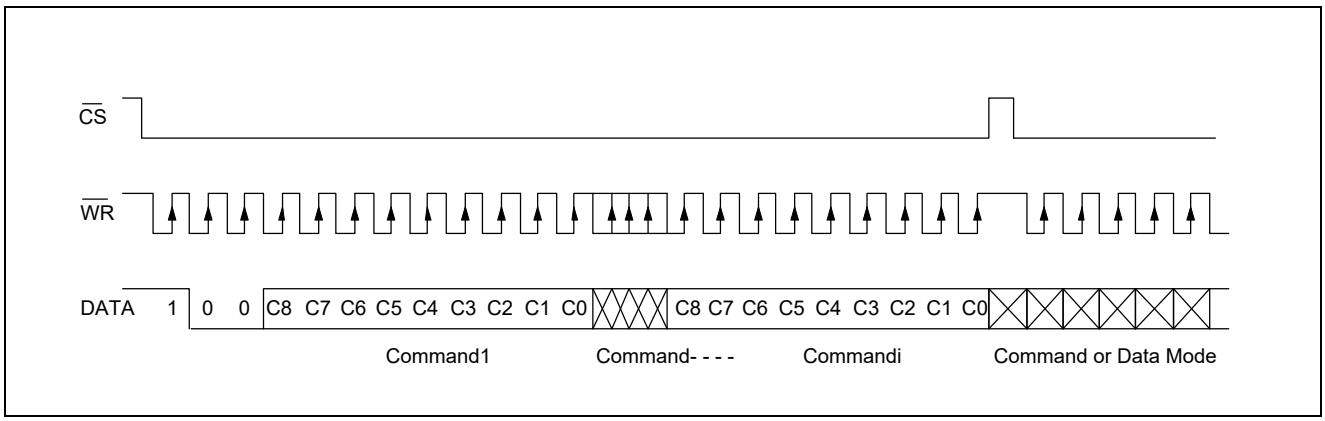
Read-Modify-Write Mode (Command Code:101)



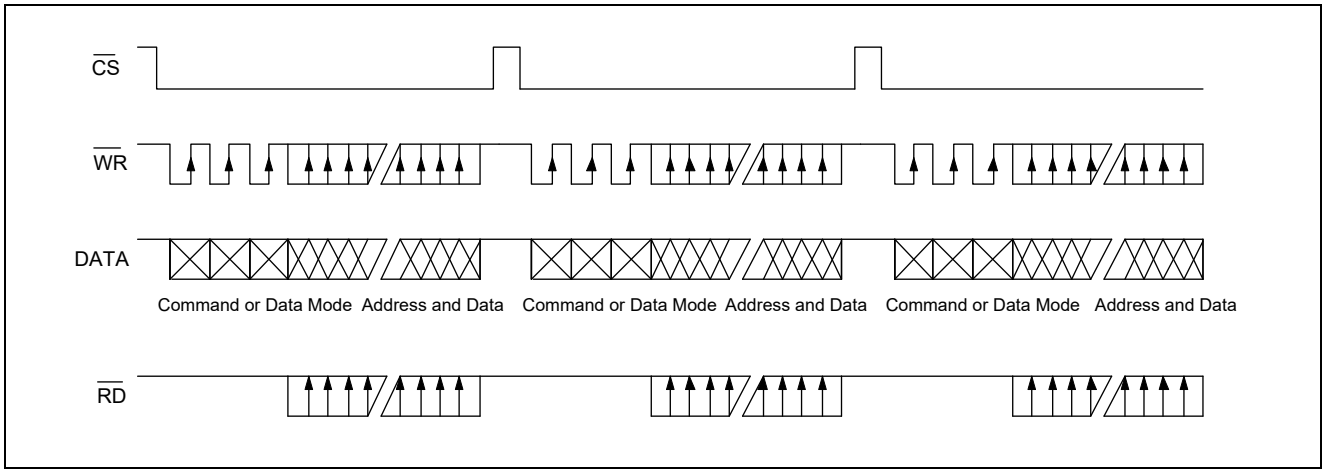
Read-Modify-Write Mode (Successive Address Accessing)



Command Mode (Command Code:100)



Mode (Data And Command Mode)



Command Summary

Name	ID	Command Code	D/C	Function	Def
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	YES
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
TIMERS DIS	100	0000-0100-X	C	Disable time base output	
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	C	Turn off tone outputs	YES
TONE ON	100	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	100	0000-11XX-X	C	Clear the contents of time base generator	

Command Summary (Continued)

Name	ID	Command Code	D/C	Function	Def
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32k	100	0001-01XX-X	C	System clock source, crystal oscillator	
RC 256k	100	0001-10XX-X	C	System clock source, on-chip RC oscillator	YES
EXT 256k	100	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	100	0010-abX0-X	C	LCD 1/2 bias option ab=00：2 COMS ab=01：3 COMS ab=10：4 COMS	
BIAS 1/3	100	0010-abX1-X	C	LCD 1/3 bias option ab=00：2 COMS ab=01：3 COMS ab=10：4 COMS	
TONE 4k	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2k	100	011X-XXXX-X	C	Tone frequency, 2kHz	
$\overline{\text{IRQ}}$ DIS	100	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	YES
$\overline{\text{IRQ}}$ EN	100	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	100	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	100	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	100	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	100	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	YES
TEST	100	1110-0000-X	C	Test mode, user don't use.	
NORMAL	100	1110-0011-X	C	Normal mode	YES

Note：A5～A0：RAM Address
D3～D0：RAM data
D/C：Data/Command Mode

Absolute Maximum Ratings

Parameter	Symbol	Range	Unit
Supply Voltage	V_{DD}	-0.3～5.5	V
Input Voltage	V_{IN}	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+125	˚C
Operating Junction Temperature	T_J	-40～+150	˚C

Recommended Operating Conditions

Parameter	Symbol	Range	Unit
Supply Voltage	V_{DD}	2.4～5.2	V
Operating Temperature	T_A	-40～+85	˚C

Electronic Characteristics

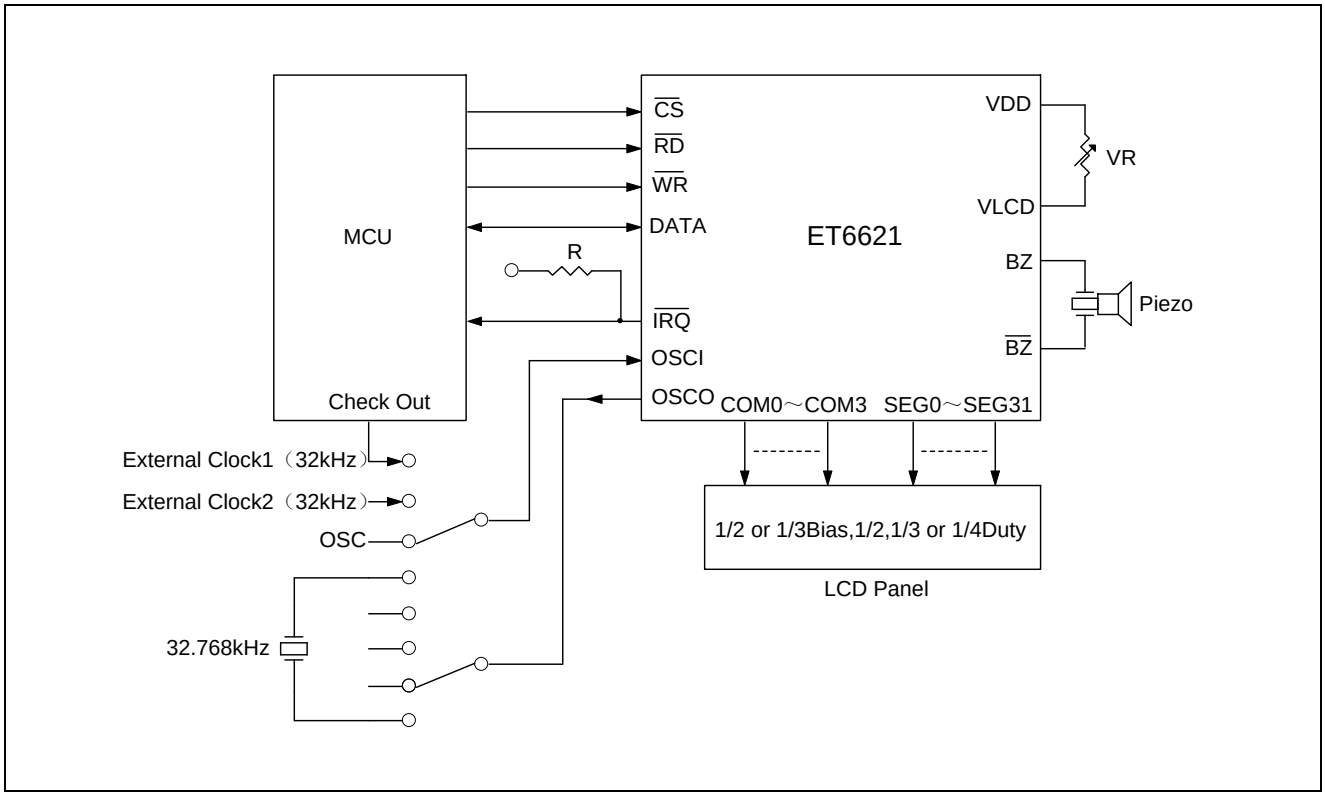
D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions	
						VDD	Conditions
Operating Voltage	V_{DD}	2.4	—	5.2	V	—	—
Operating Current	I_{DD1}	—	150	300	μA	3V	No load/LCD ON On-chip RC oscillator
		—	300	600		5V	
Operating Current	I_{DD2}	—	60	120	μA	3V	No load/LCD ON Crystal oscillator
		—	120	240		5V	
Operating Current	I_{DD3}	—	100	200	μA	3V	No load/LCD ON External clock source
		—	200	400		5V	
Standby Current	I_{STB}	—	0.1	5	μA	3V	No load, Power down mode
		—	0.3	10		5V	
Input Low Voltage	V_{IL}	0	—	0.6	V	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$
		0	—	1.0		5V	
Input High Voltage	V_{IH}	2.4	—	3.0	V	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$
		4.0	—	5.0		5V	
DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$	I_{OL1}	0.5	1.2	—	mA	3V	V_{OL} =0.3V
		1.3	2.6	—		5V	V_{OL} =0.5V
DATA, BZ, $\overline{BZ}$	I_{OH1}	-0.4	-0.8	—	mA	3V	V_{OH} =2.7V
		-0.9	-1.8	—		5V	V_{OH} =4.5V
LCD Common Sink Current	I_{OL2}	80	150	—	μA	3V	V_{OL} =0.3V
		150	250	—		5V	V_{OL}=0.5V
LCD Common Source Current	I_{OH2}	-80	-120	—	μA	3V	V_{OH} =2.7V
		-120	-200	—		5V	V_{OH} =4.5V
LCD Segment Sink Current	I_{OL3}	60	120	—	μA	3V	V_{OL} =0.3V
		120	200	—		5V	V_{OL} =0.5V
LCD Segment Source Current	I_{OH3}	-40	-70	—	μA	3V	V_{OH} =2.7V
		-70	-100	—		5V	V_{OH} =4.5V
Pull-high Resistor	R_{PH}	40	80	150	KΩ	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$
		30	60	100		5V	

A.C. Characteristics

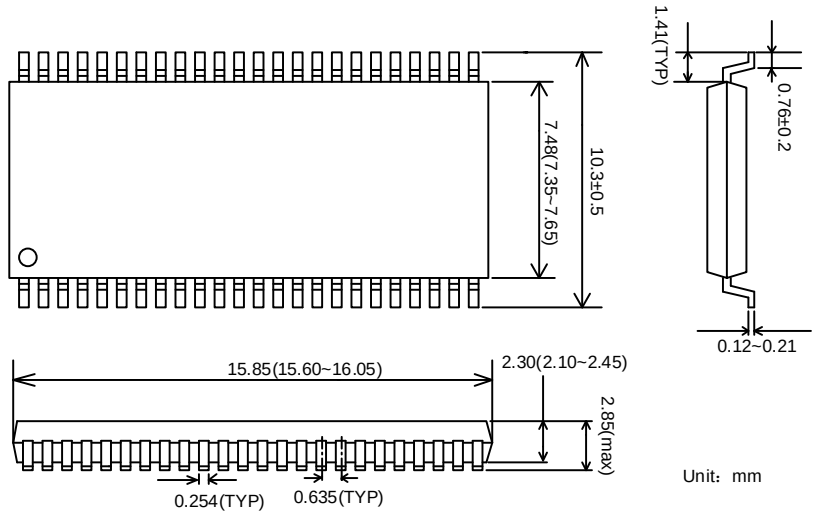
Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	—	256	—	kHz	3V	On-chip RC oscillator
		—	256	—		5V	
System Clock	f_{SYS2}	—	32.768	—	kHz	3V	Crystal oscillator
		—	32.768	—		5V	
System Clock	f_{SYS3}	—	256	—	kHz	3V	External clock source
		—	256	—		5V	
LCD Clock	f_{LCD1}	—	f_{SYS1}/1024	—	Hz	—	On-chip RC oscillator
		—	f_{SYS2}/128	—			Crystal oscillator
		—	f_{SYS3}/1024	—			External clock source
LCD Common Period	t_{COM}	—	n/ f_{LCD}	—	sec	—	n:Number of COM
Serial Data Clock ($\overline{WR}$ pin)	F_{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Data Clock ($\overline{RD}$ pin)	F_{CLK2}	—	—	75	kHz	3V	Duty cycle 50%
		—	—	150		5V	
Serial Interface Reset Pulse Width	t_{CS}	—	250	—	ns	—	$\overline{CS}$
$\overline{WR}$, $\overline{RD}$ Input Pulse Width	t_{CLK}	3.34	—	—	μs	3V	Write mode
		6.67	—	—			Read mode
		1.67	—	—	μs	5V	Write mode
		3.34	—	—			Read mode
Rise/Fall Time Serial Data Clock Width	t_r, t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	

Application Circuits



Package Dimension

SSOP48



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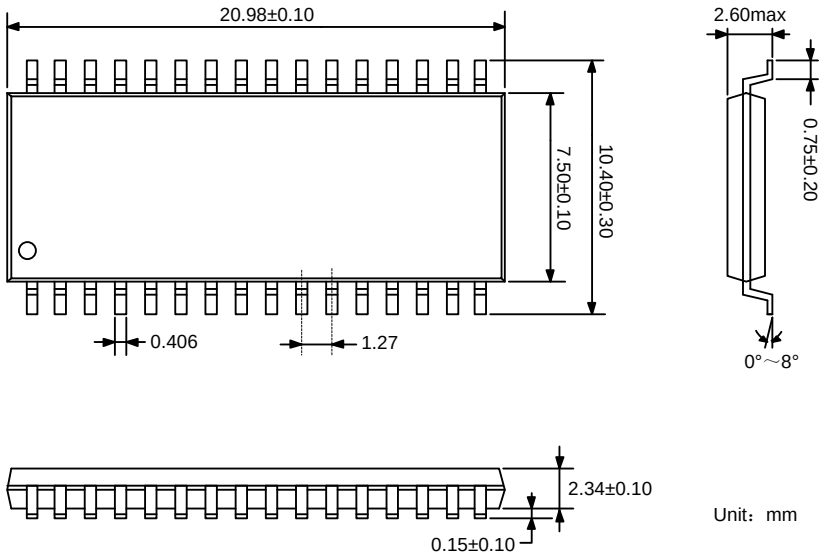

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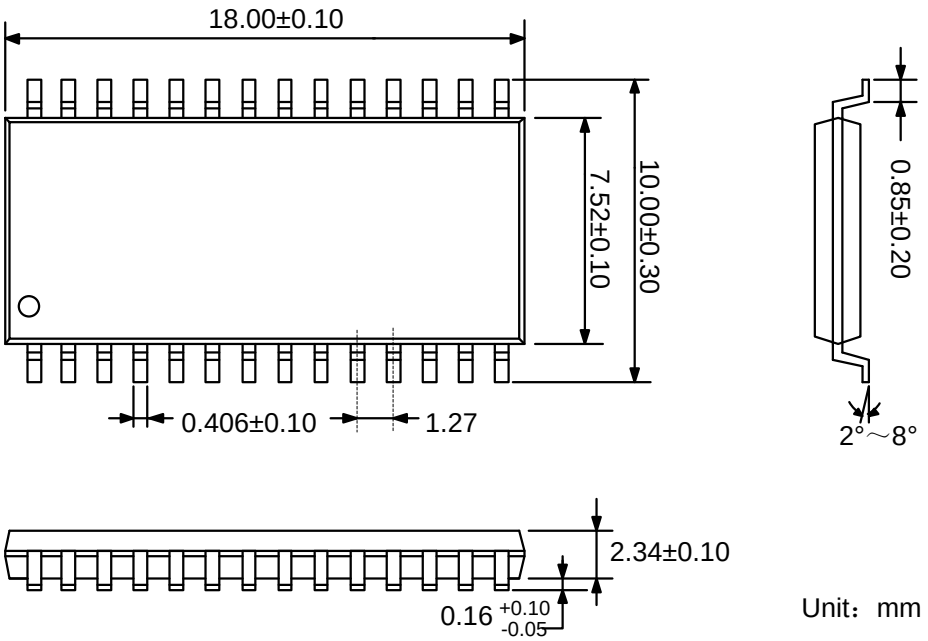

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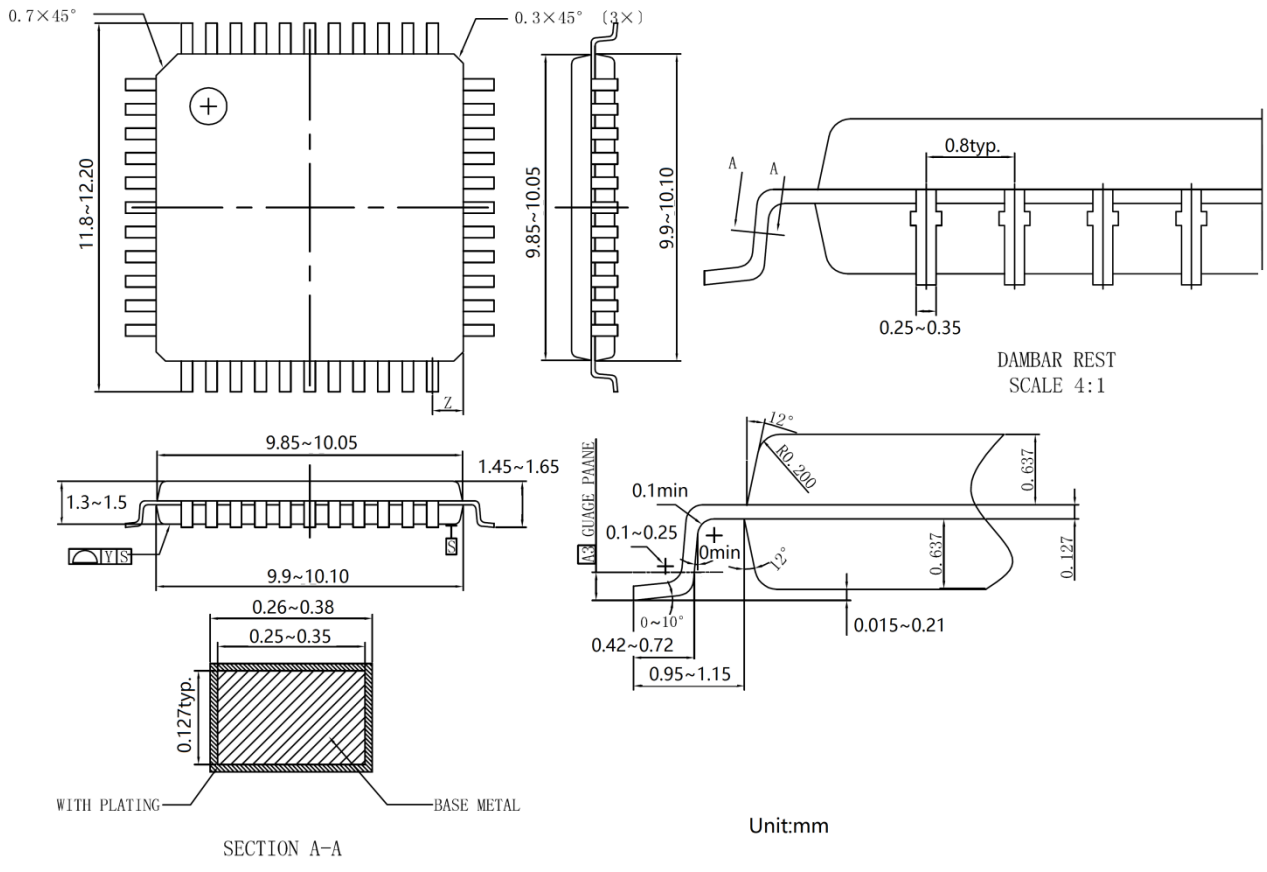

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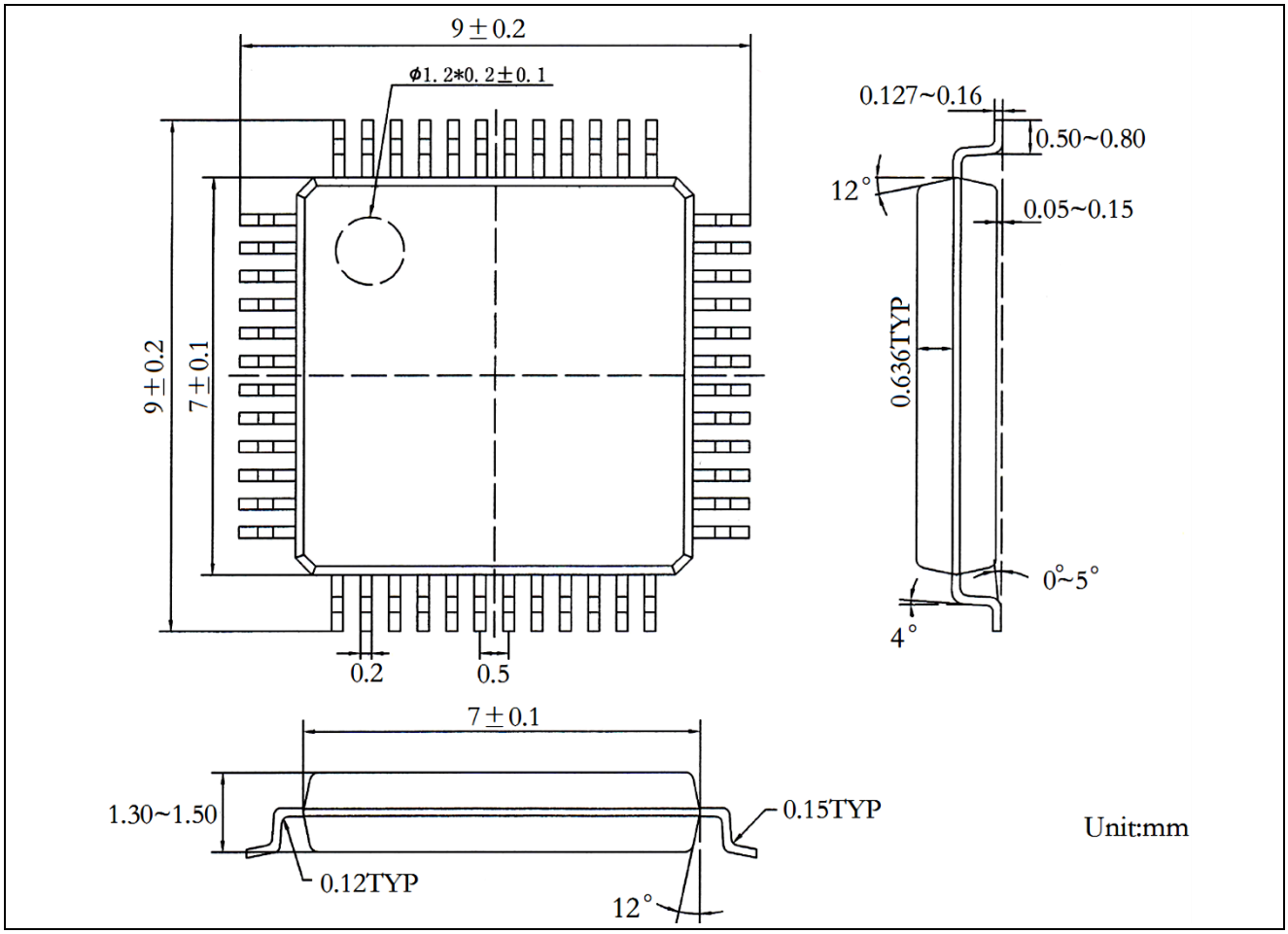

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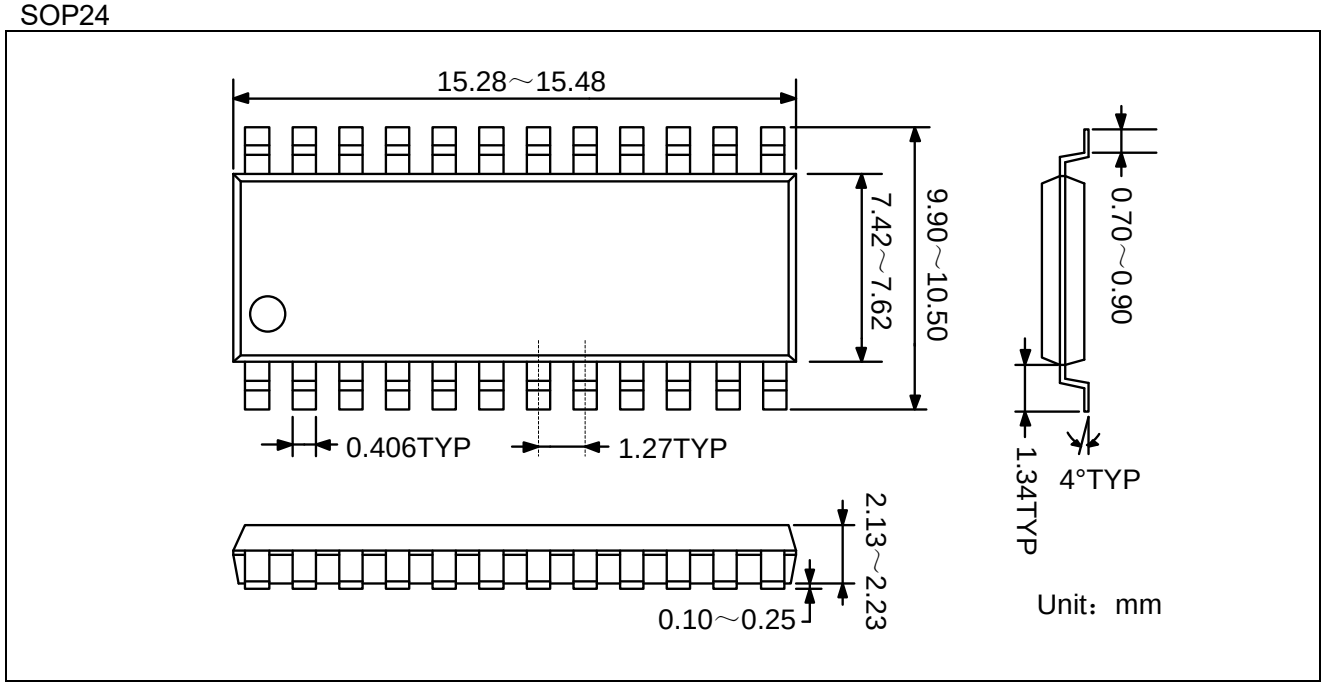

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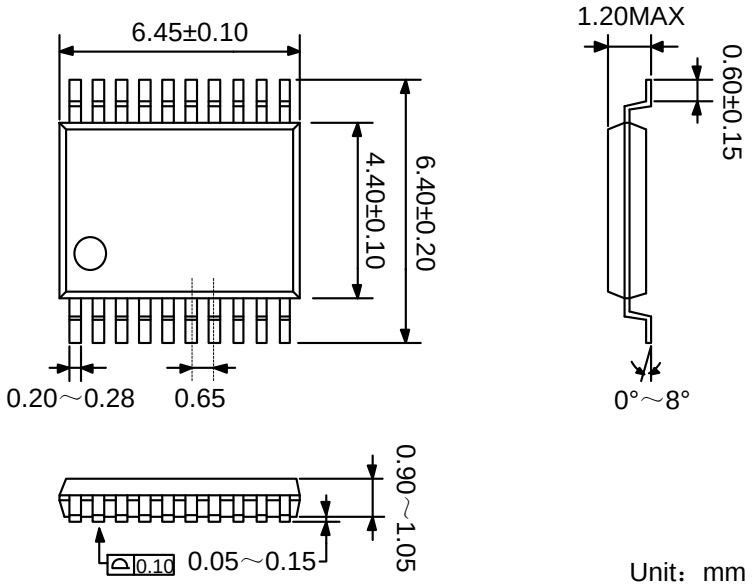

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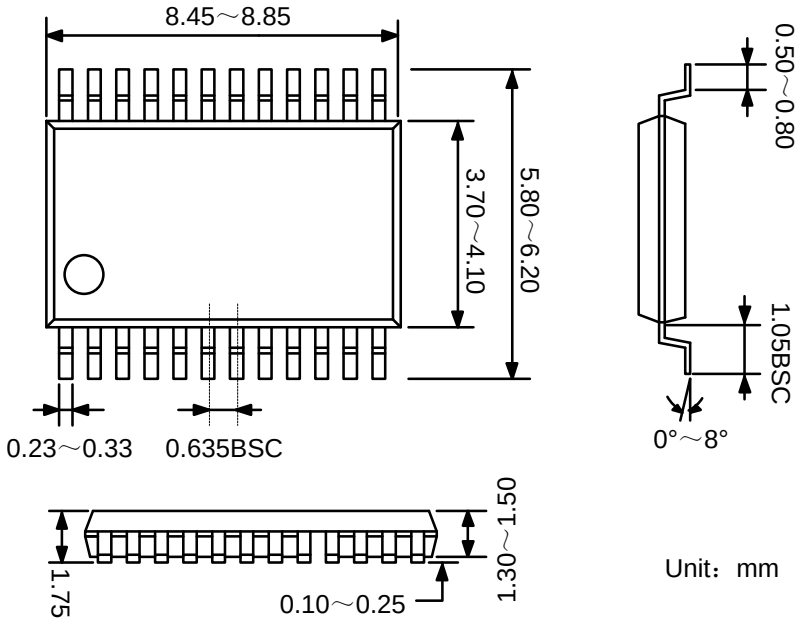

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
2.2	2017-12-12	Add LQFP44 Package	Wanggp	Wanggp	Zhujl
2.3	2018-01-08	Add ET6621QH and its configuration	Wanggp	Wanggp	Zhujl
2.4	2018-03-02	Add QFN24 Package	Wanggp	Wanggp	Zhujl
2.5	2018-08-13	Add TSSOP20& SSOP24Package	Wanggp	Wanggp	Liujy
2.6	2020-04-20	Formalize format	Shib	Shib	Shib
2.7	2020-11-16	Update TOTG	Wanggp	Wanggp	Liujy
2.8	2022-12-12	Update Typos	Wanggp	Wanggp	Zhujl