ET6416 - 16 bit I²C-bus/SMBus I/O Expander

General description

The ET6416 is a 16-bit general purpose I/O expander that provides remote I/O expansion for most micro-controller families via the I²C-bus interface.

ET6416 provides a simple solution for I/O port expansion, which can be realized with little interconnection. In addition to providing a set of flexible GPIO ports, it also supports the level conversion between different voltage devices, so that it can be flexibly applied in multi voltage mixed signal environment.

ET6416 has two supply voltage port: VDDI and VDDP, VDDI provides the power supply voltage for the interface of the main control terminal(micro-controller) and VDDP provides the power supply voltage for the core circuit and Port P.

ET6416 has four pairs of 8-bits registers: configuration register, input register, output register and polarity reversal register.

When power-on, all I/O ports are configured to input status. By configuring the I/O ports' configuration register, the system can determine the input and output status of each I/O port. Each input or output data is stored in the corresponding input or output register. The polarity of input registers can be flipped by configuring polarity reversal registers to save external logic gates.

When time-out or error operation occurs, the host can reset ET6416 by applying a low level on $\overline{\text{RESET}}$ Port. When power on $\overline{\text{RESET}}$, all registers are in default state, and I²C BUS/SM BUS state machine is initialized.

When any input state is different from its corresponding input register state, the ET6416 open drain interrupt $\overline{\text{INT}}$ output is active to indicate to the host that the input state has changed.

The $\overline{\text{INT}}$ can be connected to the interrupt input of the micro-controller. By sending the interrupt signal, the microcontroller port is informed that there is data entering, instead of passing through I²C BUS.

The Port P output of ET6416 can provide 25mA perfusion current, which can directly drive LED.

The hardware address pin (ADDR) can be used to program and change the I²C BUS address.

Features

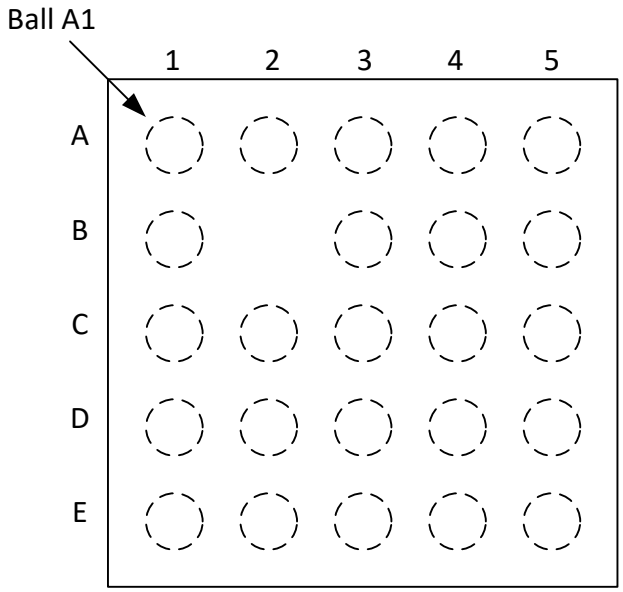
- I²C-BUS to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Allows bidirectional voltage-level translation and GPIO expansion between:
  - 1.8 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 2.5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 3.3 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P

- Low standby current consumption:
  - 1.5uA typical at V_{DDP} = 5 V
  - 1.0uA typical at V_{DDP} = 3.3 V
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - V_{HYS} = 0.18 V (typical) at 1.8 V
  - V_{HYS} = 0.25 V (typical) at 2.5 V
  - V_{HYS} = 0.33 V (typical) at 3.3 V
  - V_{HYS} = 0.5 V (typical) at 5 V
- Active LOW reset input $\overline{RESET}$
- Open-drain active LOW interrupt output $\overline{INT}$
- 400 kHz Fast-mode I^2C-BUS
- Input/Output configuration register
- Polarity Inversion register
- Internal power-on reset
- Power-up with all channels configured as inputs
- No glitch on power-up
- Noise filter on SCL/SDA inputs
- Outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA
- ESD protection exceeds
  - ±2000 V Human-Body Model PASS
  - ±1000 V Charged-Device Model PASS
- Package: VFBGA24

Device Information

Part No.	Package	Size
ET6416	VFBGA24	3mm × 3mm × 0.85mm

Pin Assignments



1	2	3	4	5	
P0_0	$\overline{\text{RESET}}$	$\overline{\text{INT}}$	SDA	SCL	A
P0_2		V_{DDI}	V_{DDP}	ADDR	B
P0_3	P0_4	P0_1	P1_7	P1_6	C
P0_5	P0_7	P1_2	P1_4	P1_5	D
P0_6	V_{SS}	P1_0	P1_1	P1_3	E

ET6416(VFBGA24)

Figure 1. Pin Assignments (Top View)

Pin. Function

Symbol	Pin	Description
$\overline{\text{INT}}$	A3	Interrupt output. Connect to V_{DDI}(I^2C-BUS) or V_{DDP} through a pull-up resistor.
V_{DDI}	B3	Supply voltage of I^2C-bus. Connect directly to the VDD of the external I^2C master. Provides voltage-level translation.
$\overline{\text{RESET}}$	A2	Active LOW reset input. Connect to V_{DD}(I^2C-BUS) through a pull-up resistor if no active connection is used.
P0_0	A1	Port 0 input/output 0.
P0_1	C3	Port 0 input/output 1.
P0_2	B1	Port 0 input/output 2.
P0_3	C1	Port 0 input/output 3.
P0_4	C2	Port 0 input/output 4.
P0_5	D1	Port 0 input/output 5.
P0_6	E1	Port 0 input/output 6.
P0_7	D2	Port 0 input/output 7.
V_{SS}	E2	GND
P1_0	E3	Port 1 input/output 0.
P1_1	E4	Port 1 input/output 1.
P1_2	D3	Port 1 input/output 2.
P1_3	E5	Port 1 input/output 3.
P1_4	D4	Port 1 input/output 4.

Symbol	Pin	Description
P1_5	D5	Port 1 input/output 5.
P1_6	C5	Port 1 input/output 6.
P1_7	C4	Port 1 input/output 7.
ADDR	B5	Address input. Connect directly to V_{DDP} or ground.
SCL	A5	Serial clock bus. Connect to V_{DD}(I^2C-bus) through a pull-up resistor.
SDA	A4	Serial data bus. Connect to V_{DD}(I^2C-bus) through a pull-up resistor.
V_{DDP}	B4	Supply voltage of ET6416 for Port P.

Block Diagram

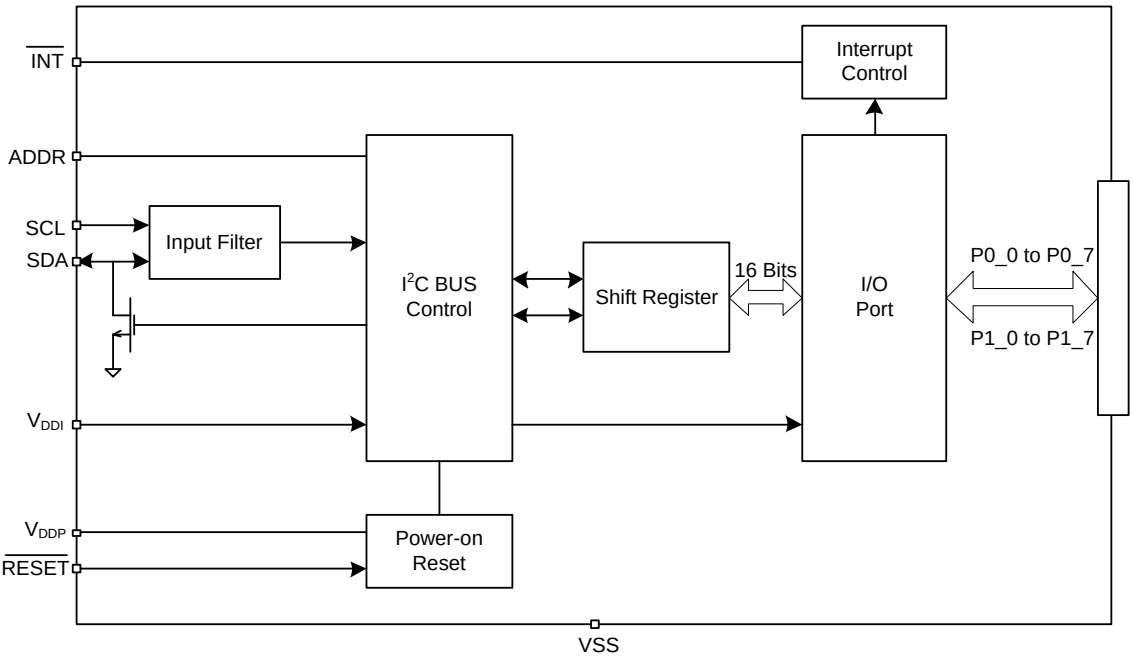


Figure 2. Block Diagram

Functions Description

Voltage Translation

V_{DDI} (SDA and SCL)	V_{DDP} (Port P)
1.8 V ~ 5.0V	1.8 V ~ 5.0V

BUS Transactions

The ET6416 is an I²C-bus slave device. Data is exchanged between the master and ET6416 through write and read commands using I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Chip Address

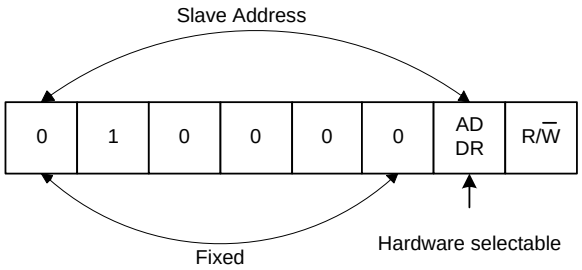


Figure 3. Chip address

ADDR is the hardware address package pin and is held to either HIGH (logic 1) or LOW (logic 0) to assign one of the two possible slave addresses. The last bit of the slave address (R/$\overline{W}$) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

Write Commands

Data is transmitted to the ET6416 by sending the device address and setting the Least Significant Bit (LSB) to a logic '0'. The command byte is sent after the address and determines which register receives the data that follows the command byte.

The eight registers within the ET6416 are configured to operate as four register pairs. The four pairs are input Resisters, output Resisters, polarity inversion and configuration Registers. After sending data to one register, the next data byte is sent to the other register in the pair. For example, if the first byte is sent to Output Resisters1 (register 3), the next byte is stored in Output Resisters0 (register 2).

There is no limit on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register pair independently of the other registers or the host can update a single register.

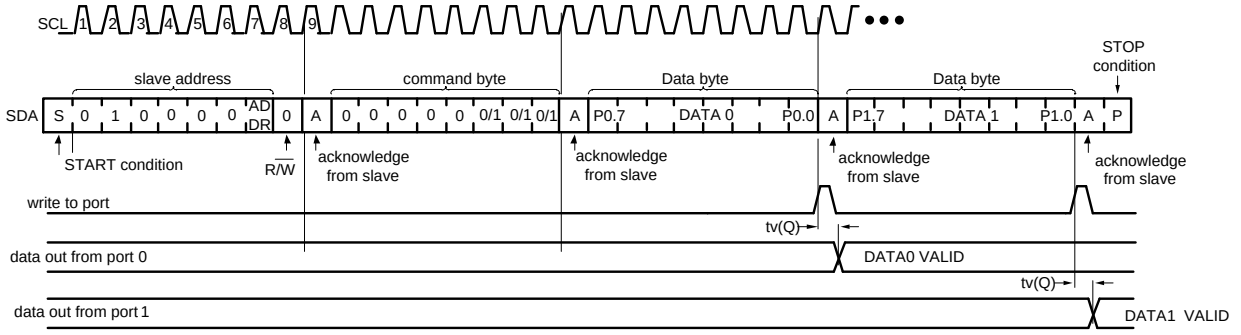


Figure 4. Write Commands

Read Commands

To read data from the ET6416, the bus master must first send the ET6416 address with the least significant bit set to a logic ‘0’. The command byte is sent after the address and determines which register is to be accessed.

After a restart, the device address is sent again, but this time the least significant bit is set to a logic ‘1’. Data from the register defined by the command byte is sent by the ET6416. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflects the information in the other register in the pair. For example, if Input Resisters 1 is read, the next byte read is Input Resisters 0.There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

After a subsequent restart, the command byte contains the value of the next register to be read in the pair. For example, if Input Resisters 1 was read last before the restart, the register that is read after the restart is the Input Resisters 0.

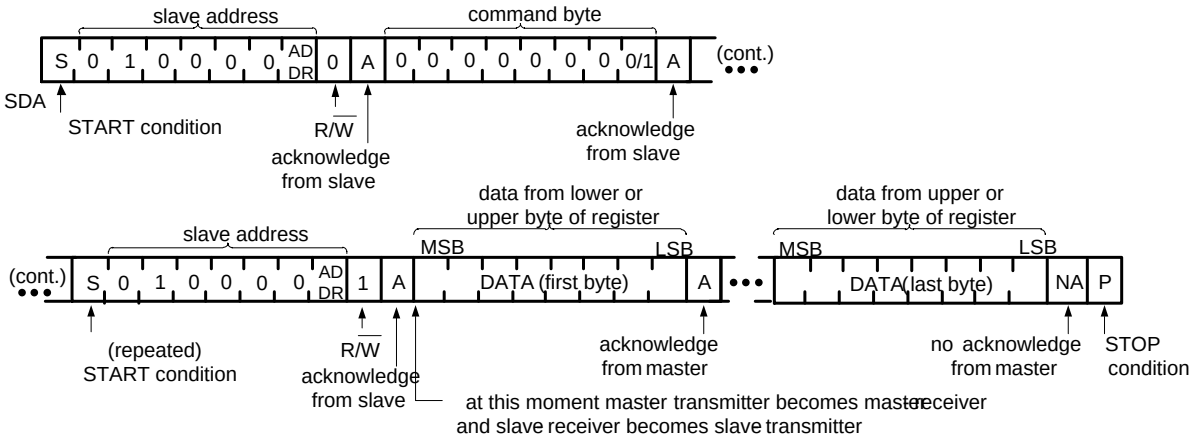


Figure 5. Read Commands

I/O Port

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either VDDP or VSS . The external

voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

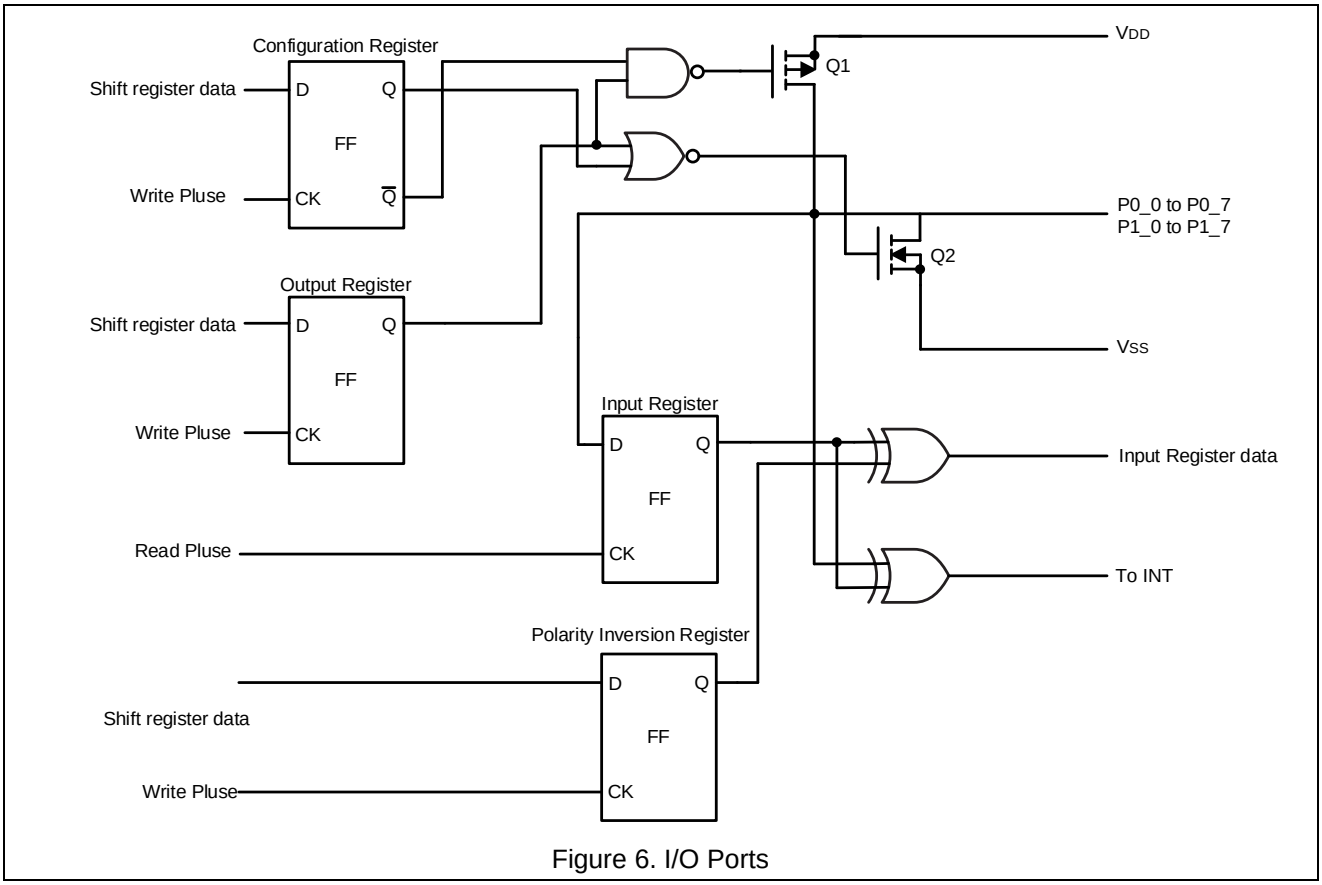


Figure 6. I/O Ports

Power-on Reset

When power (from 0 V) is applied to VDDP , an internal power-on reset holds the ET6416 in a reset condition until VDDP has reached VPOR. At that time, the reset condition is released and the ET6416 registers and I²C-bus/SMBus state machine initializes to their default states. After that, VDDP must be lowered to below VPOR and back up to the operating voltage for a power-reset cycle.

Reset Input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping the VDDP at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of tw(rst) . The ET6416 registers and I²C-bus/SMBus state machine are changed to their default state once $\overline{\text{RESET}}$ is LOW (0). When $\overline{\text{RESET}}$ is HIGH (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pull-up resistor to VDDI(I²C-bus) if no active connection is used.

Interrupt Output ($\overline{\text{INT}}$)

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time to V(INT) , the signal $\overline{\text{INT}}$ is valid. The interrupt is reset when data on the port changes back to the original value or when data is read from the port that generated the interrupt. Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the I/Os after resetting is detected and is transmitted as $\overline{\text{INT}}$.

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to VDDP or VDDI(I^2C-bus) depending on the application. $\overline{INT}$ should be connected to the voltage source of the device that requires the interrupt information.

Interface definition

Byte	Bit							
	7(MSB)	6	5	4	3	2	1	0(LSB)
I^2C-BUSslave address	L	H	L	L	L	L	ADDR	R/$\overline{W}$
I/O data bus	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Pointer register and Command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the ET6416. The lower three bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register is write only.

While a new command has been sent, the register that was last addressed continues to be accessed by reads until a new command byte is sent.

Pointer Register Bits	Command byte	Register	Protocol	Default Value
0000 0000	00h	Input Registers 0	Read only	xxxx xxxx
0000 0001	01h	Input Registers 1	Read only	xxxx xxxx
0000 0010	02h	Output Registers 0	Read/Write	1111 1111
0000 0011	03h	Output Registers 1	Read/Write	1111 1111
0000 0100	04h	Polarity inversion Registers 0	Read/Write	0000 0000
0000 0101	05h	Polarity inversion Registers 1	Read/Write	0000 0000
0000 0110	06h	Configuration Registers 0	Read/Write	1111 1111
0000 0111	07h	Configuration Registers 1	Read/Write	1111 1111

Register descriptions

Register	Bit	7	6	5	4	3	2	1	0
00h	Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
	Default	X	X	X	X	X	X	X	X
01h	Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
	Default	X	X	X	X	X	X	X	X
02h	Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
	Default	1	1	1	1	1	1	1	1
03h	Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
	Default	1	1	1	1	1	1	1	1
04h	Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
	Default	0	0	0	0	0	0	0	0
05h	Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
	Default	0	0	0	0	0	0	0	0
06h	Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
	Default	1	1	1	1	1	1	1	1
07h	Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
	Default	1	1	1	1	1	1	1	1

Input Registers (00h、01h)

The Input registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect.

The default value ‘X’ is determined by the externally applied logic level.

Output Registers (02h、03h)

The Output registers (registers 2 and 3) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, not the actual pin value.

Polarity inversion Registers (04h、05h)

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with ‘1’), the corresponding port pin’s polarity is inverted in the input register. If a bit in this register is cleared (written with a ‘0’), the corresponding port pin’s polarity is retained.

Configuration Registers (06h、07h)

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output.

Note： When the P port is suspended, configure it to the output state please.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDI}	I^2C-bus supply voltage		-0.5	+6.5	V
V_{DDP}	Supply voltage port P		-0.5	+6.5	V
V_I	Input voltage		-0.5	+6.5	V
V_O	Output voltage		-0.5	+6.5	V
I_{IK}	Input clamping current	ADDR, $\overline{RESET}$, SCL; V_I < 0V	-	±20	mA
I_{OK}	Output clamping current	$\overline{INT}$; V_O < 0V	-	±20	mA
I_{IOK}	Input/output clamping current	P port; V_O < 0V or V_O > V_{DDP}	-	±20	mA
		SDA; V_O < 0V or V_O > V_{DDI}	-	±20	mA
I_{OL}	LOW-level output current	P port; V_O = 0V to V_{DDP}	-	50	mA
		SDA, $\overline{INT}$; V_O = 0V to V_{DDI}	-	25	mA
I_{OH}	HIGH-level output current	P port; V_O = 0V to V_{DDP}	-	25	mA
I_{DD}	Supply current	through V_{SS}	-	200	mA
I_{DDP}	Supply current port P	through V_{DDP}	-	160	mA
I_{DDI}	I^2C-bus supply current	through V_{DDI}	-	10	mA
T_{STG}	Storage temperature		-65	+150	˚C
T_{JMAX}	Maximum junction temperature		-	150	˚C
$R_{\theta JA}$	Transient thermal impedance from junction to ambient	VFBGA24		171	˚C/W

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDI}	I^2C-bus supply voltage		1.65	5.5	V
V_{DDP}	Supply voltage port P		1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA, $\overline{RESET}$	0.7×V_{DDI}	5.5	V
		ADDR, P1_7 to P0_0	0.7×V_{DDP}	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA, $\overline{RESET}$	-0.5	0.3×V_{DDI}	V
		ADDR, P1_7 to P0_0	-0.5	0.3×V_{DDP}	V
I_{OH}	HIGH-level output current	P1_7 to P0_0	-	10	mA
I_{OL}	LOW-level output current	P1_7 to P0_0	-	23	mA
T_A	Ambient temperature	Operating in free air	-40	+85	˚C

Electrical Characteristics

D.C. Characteristics

T_A = 25°C;V_{DDI} = 1.65V to 5.5V; (Unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IK}	Input clamping voltage	I_I = -18mA	-1.2	-	-	V
V_{POR}	Power-on reset voltage	V_I = V_{DDP} or V_{SS}; I_O = 0mA	-	1.1	1.4	V
V_{OH}	HIGH-level output voltage	P port				
		I_{OH} = -8mA; V_{DDP} = 1.65V	1.2	-	-	V
		I_{OH} = -10mA; V_{DDP} = 1.65V	1.1	-	-	V
		I_{OH} = -8mA; V_{DDP} = 2.3V	1.8	-	-	V
		I_{OH} = -10mA; V_{DDP} = 2.3V	1.7	-	-	V
		I_{OH} = -8mA; V_{DDP} = 3.0V	2.6	-	-	V
		I_{OH} = -10mA; V_{DDP} = 3.0V	2.5	-	-	V
		I_{OH} = -8mA; V_{DDP} = 4.5V	4.1	-	-	V
		I_{OH} = -10mA; V_{DDP} = 4.5V	4.0	-	-	V
V_{OL}	LOW-level output voltage	P port; I_{OL} = 8 mA				
		V_{DDP} = 1.65V	-	-	0.45	V
		V_{DDP} = 2.3V	-	-	0.25	V
		V_{DDP} = 3.0V	-	-	0.25	V
		V_{DDP} = 4.5V	-	-	0.2	V
I_{OL}	LOW-level output current	V_{OL} = 0.4V; V_{DDP} = 1.65V to 5.5V				
		SDA	3	-	-	mA
		$\overline{INT}$	3	15	-	mA
		P port				
		V_{OL} = 0.5V; V_{DDP} = 1.65V	8	10	-	mA
		V_{OL} = 0.7V; V_{DDP} = 1.65V	10	13	-	mA
		V_{OL} = 0.5V; V_{DDP} = 2.3V	8	10	-	mA
		V_{OL} = 0.7V; V_{DDP} = 2.3V	10	13	-	mA
		V_{OL} = 0.5V; V_{DDP} = 3.0V	8	14	-	mA
		V_{OL} = 0.7V; V_{DDP} = 3.0V	10	19	-	mA
		V_{OL} = 0.5V; V_{DDP} = 4.5V	8	17	-	mA
		V_{OL} = 0.7V; V_{DDP} = 4.5V	10	24	-	mA
I_I	Input current	V_{DDP} = 1.65V to 5.5V				
		SCL, SDA, $\overline{RESET}$; V_I = V_{DDI} or V_{SS}	-	-	±1	uA
		ADDR; V_I = V_{DDP} or V_{SS}	-	-	±1	uA
I_{IH}	HIGH-level input current	P port; V_I = V_{DDP}; V_{DDP} = 1.65V to 5.5V	-	-	1	uA
I_{IL}	LOW-level input current	P port; V_I = V_{SS}; V_{DDP} = 1.65V to 5.5V	-	-	1	uA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	I_{DDI} + I_{DDP}; SDA, P port, ADDR, $\overline{RESET}$; V_I on SDA and $\overline{RESET}$ = V_{DDI} or V_{SS}; V_I on P port and ADDR = V_{DDP}; I_O = 0mA; I/O = inputs; F_{SCL} = 400kHz				
		V_{DDP} = 3.6V to 5.5V	-	10	25	uA
		V_{DDP} = 2.3V to 3.6V	-	6.5	15	uA
		V_{DDP} = 1.65V to 2.3V	-	4	9	uA
		I_{DDI} + I_{DDP}; SCL, SDA, P port, ADDR, $\overline{RESET}$; V_I on SCL, SDA and $\overline{RESET}$ =V_{DDI} or V_{SS};V_I on P port and ADDR= V_{DDP}; I_O = 0mA; I/O = inputs; F_{SCL} = 0kHz				
		V_{DDP} = 3.6V to 5.5V	-	1.5	7	uA
		V_{DDP} = 2.3V to 3.6V	-	1	3.2	uA
		V_{DDP} = 1.65V to 2.3V	-	0.5	1.7	uA
		Active mode;I_{DDI} + I_{DDP}; P port, ADDR, $\overline{RESET}$; V_I on $\overline{RESET}$ = V_{DDI}; V_I on P port and ADDR = V_{DDP}; I_O = 0mA; I/O = inputs; F_{SCL} = 400kHz, continuous register read				
		V_{DDP} = 3.6V to 5.5V	-	60	125	uA
		V_{DDP} = 2.3V to 3.6V	-	40	75	uA
		V_{DDP} = 1.65V to 2.3V	-	20	45	uA
ΔI_{DD}	Additional quiescent supply current	SCL, SDA, $\overline{RESET}$; one input at V_{DDI} - 0.6V, other inputs at V_{DDI} or V_{SS}; V_{DDP} = 1.65V to 5.5V	-	-	25	uA
		P port, ADDR; one input at V_{DDP} - 0.6V, other inputs at V_{DDP} or V_{SS}; V_{DDP} = 1.65V to 5.5V	-	-	80	uA
C_I	Input capacitance	V_I = V_{DDI} or V_{SS} ; V_{DDP} = 1.65V to 5.5V	-	4.2	7	pF
C_{IO}	Input/output capacitance	V_{IO} = V_{DDI} or V_{SS} ; V_{DDP} = 1.65V to 5.5V	-	4.5	8	pF
		V_{IO} = V_{DDP} or V_{SS} ; V_{DDP} = 1.65V to 5.5V	-	4.5	8.5	pF

A.C. Characteristics*

T_A = 25°C;V_{DDI} = 1.65V to 5.5V; (Unless otherwise specified.)

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	us
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	us
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
$t_{SU;DAT}$	Data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	Data hold time		0	-	0	-	ns
t_r	Rise time of both SDA and SCL signals		-	1000	-	300	ns
t_f	Fall time of both SDA and SCL signals			300	-	300	ns
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7	-	0.6	-	us
$t_{HD;STA}$	Hold time (repeated) START condition		4	-	0.6	-	us
$t_{SU;STO}$	Set-up time for STOP condition		4	-	0.6	-	us
$t_{VD;DAT}$	Data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	us
$t_{VD;ACK}$	Data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	us
t_{wrst}	Reset pulse width		30	-	30	-	ns
t_{recrst}	Reset recovery time		200	-	200	-	ns
t_{rst}	Reset time		600	-	600	-	ns
t_{vINT}	Valid time on pin $\overline{INT}$	from P port to $\overline{INT}$	-	1	-	1	us
t_{rstINT}	Reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	1	-	1	us
t_{vQ}	Data output valid time	from SCL to P port	-	400	-	400	ns
t_{suD}	Data input set-up time	from P port to SCL	0	-	0	-	ns
t_{hD}	Data input hold time	from P port to SCL	300	-	300	-	ns

Note*: Guaranteed by characterization. Not production tested.

Load Configuration

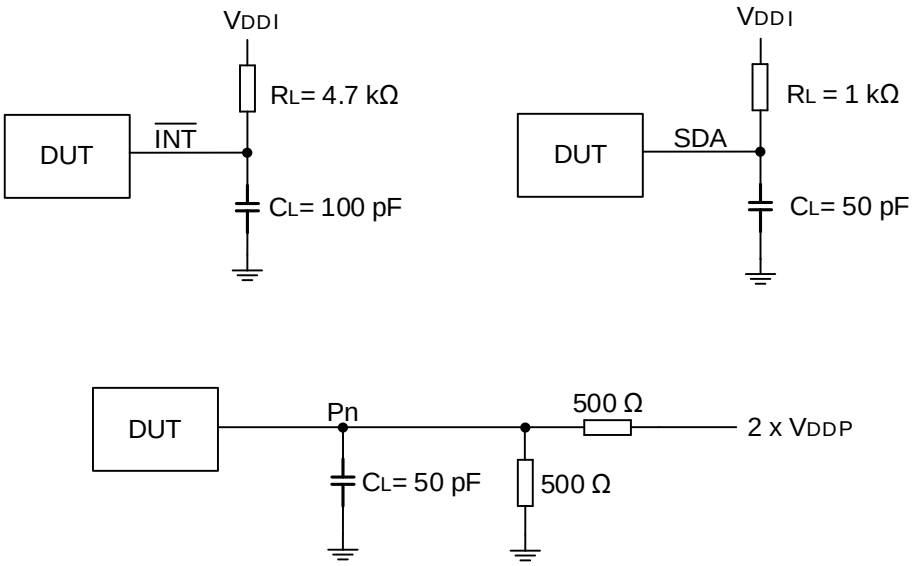


Figure 7. $\overline{INT}$、SDA、Port P load configuration

Note: C_L includes probe and clamp capacitance.

I²C Timing Waveform

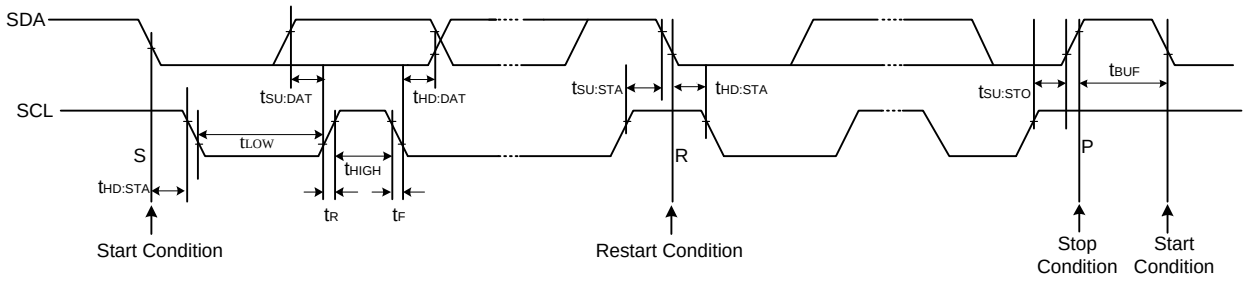


Figure 8. SDA Waveform

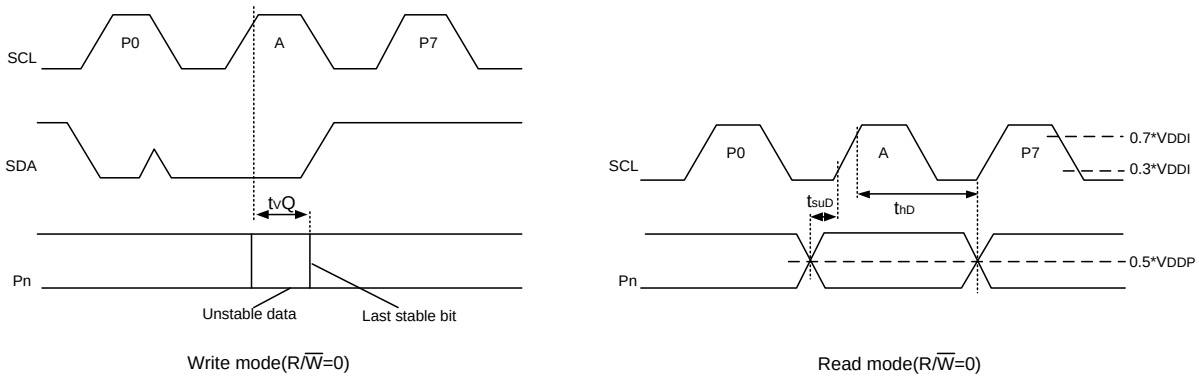


Figure 9. SDA Read/Write mode waveform

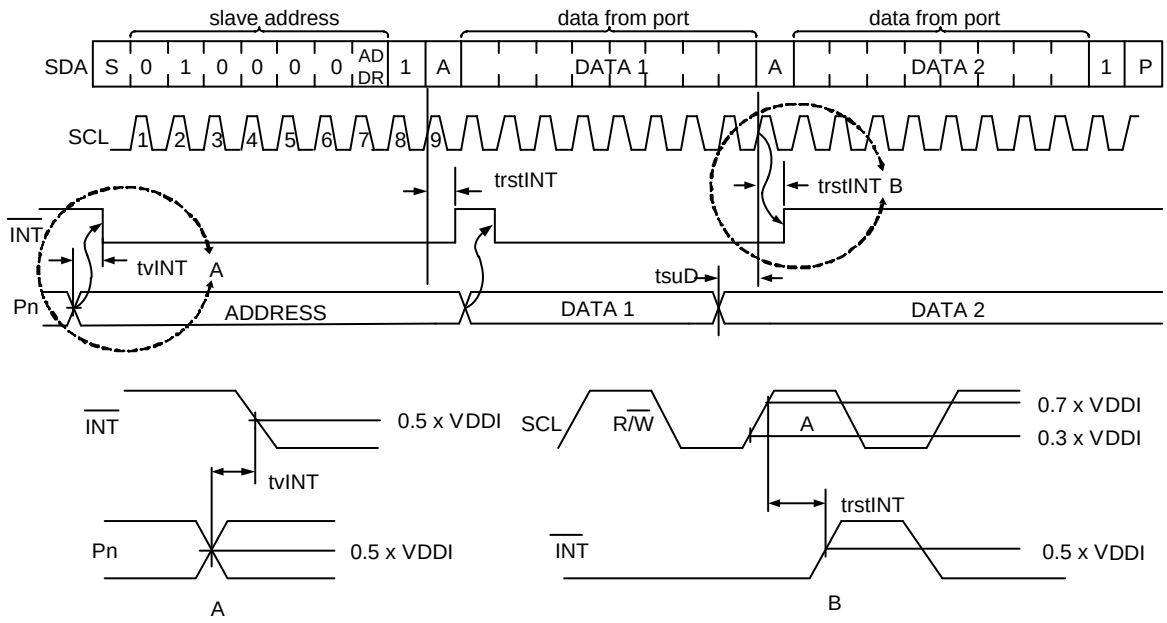


Figure 10. $\overline{\text{INT}}$、SDA、Port P waveform

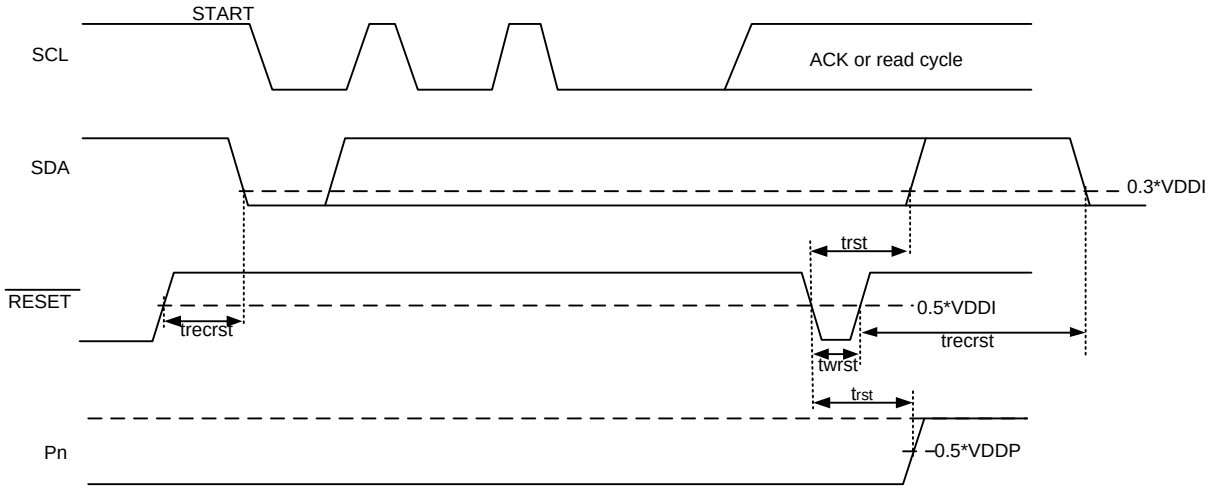


Figure 11. $\overline{\text{RESET}}$ waveform

Application Circuits

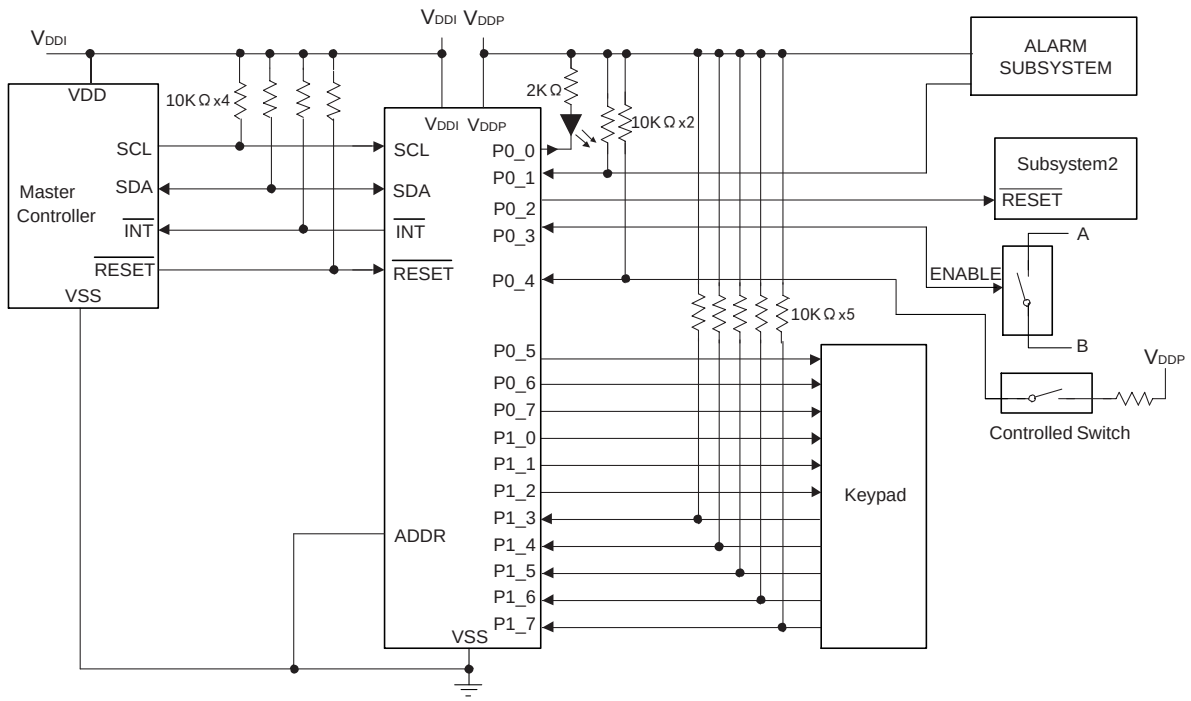


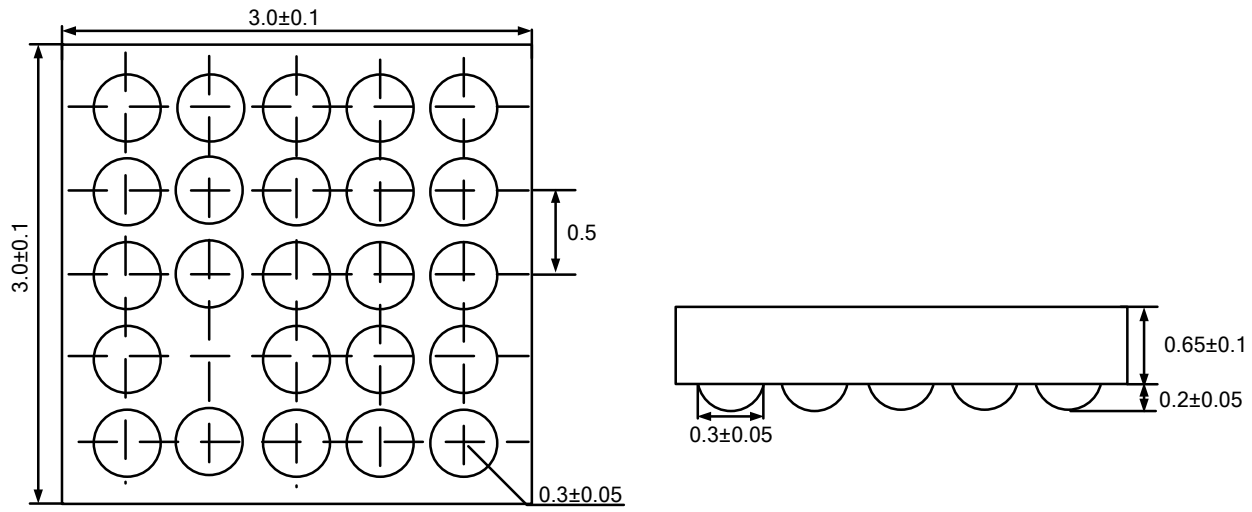
Figure 12. Application circuit

Note：(1) This application circuits is for reference only.

(2) When the P port is suspended, configure it to the output state please.

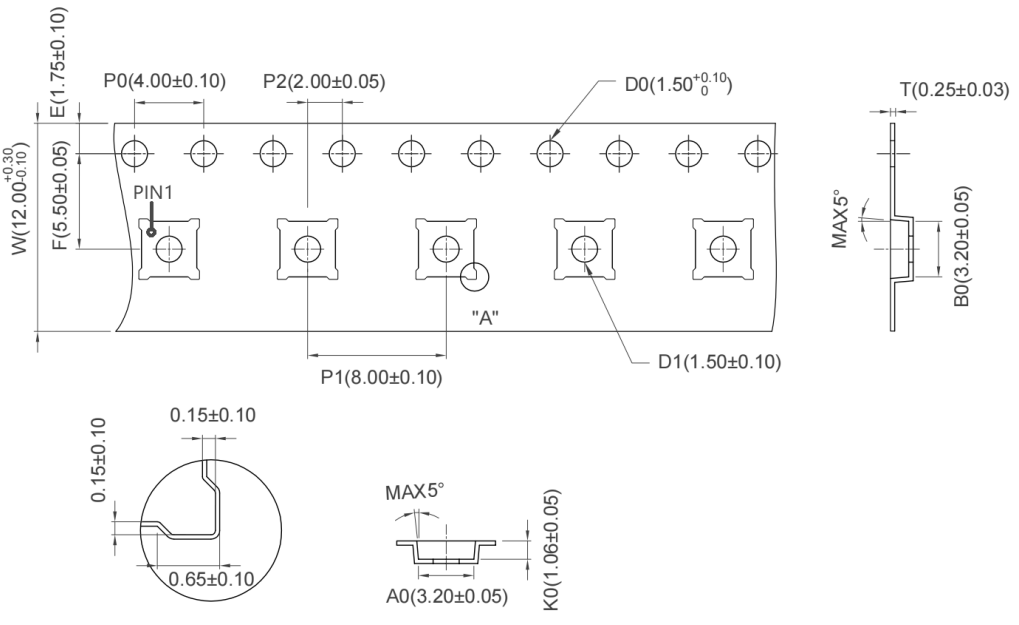
Package

VFBGA24



Unit: mm

Tape Information



Unit: mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0	2020-03-19	Preliminary Version	Shilj	Shilj	Liujy
1.0	2020-05-15	Released Version	Shilj	Shilj	Liujy
1.1	2020-10-13	Add Marking	Shilj	Shilj	Liujy
1.2	2020-11-12	Update Package size of QFN24	Shilj	Shilj	Liujy
1.3	2021-8-12	Add note on page 6 and 15	Shilj	Shilj	Liujy
1.4	2022-5-27	Layout update	Shib	Shilj	Liujy
1.5	2023-1-22	Update Typeset	Shib	Shib	Liujy