800mA Dual-rail Very Low Dropout LDO

General Description

The ET554ADJY1B is a CMOS-based low-dropout, low-power linear regulators, offering 800mA with NMOS pass transistor and a separate bias supply voltage (VBIAS). The device provides very stable, accurate output voltage with low noise, high ripple rejection and low supply current suitable for space constrained, noise sensitive application. The ET554ADJY1B series consist of an accurate voltage-reference block, an error amplifier, a thermal-shutdown circuit, and a current limit circuit.

The ET554ADJY1B is available in the DFN6(1.2mm ×1.2mm) package.

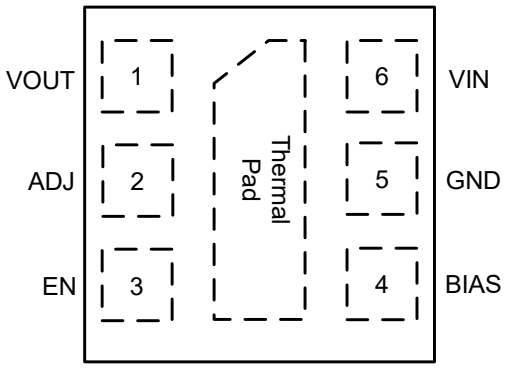
Features

- Wide V_{IN} Input Voltage Range: 1.0V to 5.5V
- Wide V_{BIAS} Voltage Range: 2.7V to 5.5V
- ADJ Output Voltage Range: 1.0V to 3.6V
- Very Low V_{BIAS} Input Current of Typ. 80μA
- Ultra Low Dropout: Typ. 220mV at 800mA, 1.2V Output, 2.8V Bias
- Built-in Over Current Protection and Thermal Shutdown Circuit
- Built-in Auto-discharging Circuit
- Built-in Under Voltage Lock-out
- Stable with a 2.2μF Ceramic Capacitor
- Package: DFN6 (1.2mm × 1.2mm)
- MSL: Level 1

Applications

- Constant-Voltage Power Supply for Battery-Powered Device
- Constant-Voltage Power Supply for Smartphones, Tablets
- Constant-Voltage Power Supply for Cameras, DVRs, STB and Camcorders

Pin Configuration

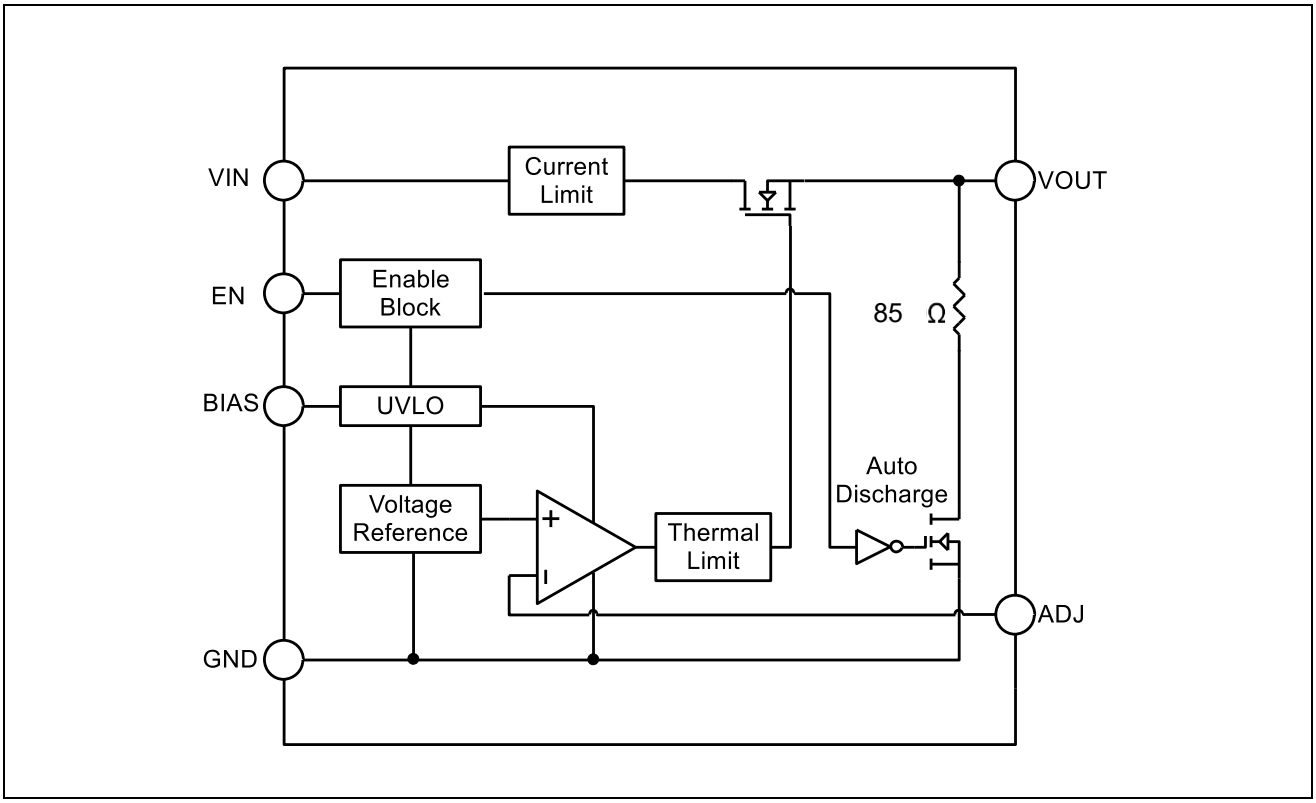


(Top View)

Pin Function

Symbol	Pin Name	Pin Description
VOUT	1	The power output of the device.
ADJ	2	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.
EN	3	Enable Input.
BIAS	4	Input voltage for controlling circuit.
GND	5	Ground pin.
VIN	6	Input voltage Pin. Large bulk capacitance should be placed closely to this pin. A 1μF ceramic capacitor is recommended at this pin.
TP		Thermal pad, connect to GND

Block Diagram



Functional Description

The ET554ADJY1B dual−rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability. V_{IN} to V_{OUT} operating voltage difference can be very low compared with standard PMOS regulators in very low V_{IN} applications.

The ET554ADJY1B offers smooth monotonic start-up.

Input and output Capacitor

The device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 2.2μF to 4.7μF. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range. In applications where no low input supplies impedance available (PCB inductance in VIN and/or VBIAS inputs as example), the recommended C_{IN} = 1uF and C_{BIAS}= 0.1uF or greater.

Enable Pin Operation

The ET554ADJY1B is turned on by setting the EN pin to “H”. The threshold limits are covered in the electrical characteristics table in this datasheet. When the EN pin is not used, connect the EN pin with VBIAS to keep the LDO in operating mode.

Current Limit Protection

When output current of VOUT pin is higher than current limit threshold or the VOUT pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool down. When the junction temperature reduces to approximately +145°C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Auto Discharging

When the EN pin set to “L”, the output circuit will be disable immediately, and the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of V_{OUT} in very short time. The Auto-Discharging function is optional.

Output Voltage Adjust

The required output voltage of Adjustable devices can be adjusted from 1.0V to 3.6 V using two external resistors. Typical application schematics is shown blow.

$$\mathbf{V_{OUT} = V_{REF} \times (1+R1/R2)}$$

Typical value of V_{REF} is 0.8V. It is recommended to keep the total serial resistance of resistors (R1+R2) not greater than 100KΩ.

The output voltage needs to take into account the error caused by the resistance accuracy.

Absolute Maximum Ratings

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage(VIN Pin)	-0.3 to 6.0	V
V_{BIAS}	Input Voltage (VBIAS Pin)	-0.3 to 6.0	V
V_{EN}	Input Voltage (EN Pin)	-0.3 to 6.0	V
V_{BIAS}	Input Voltage (ADJ Pin)	-0.3 to 6.0	V
V_{OUT}	Output Voltage	-0.3 to 6.0	V
I_{OUT_MAX}	Maximum Load Current	800	mA
$PD_{\_MAX}$	Maximum Power Consumption	640	mW
T_{STG}	Storage Temperature Range	-65 to +150	ºC
T_J	Operating Junction Temperature	-40 to +150	ºC
V_{ESD}	Human Body Model (JESD22-A114)	±3000	V
	Charged Device Model (JESD22-C101)	±1500	V
I_{LU}	Latch up Current Maximum Rating (JESD78E)	±200	mA

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	IN Input Voltage	V_{OUT}+ V_{DROP} to 5.5	V
V_{OUT}	Output Voltage	1.0 to 3.6	V
V_{BIAS}	BIAS Input Voltage	2.7 to 5.5 & V_{BIAS}>=V_{OUT}+1.4V	V
I_{OUT}	Output Current	0 to 800	mA
T_A	Operating Ambient Temperature	-40 to +85	ºC
C_{IN}	Effective Input Ceramic Capacitor Value	0.47 to 10	µF
C_{BIAS}	Effective Input Ceramic Capacitor Value	0.047 to 4.7	µF
C_{OUT}	Effective Output Ceramic Capacitor Value	1 to 10	µF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

Electrical Characteristics

(Unless otherwise noted, V_{IN}= V_{OUT}+0.3V, V_{BIAS}= 2.7V or V_{OUT}+1.6V whichever is greater, I_{OUT}=1mA, C_{IN}=1μF, C_{OUT}= 2.2μF, C_{BIAS} = 0.1uF, T_A = -40ºC ~ 85ºC.Typical values are at T_A = 25ºC)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}(1)	Input Voltage Range	V_{IN} > V_{OUT}	V_{OUT}+ V_{DROP}		5.5	V
V_{BIAS}	V_{BIAS} Voltage Range	V_{BIAS} > V_{OUT}+1.4V	2.7		5.5	V
V_{UVLO}	Under-Voltage Lock-Out	V_{BIAS} Rising	1.9	2.1	2.4	V
V_{UVLO_HYS}		Hysteresis	0.10	0.25	0.40	
I_{Q_ON}(2)	V_{BIAS} Current	Active mode: V_{EN}=V_{BIAS}	55	80	110	μA
I_{Q_OFF}		V_{EN}=0V		0.15	1	μA
V_{ADJ}(3)	V_{ADJ} Voltage	I_{OUT}=1mA~0.8A, T_A=25ºC	784		816	mV
		I_{OUT}=1mA~0.5A, T_A=-40ºC~85ºC	784		816	mV
		I_{OUT}=1mA~0.8A, T_A=-40ºC~85ºC	780		820	mV
V_{DROP}(4)	Dropout Voltage	I_{OUT}=0.5A, V_{OUT}=1.2V, V_{BIAS}=2.8V		125	200	mV
		I_{OUT}=0.8A, V_{OUT}=1.2V, V_{BIAS}=2.8V		220	350	
		I_{OUT}=0.5A, V_{OUT}=1.8V, V_{BIAS}=3.2V		145	220	
I_{LIM}	Limit Current		800	1450	1800	mA
I_{SC}	Short Current		30	130	250	mA
Reg_{LOAD}	Load Regulation	V_{BIAS}=2.7V or V_{OUT}+1.6V, whichever is greater, 1mA ≤ I_{OUT} ≤ 800mA		2	20	mV
Reg_{LINE}	V_{IN} Line Regulation	V_{OUT}+0.3V ≤ V_{IN}≤ 5 V (V_{BIAS} = V_{OUT} +1.6V, I_{OUT}=1mA)		0.01	0.1	%/V
	V_{BIAS} Line Regulation	2.7V or V_{OUT} + 1.4V, whichever is greater < V_{BIAS} < 5.5 V (V_{IN} = V_{OUT} + 0.3V, I_{OUT}=1mA)		0.01	0.1	%/V
PSRR(5)	Ripple Rejection	V_{BIAS} = 2.7V or V_{OUT} + 1.6V, whichever is greater, V_{IN} to V_{OUT}, f = 1kHz, Ripple 0.2Vp-p, V_{IN}=V_{OUT}+0.5V, I_{OUT} = 30mA	65	80		dB
		V_{BIAS} = 2.7V or V_{OUT} +1.6V, whichever is greater, V_{BIAS} to V_{OUT}, f = 1kHz, Ripple 0.2Vp-p, V_{IN}=V_{OUT}+0.5V, I_{OUT} = 30mA	65	80		
e_N(5)	Output Noise	V_{IN} = V_{OUT}+0.5V, f= 10 Hz to 100 kHz	30× V_{OUT}	45× V_{OUT}	65× V_{OUT}	μV_{RMS}
I_{EN}	EN Pull-down Current	V_{EN}=5.5V, V_{BIAS}=5.5V		0.2	1	μA
V_{ENH}	EN Input Voltage High		0.9		5.5	V

Electrical Characteristics(Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{ENL}	EN Input Voltage Low		0.0		0.4	V
R_{DIS}	Output Resistance of Auto Discharge at Off State	V_{BIAS}=3.8V, V_{IN}=5.5V, V_{EN}=0V, I_{OUT} =10mA	40	85	150	Ω
V_{TRLN}(5)	Line Transient	V_{IN}= V_{OUT}+0.3V to 5.5V in 10us, V_{BIAS} = V_{OUT}+1.6V, V_{OUT}=1.2V, I_{OUT}=1mA, T_A=25ºC		5	30	mV
		V_{IN}=5.5V to V_{OUT}+0.3V in 10us, V_{BIAS} = V_{OUT}+1.6V, V_{OUT}=1.2V, I_{OUT}=1mA, T_A=25ºC		5	30	mV
V_{TRLD}(5)	Load Transient	I_{OUT}=1mA to 500mA in 10us V_{OUT}=1.2V, V_{IN} = V_{OUT}+0.5V, V_{BIAS} = 2.7V or V_{OUT}+1.6V, whichever is greater, T_A=25ºC		50	120	mV
		I_{OUT}=500mA to 1mA in 10us V_{OUT}=1.2V, V_{IN} = V_{OUT}+0.5V, V_{BIAS} = 2.7V or V_{OUT}+1.6V, whichever is greater, T_A=25ºC		80	150	mV
T_{ON}	Turn-On Time	From Assertion of V_{EN} to V_{OUT}=98%$V_{OUT(NOM)}$	70	130	210	μs
T_{TSD}(5)	Thermal Shutdown Temperature	Temperature increasing	145	160	175	ºC
T_{TSR}(5)	Thermal Shutdown Released Temperature	Temperature decreasing	120	135	150	ºC

Notes 1: The maximum input voltage should take into account the maximum power consumption ($P_{D(MAX)}$).

The calculation formula is as follows:

$$\mathbf{P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT}}$$

The maximum power consumption of the circuit is 640mW.

$$\mathbf{V_{IN(MAX)} = 640mW / I_{OUT} + V_{OUT}}$$

For example:

If V_{OUT}= 1.2V, I_{OUT}=800mA, the maximum input voltage is $V_{IN(MAX)}$=640mW / 800mA+1.2=2.0V

If I_{OUT} >500mA, V_{BIAS} should be bigger than V_{OUT}+1.6V.

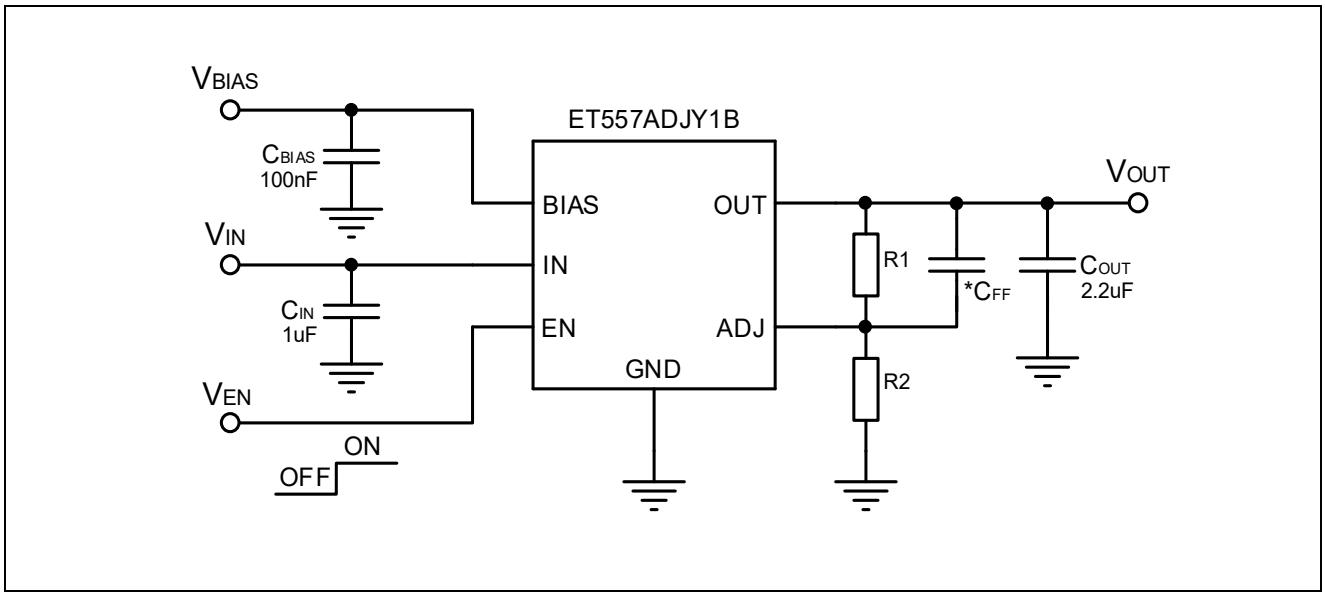
Notes 2: Since the power on process of BIAS needs a large current, the BIAS input voltage should have a current driving capacity of more than 10mA.

Notes 3: V_{ADJ} is the conversion value when $V_{OUT-SET}$=1V. V_{ADJ}=$V_{OUT-SET}$ /(1+R1/R2). The ratio of R1/R2=0.250 is accurate to the third decimal place.

Notes 4: V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET} +$V_{DROPMAX}$ with output current.

Notes 5: Guaranteed by design and characterization. not a FT item.

Application Circuits

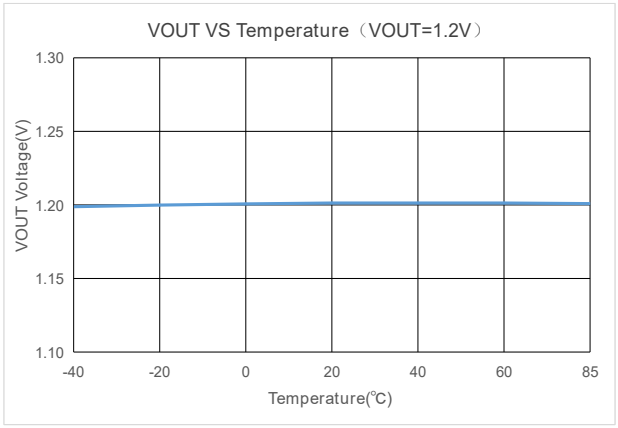


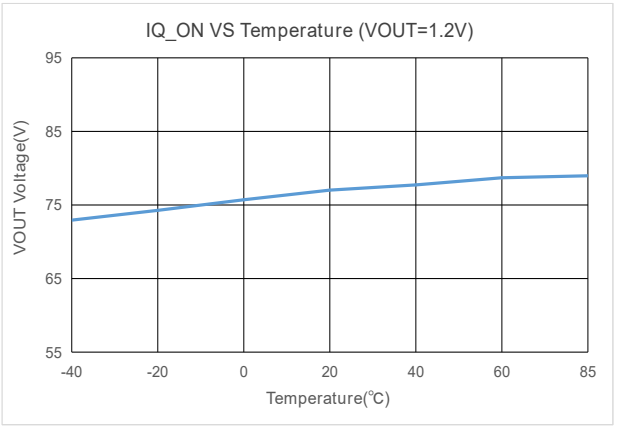
Notes 6: Adjust Version: V_{OUT} = 0.8×(1+R1/R2), (R1+R2) no greater than 100kΩ.

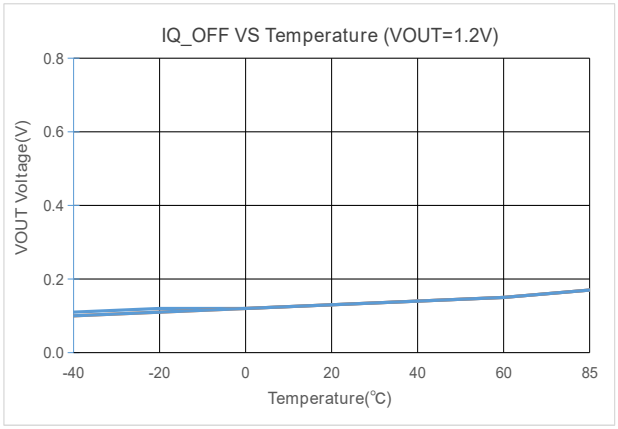
Notes 7: The feedforward capacitor C_{FF} is optional for the optimization of transient response.

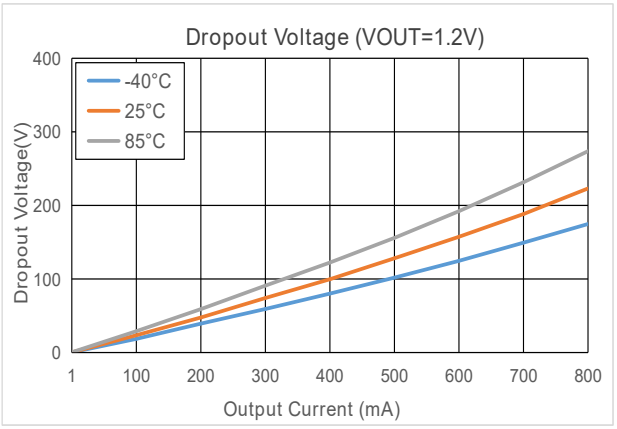
Typical Characteristics

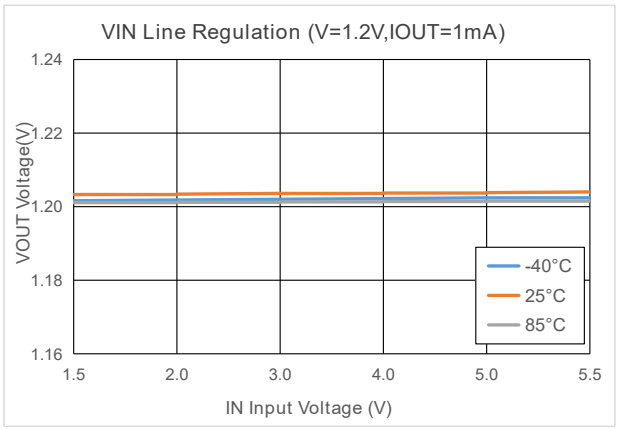
(V_{OUT}=1.2V, V_{IN}=V_{OUT}+0.3V, V_{BIAS}=V_{OUT}+1.6V, C_{IN}=1μF, C_{OUT}=2.2μF, C_{BIAS}=1uF, T_A= -40ºC~+85ºC)

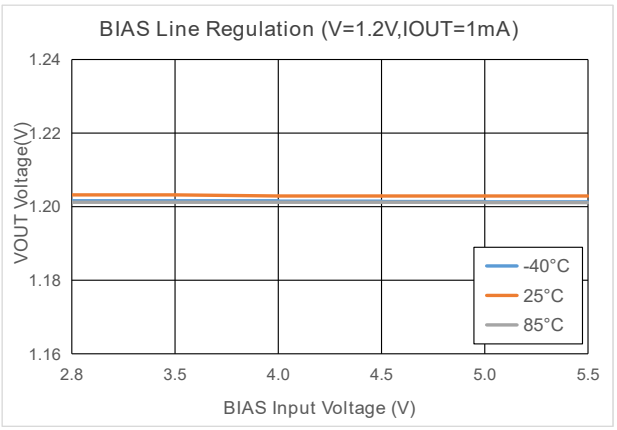






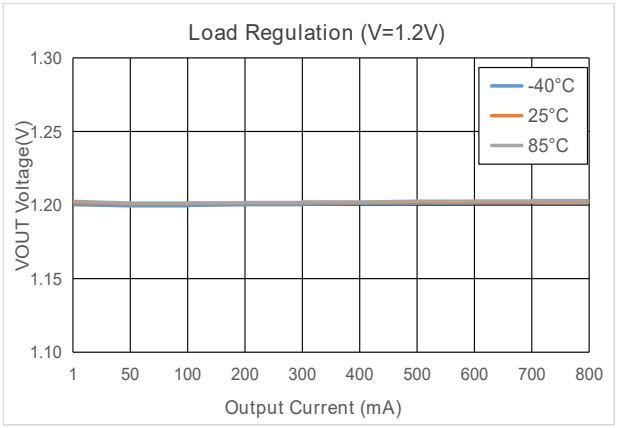


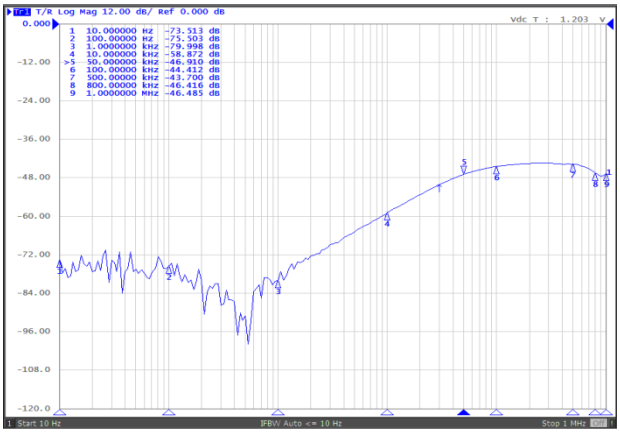


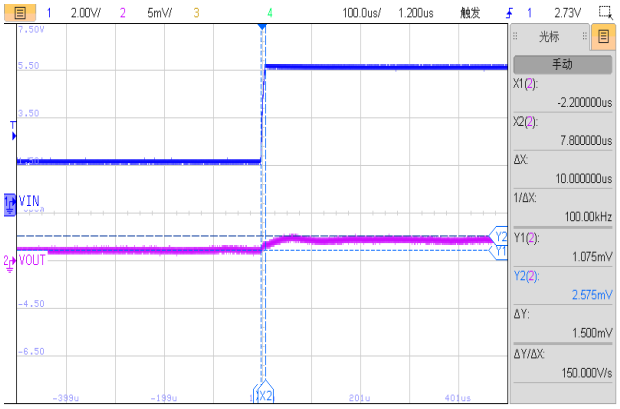


Typical Characteristics(Continued)

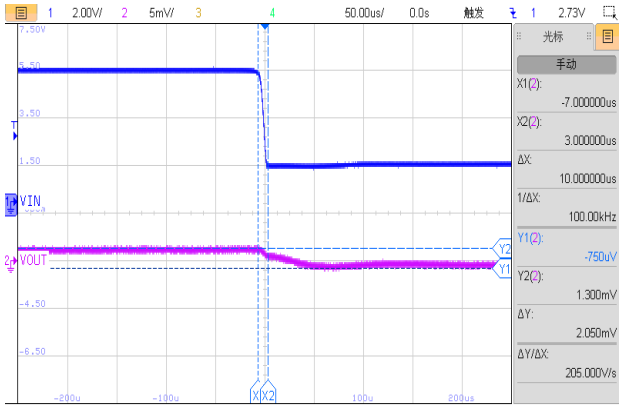
(V_{OUT}=1.20V, V_{IN}=V_{OUT}+0.3V, V_{BIAS}=V_{OUT}+1.6V, C_{IN}=1μF, C_{OUT}=2.2μF, C_{BIAS}=1uF, T_A= -40ºC~+85ºC)



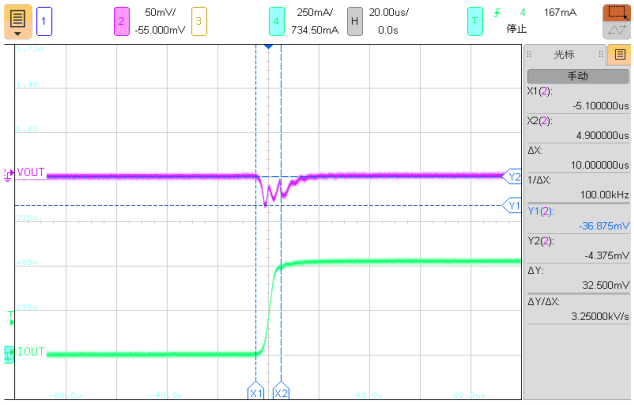




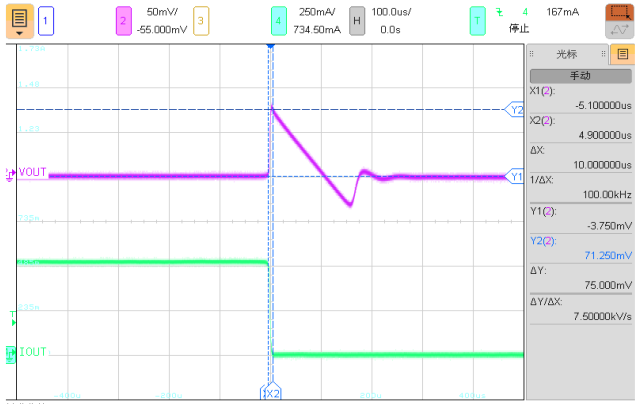
Input Transient(V_{IN}=1.5~5.5V tr=10us I_{OUT}=1mA)



Input Transient(V_{IN}=5.5~1.5V tf=10us I_{OUT}=1mA)



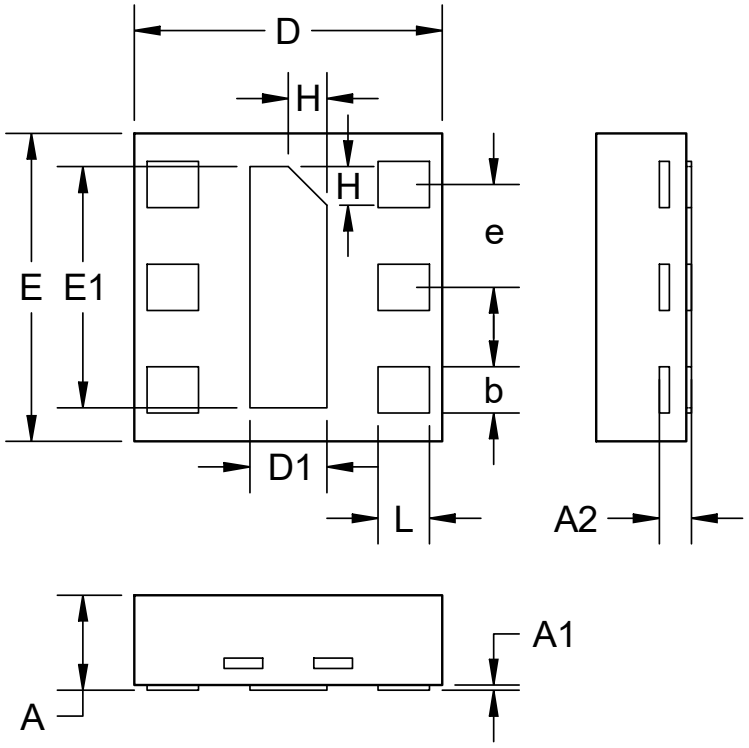
Load Transient(V_{IN}=1.5 VI_{OUT}=1mA~0.5A tr=10us)



Load Transient(V_{IN}=1.5 I_{OUT}=0.5A~1mA tf=10us)

Package Dimension

DFN6(1)

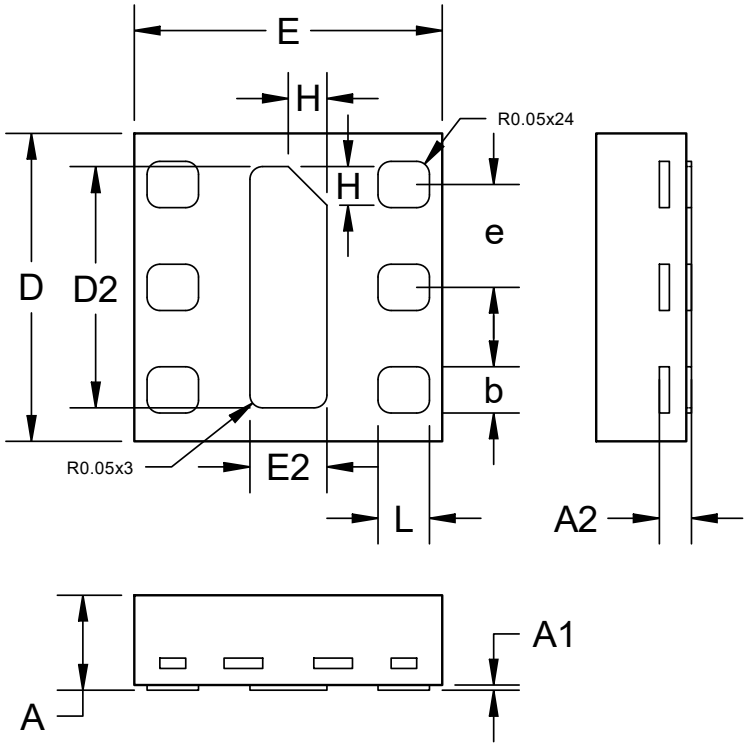


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.34	0.37	0.42
A1	0.00	0.02	0.05
A2		0.10REF	
b	0.13	0.18	0.23
D	1.10	1.20	1.30
E	1.10	1.20	1.30
D1	0.25	0.30	0.35
E1	0.89	0.94	0.99
e	0.30	0.40	0.50
H		0.15REF	
L	0.15	0.20	0.25

DFN6(2)

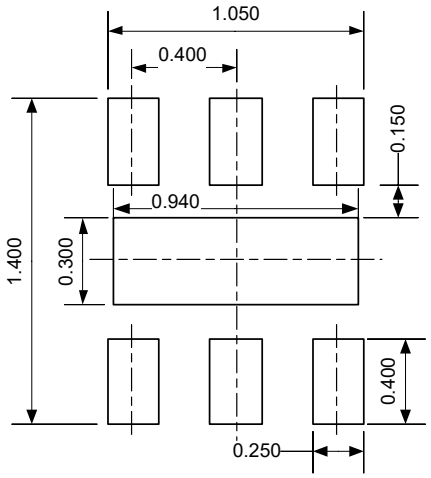


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

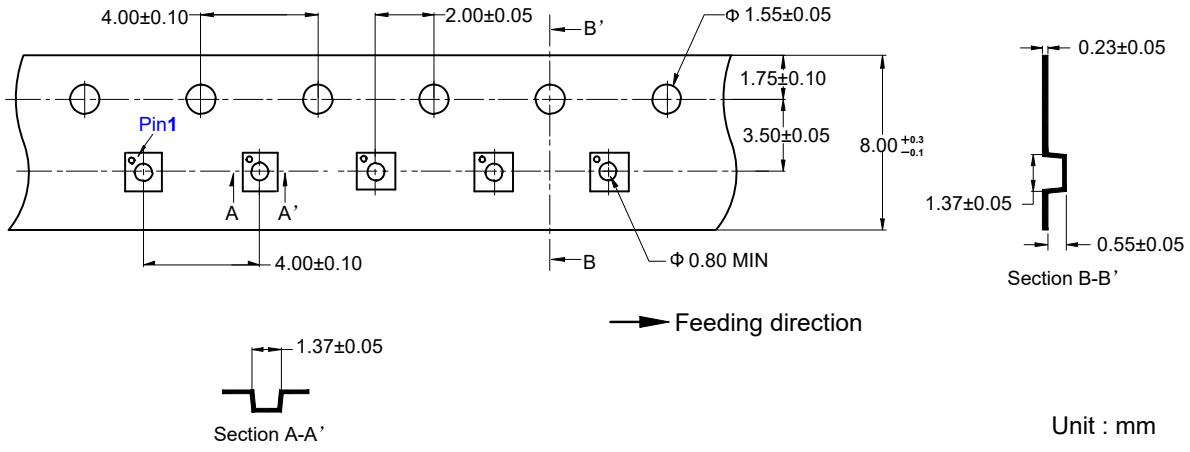
SYMBOL	MIN	NOM	MAX
A	0.30	0.35	0.42
A1	0.00	0.02	0.05
A2		0.125REF	
D	1.15	1.20	1.25
E	1.15	1.20	1.25
b	0.13	0.18	0.23
L	0.15	0.20	0.25
D2	0.89	0.94	0.99
E2	0.25	0.30	0.35
e		0.40 BSC	
H		0.15 REF	

Recommend PCB Layout



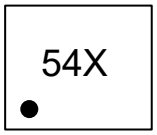
Unit : mm

Reel



Unit : mm

Marking Information



54 - Part Number

X - Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2023-08-22	Initial Version	Yangxx	Liuyg	Liujy
0.1	2023-11-02	Add New Package Information	Tugz	Liuyg	Liujy
0.2	2023-11-15	Update Package Information	Tugz	Liuyg	Liujy
1.0	2024-06-15	Official Version	Tugz	Liuyg	Liujy