ET51200M - Sink and Source DDR Termination Regulator

General Description

The ET51200M device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration.

The ET51200M maintains a fast-transient response and requires a minimum output capacitance of only 20μF. The ET51200M supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4 VTT bus termination.

The ET51200M is available in the thermally efficient ESOP8 thermal pad package, and is rated both Green and Pb-free. It is specified from -40°C to +85°C.

Features

- Input Voltage: Supports 2.5V Rail and 3.3V Rail
- VIN Voltage Range: 1.1V to 3.5V
- Sink and Source Termination Regulator Includes Droop Compensation
- (Typically 3×10uF MLCCs) for Memory Termination Applications (DDR)
- EN Input Control
- VREF Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider
- Built-in Soft Start, UVLO, and OCL
- Thermal Shutdown
- Supports DDR, DDR2, DDR3, DDR3L, Low Power DDR3, and DDR4 VTT Applications

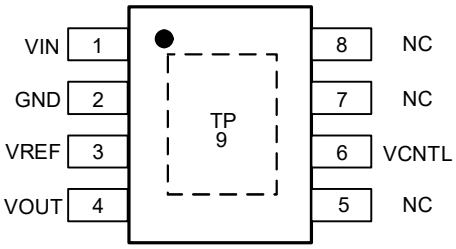
Device Information

Part No.	Package	Packing Option	MSL
ET51200M	ESOP8	Tape and Reel, 4K/Reel	Level 3

Applications

- Memory Termination Regulator for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4
- Notebooks, Desktops, and Servers
- Telecom and Datacom
- Base Stations
- LCD-TVs and PDP-TVs

Pin Configuration

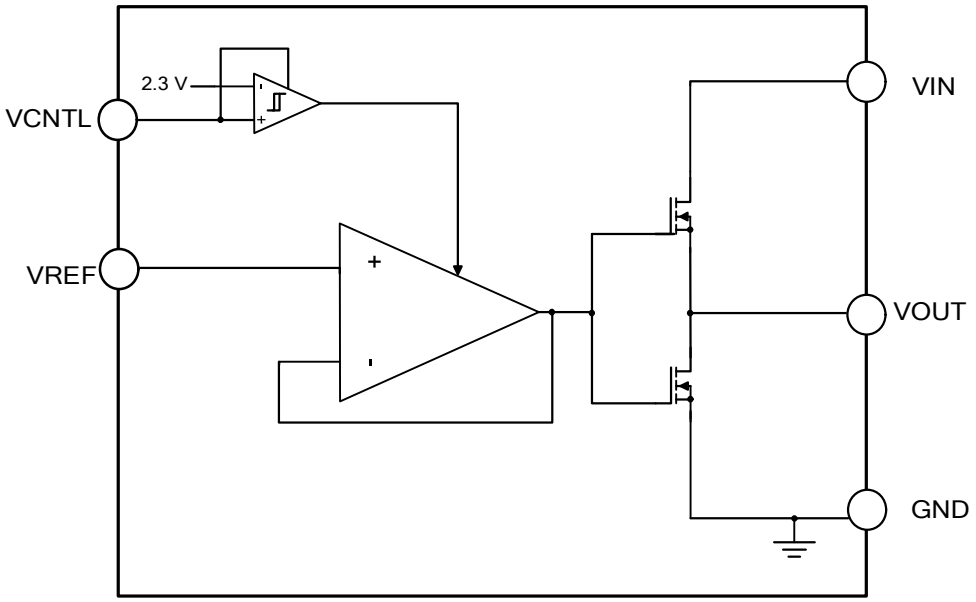


ET51200M(ESOP8)
Top View

Pin Function

Pin No.	Pin Name	Pin Description
1	VIN	Supply Voltage for the LDO.
2	GND	Power and Signal Ground.
3	VREF	Reference Input.
4	VOUT	Power Output for the LDO.
5,7,8	NC	No Internal Connection.
6	VCNTL	2.5V or 3.3V Power Supply. A ceramic decoupling capacitor with a value between 1μF and 4.7μF is required.
9	TP	Thermal Pad, Connect to GND or Floating

Block Diagram



Functional Description

Overview

The ET51200M device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration.

The device maintains a fast-transient response and only requires a minimum output capacitance of 20µF. The device supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low Power DDR3, and DDR4 VTT bus termination.

VCNTL Input Capacitor

Add a ceramic capacitor, with a value between 1.0µF and 4.7µF, placed close to the VCNTL pin, to stabilize the bias supply (2.5V rail or 3.3V rail) from any parasitic impedance from the supply.

VIN Input Capacitor

Depending on the trace impedance between the VIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VIN input capacitor. Use a 10µF (or greater) ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at the VOUT pin. In general, use one-half of the C_{VOUT} value for input.

Output Capacitor

For stable operation, the total capacitance of the VOUT output pin must be greater than 20µF. Attach three, 10µF ceramic capacitors in parallel to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL). The RC filter time constant should be almost the same as or slightly lower than the time constant of the output capacitor and its ESR.

Sink and Source Regulator (VOUT Pin)

The ET51200M is a sink and source tracking termination regulator specifically designed for low input voltage, low-cost, and low external component count systems where space is a key application parameter. The device integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response.

Reference (VREF Pin)

The output voltage, VOUT, is regulated to VREF. When VREF is configured for standard DDR termination applications, VREF can be set by an external equivalent ratio voltage divider connected to the memory supply bus (VDDQ). The ET51200M device supports VREF voltages from 0.5V to 1.8V, making it versatile and ideal for many types of low-power LDO applications. VOUT becomes active when VREF voltage rises to 0.390V and VIN is above the UVLO threshold.

Internal and External Soft-Start

The ET51200M is designed with an internal soft-start function to control the rise rate of the output voltage to prevent inrush current during start-up. When release the pull-low transistor connected with VREF pin, the current via the resistor divider charges the external soft-start capacitor and the VREF starts to rise up. The IC starts a soft-start process when the VREF reaches the enable voltage threshold. The output voltage is regulated to follow the lower voltage, which is either the internal soft-start voltage ramp or the VREF voltage, to rise up. The external soft-start interval is programmable by the resistor-divider and the soft-start capacitor.

Current Protection (VOUT Pin)

The ET51200M monitors the output current, both sourcing and sinking current, and limits the maximum output current to prevent damages during current overload or shortcircuit (shorten from VOUT to GND or VIN) conditions.

UVLO Protection (VCNTL Pin)

For VCNTL under-voltage lockout (UVLO) protection, the ET51200M monitors VCNTL voltage. When the VCNTL voltage is lower than the UVLO threshold voltage, the VOUT regulators are powered off. This shutdown is a non-latch protection.

Thermal Shutdown

The ET51200M monitors junction temperature. If the device junction temperature exceeds the threshold value, (typically 150°C), the VOUT regulator shut off, discharged by the internal discharge MOSFETs. This shutdown is a non-latch protection.

Output Tolerance Consideration for VTT DIMM Applications

The ET51200M is specifically designed to power up the memory termination rail (as shown in Figure 1). The DDR memory termination structure determines the main characteristics of the VTT rail, which is to be able to sink and source current while maintaining acceptable VTT tolerance. See Figure 2 for typical characteristics for a single memory cell.

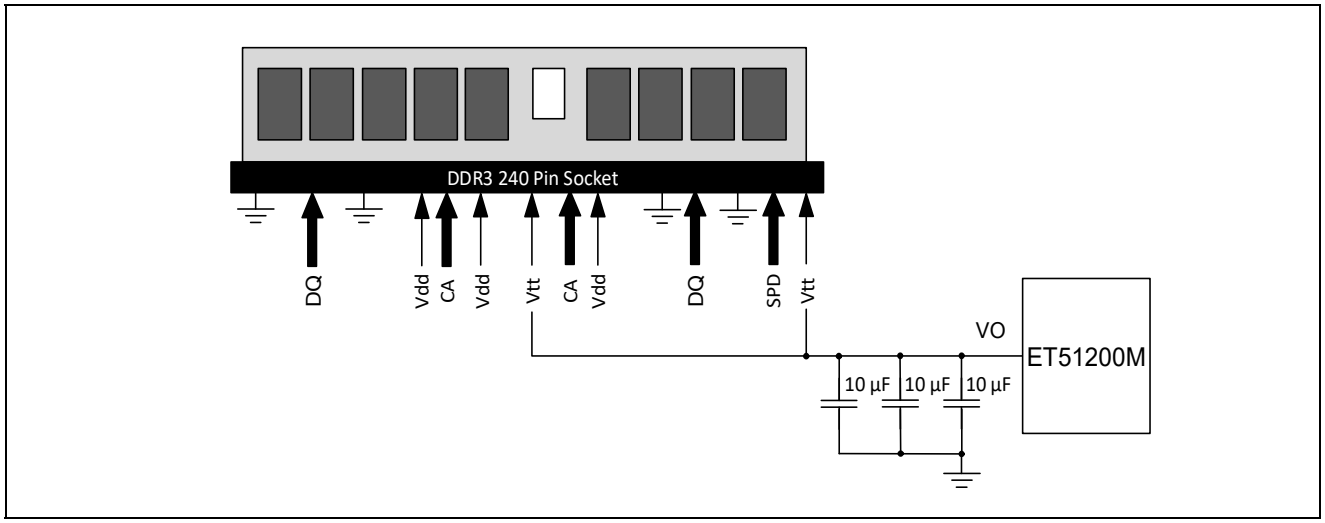


Figure 1. Typical Application Diagram for DDR3 VTT DIMM using ET51200M

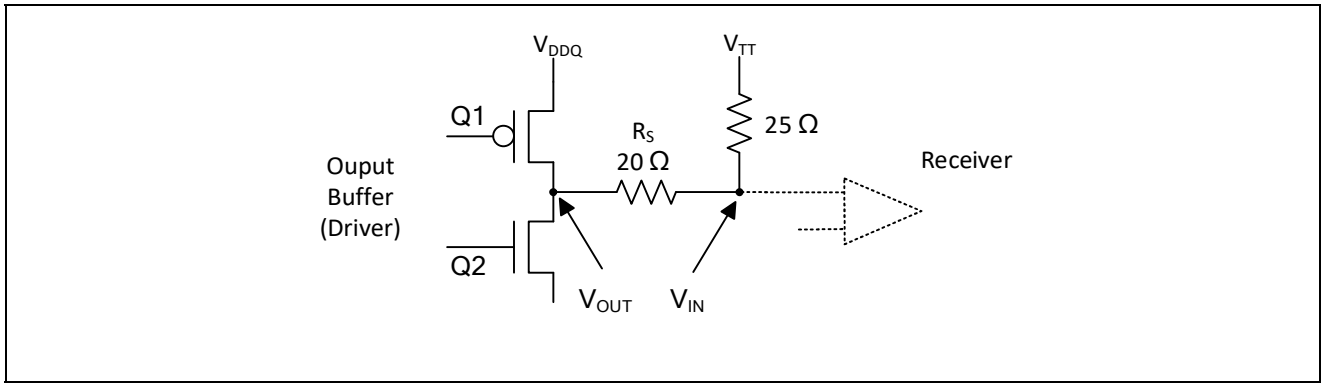


Figure 2. DDR Physical Signal System Bi-Directional SSTL Signaling

In Figure 2, when Q1 is on and Q2 is off:

• Current flows from VDDQ via the termination resistor to VTT

• VTT sinks current

In Figure 2, when Q2 is on and Q1 is off:

• Current flows from VTT via the termination resistor to GND

• VTT sources current

Because VTT accuracy has a direct impact on the memory signal integrity, it is imperative to understand the tolerance requirement on VTT. Equation 1 applies to both DC and AC conditions and is based on JEDEC VTT specifications for DDR and DDR2 (JEDEC standard: DDR JESD8-9B May 2002; DDR2 JESD8-15A Sept 2003).

$$V_{VTTREF} - 40\ mV < V_{VTT} < V_{VTTREF} + 40\ mV \quad (1)$$

The specification itself indicates that VTT must keep track of VTTREF for proper signal conditioning. The ET51200M ensures the regulator output voltage to be as shown in Equation 2, which applies to both DC and AC conditions.

$$V_{VTTREF} - 25\ mV < V_{VTT} < V_{VTTREF} + 25\ mV \quad (2)$$

where

$-2\ A < I_{VTT} < 2\ A$

The regulator output voltage is measured at the regulator side, not the load side. The tolerance is applicable to DDR, DDR2, DDR3, DDR3L, Low Power DDR3, and DDR4 applications (see Table 1 for detailed information). To meet the stability requirement, a minimum output capacitance of 20µF is needed. Considering the actual tolerance on the MLCC capacitors, three 10µF ceramic capacitors sufficiently meet the VTT accuracy requirement.

Table 1. DDR, DDR2, DDR3 and LP DDR3 Termination Technology

	DDR	DDR2	DDR3	LOW POWER DDR3
FSB Data Rates	200, 266, 333, and 400 MHz	400, 533, 677, and 800 MHz	800, 1066, 1330, and 1600 MHz	
Termination	Motherboard termination to VTT for all signals	On-die termination for data group. VTT termination for address, command and control signals	On-die termination for data group. VTT termination for address, command and control signals	
Termination Current Demand	Maximum source/sink transient currents of up to 2.6 A to 2.9 A	Not as demanding	Not as demanding	
		Only 34 signals (address, command, control) tied to VTT	Only 34 signals (address, command, control) tied to VTT	
		ODT handles data signals	ODT handles data signals	
		Less than 1A of burst current	Less than 1A of burst current	
Voltage Level	2.5V Core and I/O 1.25V VTT	1.8V Core and I/O 0.9V VTT	1.5V Core and I/O 0.75V VTT	1.2V Core and I/O 0.6V VTT

The ET51200M uses transconductance (g_M) to drive the LDO. The transconductance and output current of the device determine the voltage droop between the reference input and the output regulator. The typical transconductance level is 250 S at 2 A and changes with respect to the load in order to conserve the

quiescent current (that is, the transconductance is very low at no load condition). The (gM) LDO regulator is a single pole system. Only the output capacitance determines the unity gain bandwidth for the voltage loop, as a result of the bandwidth nature of the transconductance (see Equation 3).

$$f_{UGBW} = \frac{g_M}{2 \times \pi \times C_{OUT}} \quad (3)$$

where

- f_{UGBW} is the unity gain bandwidth
- g_M is transconductance
- C_{OUT} is the output capacitance

Consider these two limitations to this type of regulator that come from the output bulk capacitor requirement. In order to maintain stability, the zero location contributed by the ESR of the output capacitors must be greater than the -3dB point of the current loop. This constraint means that higher ESR capacitors should not be used in the design.

In addition, the impedance characteristics of the ceramic capacitor should be well understood in order to prevent the gain peaking effect around the transconductance (g_M) -3dB point because of the large ESL, the output capacitor and parasitic inductance of the VO pin voltage trace.

VREF Consideration for DDR2 Applications

During ET51200M tracking start-up, the VREFIN voltage follows the rise of the V_{DDQ} rail through a voltage divider, and VOUT follows VREF once the VREF voltage is greater than 0.39V. When the VREF voltage is lower than 0.39V, VOUT is 0V.

The JEDEC DDR2 SDRAM Standard (JESD79-2E) states that VREF must track VDDQ/2 within ±0.3V accuracy during the start-up period. To allow the ET51200M device to meet the JEDEC DDR2 specification, a resistor divider can be used to provide the VREF signal to the DIMM. The resistor divider ratio is 0.5 to ensure that the VREF voltage equals VDDQ/2.

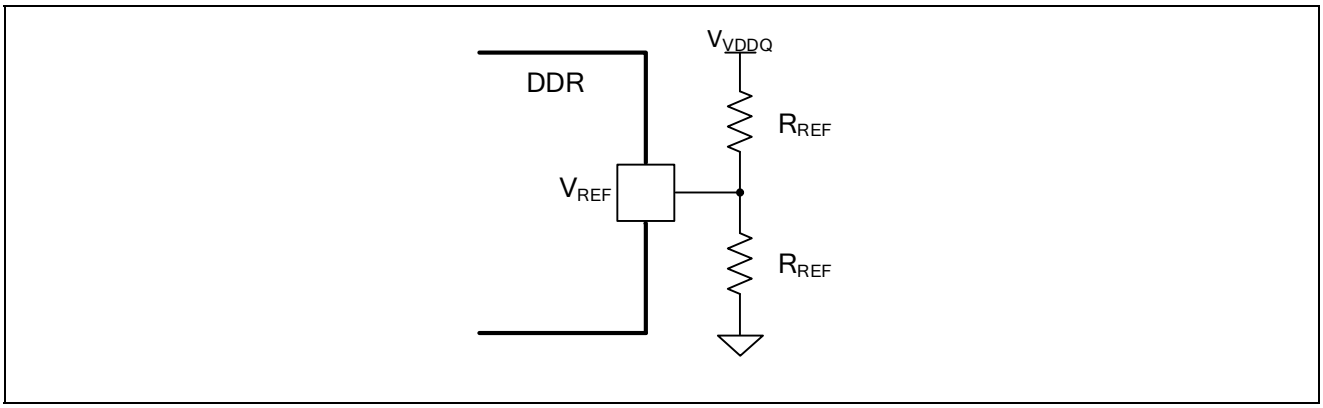


Figure 5. Resistor Divider Circuit

When selecting the resistor value, consider the impact of the leakage current from the DIMM VREF pin on the reference voltage. Use Equation 4 to calculate resistor values.

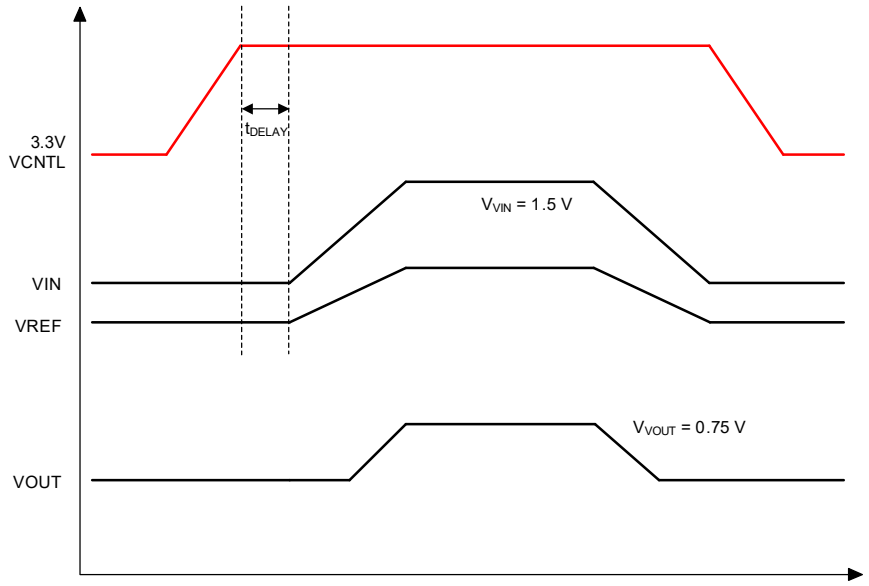
$$R_{REF} \leq \frac{2 \times \Delta V_{REF}}{I_{REF}} \quad (4)$$

where

- R_{REF} is the resistor value
- ΔV_{REF} is the VREF DC variation requirement
- I_{REF} is the maximum total VREF leakage current from DIMMs

Low Input Voltage Applications

ET51200M can be used in an application system that offers either a 2.5V rail or a 3.3V rail. The ET51200M device has a minimum input voltage requirement of 2.375V. If a 2.5V rail is used, ensure that the absolute minimum voltage (both DC and transient) at the device pin is be 2.375V or greater. The voltage tolerance for a 2.5V rail input is between ±5% accuracy, or better.



Note: It is recommended that after the VIN is powered on, wait until the internal logic is completely stable before starting the LDO. The t_{DELAY} time is suggested to be greater than 250ms.

Absolute Maximum Ratings

Symbol	Parameters (Items)	Value	Unit
V_{REF}	VREF Voltage	-0.3 to 3.6	V
V_{CTRL}	VCTRL Voltage	-0.3 to 6.0	V
V_{IN}	VIN Voltage	-0.3 to 3.6	V
V_{OUT}	VOUT Voltage	-0.3 to 3.6	V
T_J	Maximum Operating Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_L	Lead Temperature (Soldering, 10 sec)	300	°C
V_{ESD}	Human Body Model (JESD22-A114)	±2000	V
	Charged Device Model (JESD22-C101)	±500	

Thermal Characteristics

Symbol	Ratings	Value	Unit
$R_{\theta JA}$	Junction-to-Ambient thermal resistance	55	°C/W
$R_{\theta JC(TOP)}$	Junction-to-Case(TOP) thermal resistance	85	°C/W
$R_{\theta JB}$	Junction-to-Board thermal resistance	33	°C/W
P_D	Max power dissipation	1.8	W

Recommended Operating Conditions

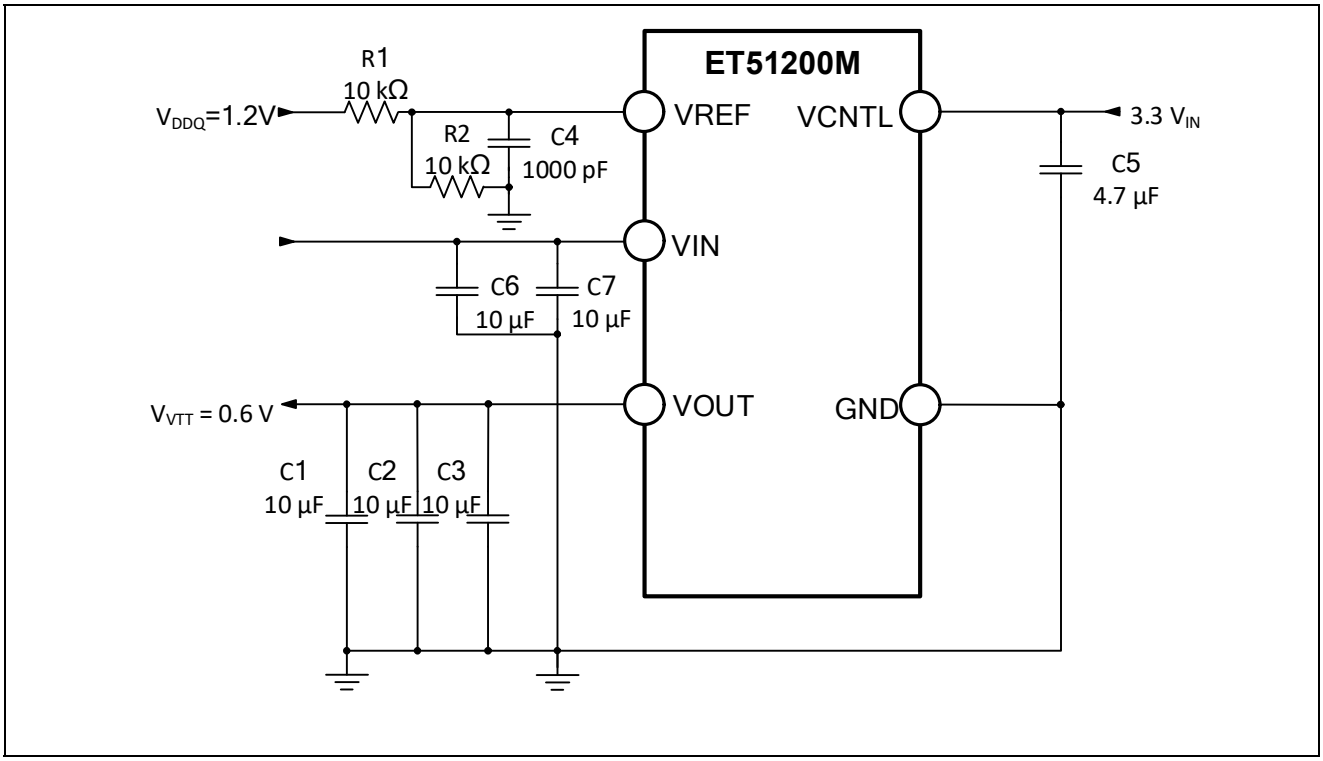
Symbol	Parameters	Rating	Unit
V_{CTRL}	VCTRL Voltage	2.375 to 5.5	V
V_{IN}	VIN Voltage	-0.1 to 3.5	V
V_{REF}	VREF Voltage	0.5 to1.8	V
V_O	VO Voltage	-0.1 to 3.5	V
T_A	Operating Free-air Temperature	-40 to 85	°C

Electrical Characteristics

Over recommended free-air temperature range, V_{CTRL} = 3.3V, V_{VIN} = 1.8V, V_{REF} = 0.9V, C_{OUT} = 3 × 10μF (unless otherwise noted) .

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{CNTL}	Input Voltage Operation Range		2.375		5.5	V
V_{VIN}	Power Supply Voltage Operation Range		1.1		3.5	V
SUPPLY CURRENT						
I_{CNTL}	Supply Current	T_A = 25°C, No Load	0.40	0.60	1.0	mA
I_{CNTL_SHDN}	Shutdown Current	T_A = 25°C, V_{REF} = 0V, No Load	35	55	80	μA
I_{IN}	Supply Current of VIN	T_A = 25°C, V_{REF} = 0.9V, No Load		1	50	μA
I_{IN_SHDN}	Shutdown Current of VIN	T_A = 25°C, V_{REF} = 0V, No Load		0.1	50	
INPUT CURRENT						
I_{REF}	Input Current, VREF				1	μA
VOUT OUTPUT						
V_{OUT}	Output DC Voltage, VOUT	V_{REFOUT} = 1.25V (DDR1), I_O = 0A	-15		15	mV
		V_{REFOUT} = 0.90V (DDR2), I_O = 0A	-15		15	mV
		V_{REFOUT} = 0.75V (DDR3), I_O = 0A	-15		15	mV
		V_{REFOUT} = 0.675V (DDR3L), I_O = 0A	-15		15	mV
		V_{REFOUT} = 0.6V (DDR4), I_O = 0A	-15		15	mV
V_{VOTOL}	Output Voltage Tolerance to VREF	-2A < I_{VO} < 2A	-70		70	mV
R_{DSCHRG}	Discharge Resistance, VOUT	V_{REF} = 0V, V_{VO} = 0.3V, T_A = 25°C	8	15	25	Ω
VREF						
V_{REF}	VREF Voltage Range		0.5		1.8	V
V_{REF_UVLO}	VREF Under-voltage Lockout	REF Rising	360	390	420	mV
V_{REF_HYS}	VREF Under-voltage Lockout Hysteresis		10	20	50	mV
UVLO AND EN LOGIC THRESHOLD						
V_{CNTL_UVLO}	UVLO Threshold	Wake Up, T_A = 25°C	2.100	2.300	2.375	V
V_{CNTL_HYS}	UVLO Hysteresis	Hysteresis		50		mV
THERMAL SHUTDOWN						
T_{TSD}	Thermal Shutdown Threshold	Shutdown Temperature		150		°C
T_{TSH}		Hysteresis		25		

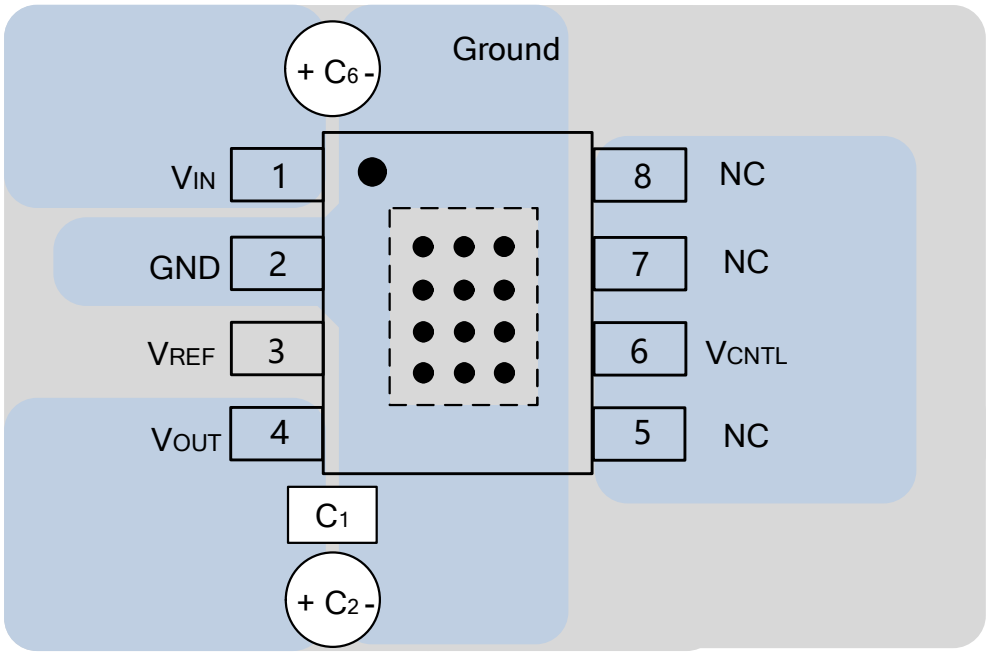
Application Circuits



*This design example describes a 3.3 VIN, DDR3 configuration.

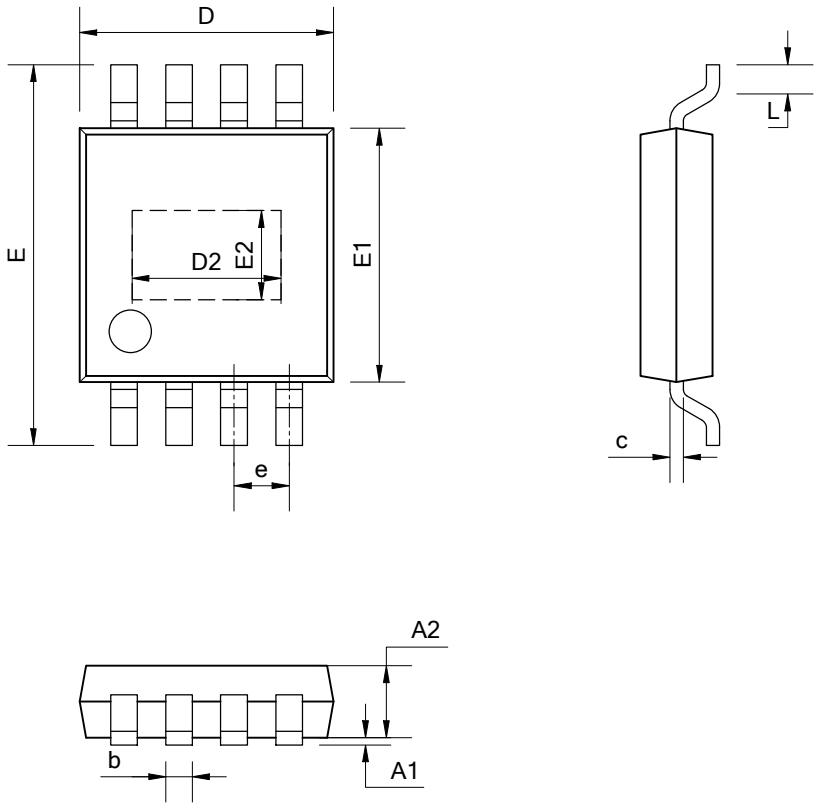
PCB Layout Guide

ESOP8(ET51200M)



Package Dimension

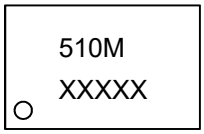
ESOP8



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A1	0.00	-	0.30
A2	1.20	1.40	1.60
b	0.35	-	0.47
c	0.15	-	0.27
D	4.70	4.90	5.10
E	5.80	6.00	6.20
D2	3.00	3.25	3.50
E1	3.70	3.90	4.10
E2	2.10	2.30	2.50
e	1.27 TYP		
L	0.35	0.60	0.85

Marking Information



510M - Part Number

XXXXX - Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2025-08-05	Preliminary Version	Marj	Yangxx	Liujy
1.0	2026-06-05	Offical Version	Marj	Yangxx	Liujy
1.0.a	2026-08-24	Update Packing Option Information	Yangxx	Yangxx	Liujy
1.0.b	2026-08-31	Update Load Regulation	Yangxx	Yangxx	Liujy
1.0.c	2026-10-26	Add Power-up Sequence	Yangxx	Yangxx	Liujy