ET51200 - Sink and Source DDR Termination Regulator

General Description

The ET51200 device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration.

The ET51200 maintains a fast-transient response and requires a minimum output capacitance of only 20μF. The ET51200 supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4 VTT bus termination.

In addition, the ET51200 provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.

The ET51200 is available in the thermally efficient DFN10 thermal pad package, and is rated both Green and Pb-free. It is specified from -40°C to +85°C.

Features

- Input Voltage: Supports 2.5V Rail and 3.3V Rail
- VLDOIN Voltage Range: 1.1V to 3.5V
- Sink and Source Termination Regulator Includes Droop Compensation
- (Typically 3 × 10uF MLCCs) for Memory Termination Applications (DDR)
- PGOOD to Monitor Output Regulation
- EN Input Control
- REFIN Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider
- Remote Sensing (VOSNS)
- ±10mA Buffered Reference (REFOUT)
- Built-in Soft Start, UVLO, and OCL
- Thermal Shutdown
- Supports DDR, DDR2, DDR3, DDR3L, Low Power DDR3, and DDR4 VTT Applications

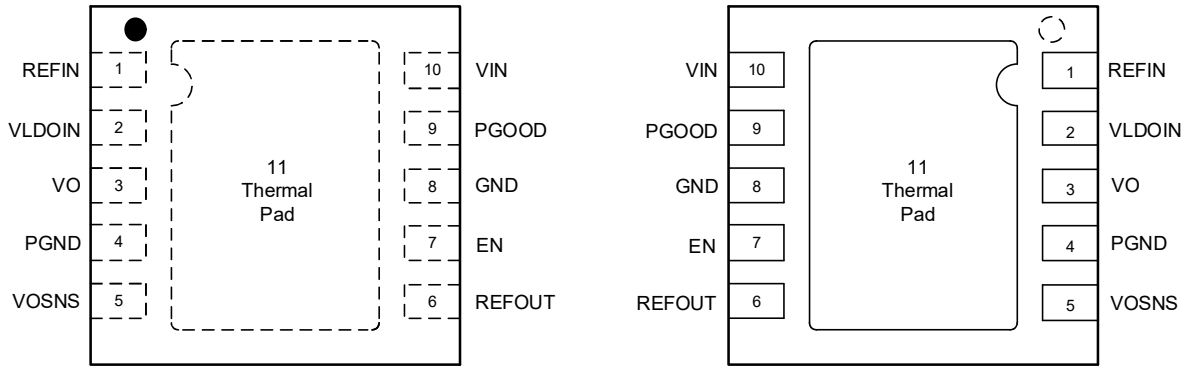
Device Information

Part No.	Package	MSL
ET51200	DFN10 (3mm×3mm)	Level 1

Applications

- Memory Termination Regulator for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4
- Notebooks, Desktops, and Servers
- Telecom and Datacom
- Base Stations
- LCD-TVs and PDP-TVs

Pin Configuration

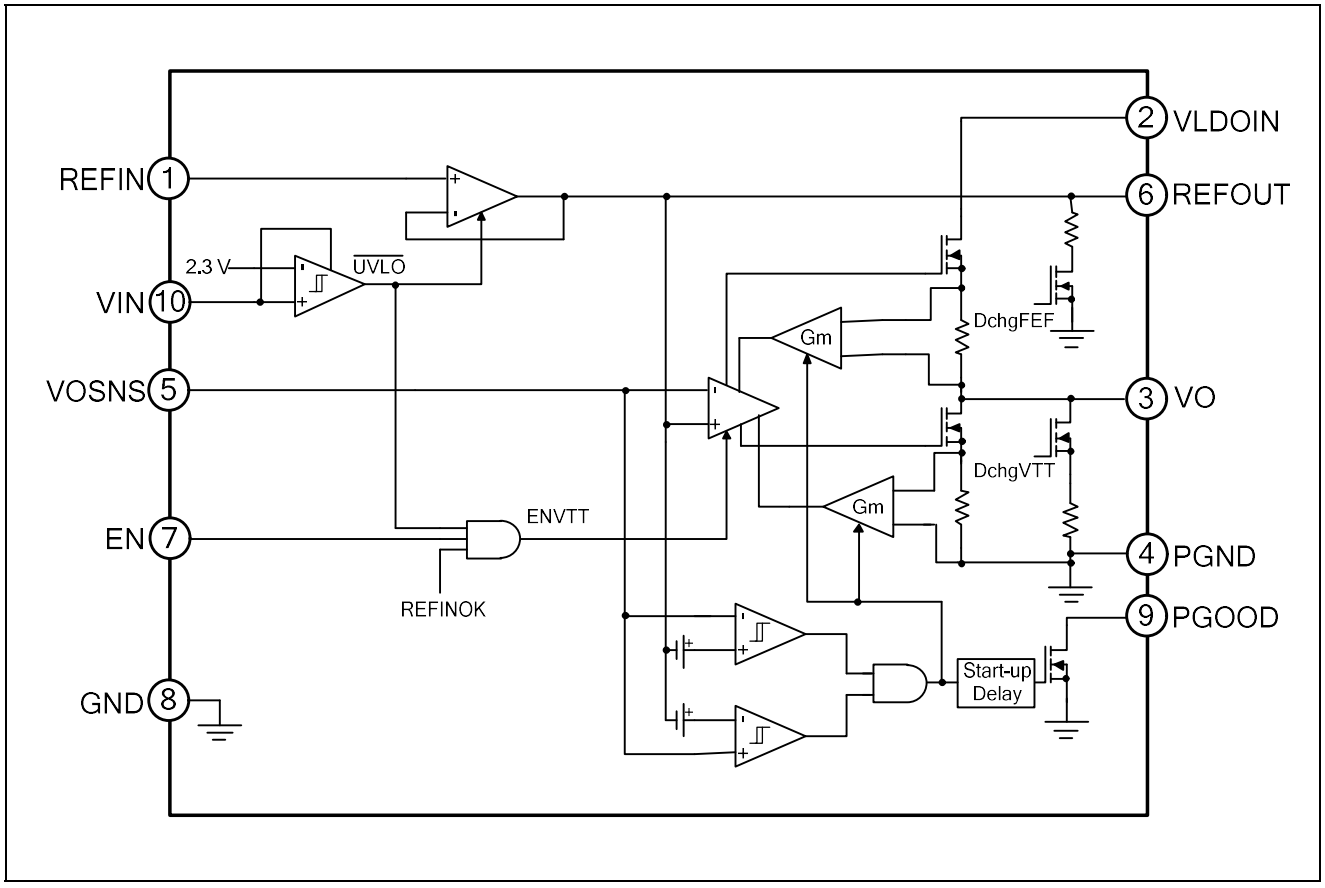


Top View Bottom View

Pin Function

Pin Name	Pin No.	Pin Description
REFIN	1	Reference input.
VLDOIN	2	Supply voltage for the LDO.
VO	3	Power output for the LDO.
PGND	4	Power ground for the LDO.
VOSNS	5	Voltage sense input for the LDO. Connect to positive terminal of the output capacitor or the load.
REFOUT	6	Reference output. Connect to GND through 0.1-μF ceramic capacitor. If there is a REFOUT capacitors at DDR side, keep total capacitance on REFOUT pin below 0.47μF. The REFOUT pin can not be open.
EN	7	For DDR VTT application, connect EN to SLP_S3. For any other application, use the EN pin as the ON/OFF function.
GND	8	Signal ground.
PGOOD	9	Open-drain, power-good indicator.
VIN	10	2.5V or 3.3V power supply. A ceramic decoupling capacitor with a value between 1μF and 4.7μF is required.
TP	11	Thermal pad, connect to GND or floating

Block Diagram



Functional Description

Overview

The ET51200 device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration.

The device maintains a fast-transient response and only requires a minimum output capacitance of 20µF. The device supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low Power DDR3, and DDR4 VTT bus termination.

VIN Input Capacitor

Add a ceramic capacitor, with a value between 1.0µF and 4.7µF, placed close to the VIN pin, to stabilize the bias supply (2.5V rail or 3.3V rail) from any parasitic impedance from the supply.

VLDOIN Input Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10µF (or greater) ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at the VO pin. In general, use one-half of the C_{VO} value for input.

Output Capacitor

For stable operation, the total capacitance of the VO output pin must be greater than 20μF. Attach three, 10μF ceramic capacitors in parallel to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL). If the ESR is greater than 2mΩ, insert an RC filter between the output and the VOSNS input to achieve loop stability. The RC filter time constant should be almost the same as or slightly lower than the time constant of the output capacitor and its ESR.

Sink and Source Regulator (VO Pin)

The ET51200 is a sink and source tracking termination regulator specifically designed for low input voltage, low-cost, and low external component count systems where space is a key application parameter. The device integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, connect a remote sensing terminal, VOSNS, to the positive terminal of each output capacitor as a separate trace from the high current path from VO.

Reference Input (REFIN Pin)

The output voltage, VO, is regulated to REFOUT. When REFIN is configured for standard DDR termination applications, REFIN can be set by an external equivalent ratio voltage divider connected to the memory supply bus (VDDQ). The ET51200 device supports REFIN voltages from 0.5V to 1.8V, making it versatile and ideal for many types of low-power LDO applications.

Reference Output (REFOUT Pin)

When it is configured for DDR termination applications, REFOUT generates the DDR VTT reference voltage for the memory application. It is capable of supporting both a sourcing and sinking load of 10mA. REFOUT becomes active when REFIN voltage rises to 0.390V and VIN is above the UVLO threshold. When REFOUT is less than 0.375V, it is disabled and subsequently discharges to GND through an internal 10kΩ MOSFET. REFOUT is independent of the EN pin state.

Soft-Start Sequencing

A current clamp implements the soft-start function of the VO pin. The current clamp allows the output capacitors to be charged with low and constant current, providing a linear ramp-up of the output voltage. When VO is outside of the power-good window, the current clamp level is one-half of the full over-current limit (OCL) level. When VO rises or falls within the PGOOD window, the current clamp level switches to the full OCL level. The soft-start function is completely symmetrical and the over-current limit works for both directions. The soft-start function works not only from GND to the REFOUT voltage, but also from VLDOIN to the REFOUT voltage.

Enable Control (EN Pin)

When EN is driven high, the VO regulator begins normal operation. When the device drives EN low, VO discharges to GND through an internal 18Ω MOSFET. REFOUT remains on when the device drives EN low. Ensure that the EN pin voltage remains lower than or equal to VIN at all times.

Power Good Function (PGOOD Pin)

The ET51200 device provides an open-drain PGOOD output that goes high when the VO output is within ±20% of REFOUT. PGOOD de-asserts within 10μs after the output exceeds the size of the power-good window. During initial VO start-up, PGOOD asserts high 2ms (Typ) after the VO enters power good window. Because PGOOD is an open-drain output, a pull-up resistor with a value between 1kΩ and 100kΩ, placed between PGOOD and a stable active supply voltage rail is required.

Current Protection (VO Pin)

The LDO has a constant over-current limit (OCL). The OCL level reduces by one-half when the output voltage is not within the power-good window. This reduction is a non-latch protection.

UVLO Protection (VIN Pin)

For VIN under-voltage lockout (UVLO) protection, the ET51200 monitors VIN voltage. When the VIN voltage is lower than the UVLO threshold voltage, both the VO and REFOUT regulators are powered off. This shutdown is a non-latch protection.

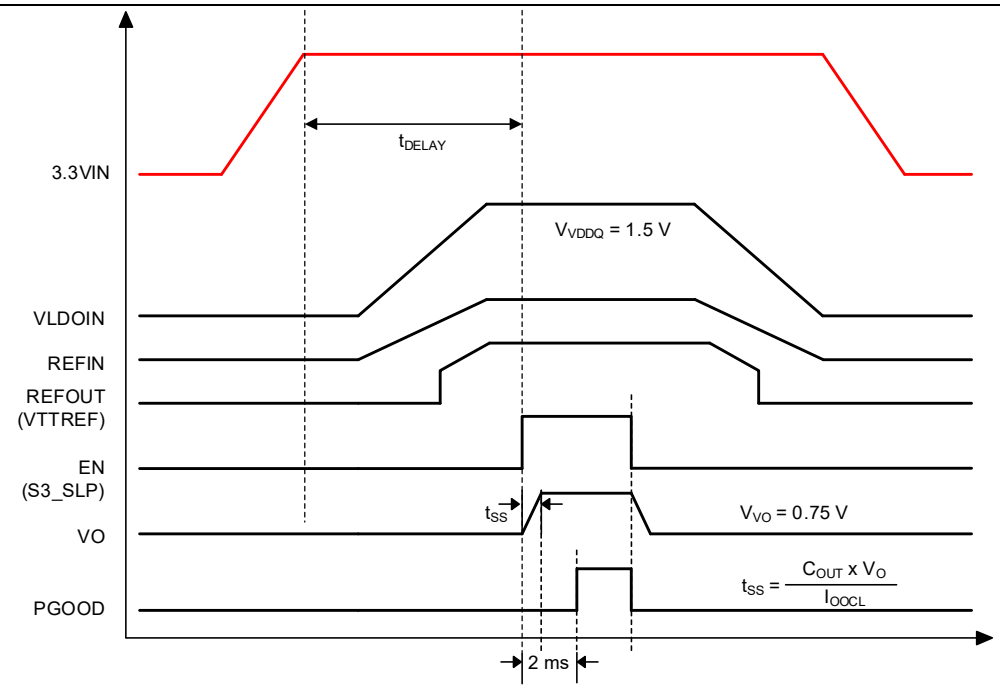
Thermal Shutdown

The ET51200 monitors junction temperature. If the device junction temperature exceeds the threshold value, (typically 150°C), the VO and REFOUT regulators both shut off, discharged by the internal discharge MOSFETs. This shutdown is a non-latch protection.

Tracking Start-up and Shutdown

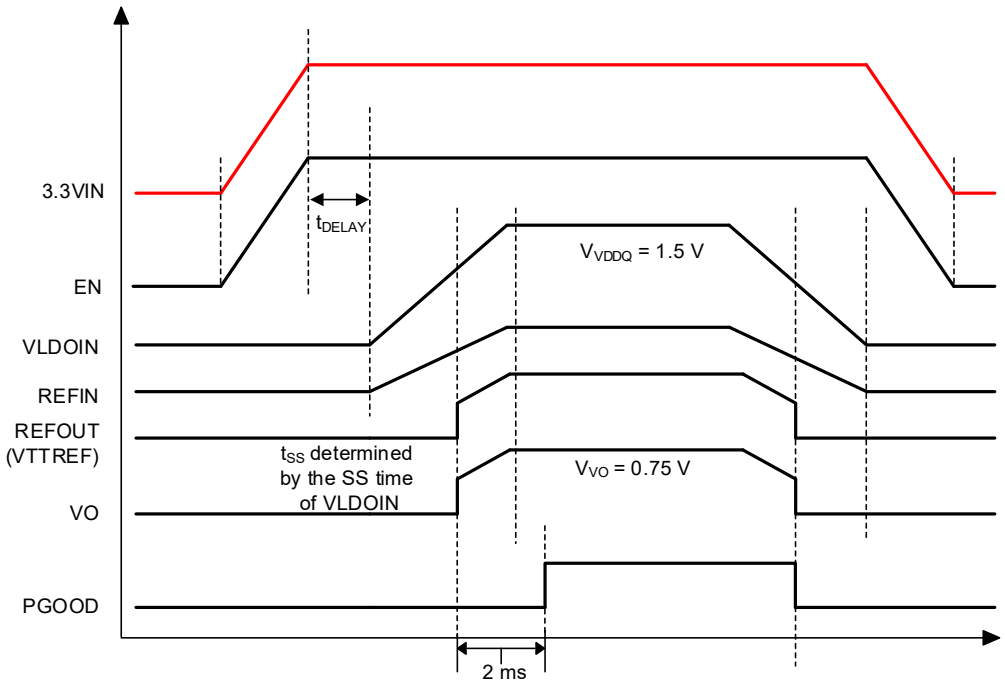
The ET51200 also supports tracking start-up and shutdown when the EN pin is tied directly to the system bus and not used to turn on or turn off the device. During tracking start-up, VO follows REFOUT once REFIN voltage is greater than 0.39V. REFIN follows the rise of VDDQ rail through a voltage divider.

The typical soft-start time (t_{SS}) for the V_{DDQ} rail is approximately 3ms, however it may vary depending on the system configuration. The soft-start time of the VO output no longer depends on the OCL setting, but it is a function of the soft-start time of the VDDQ rail. PGOOD is asserted 2ms after V_{VO} is within ±20% of REFOUT. During tracking shutdown, the VO pin voltage falls following REFOUT until REFOUT reaches 0.37V. When REFOUT falls below 0.37V, the internal discharge MOSFETs turn on and quickly discharge both REFOUT and VO to GND. PGOOD is deasserted when VO is beyond the ±20% range of REFOUT. Figure 2 shows the typical timing diagram for an application that uses tracking start-up and shutdown.



Note: It is recommended that after the VIN is powered on, wait until the internal logic is completely stable before starting the LDO. The t_{DELAY} time is suggested to be greater than 250ms.

Figure 1. Typical Timing Diagram for S3 and Pseudo-S5 Support



Note: It is recommended that after the VIN is powered on, wait until the internal logic is completely stable before starting the LDO. The t_{DELAY} time is suggested to be greater than 250ms.

Figure 2. Typical Timing Diagram of Tracking Start-up and Shutdown

Output Tolerance Consideration for VTT DIMM Applications

The ET51200 is specifically designed to power up the memory termination rail (as shown in Figure 3). The DDR memory termination structure determines the main characteristics of the VTT rail, which is to be able to sink and source current while maintaining acceptable VTT tolerance. See Figure 4 for typical characteristics for a single memory cell.

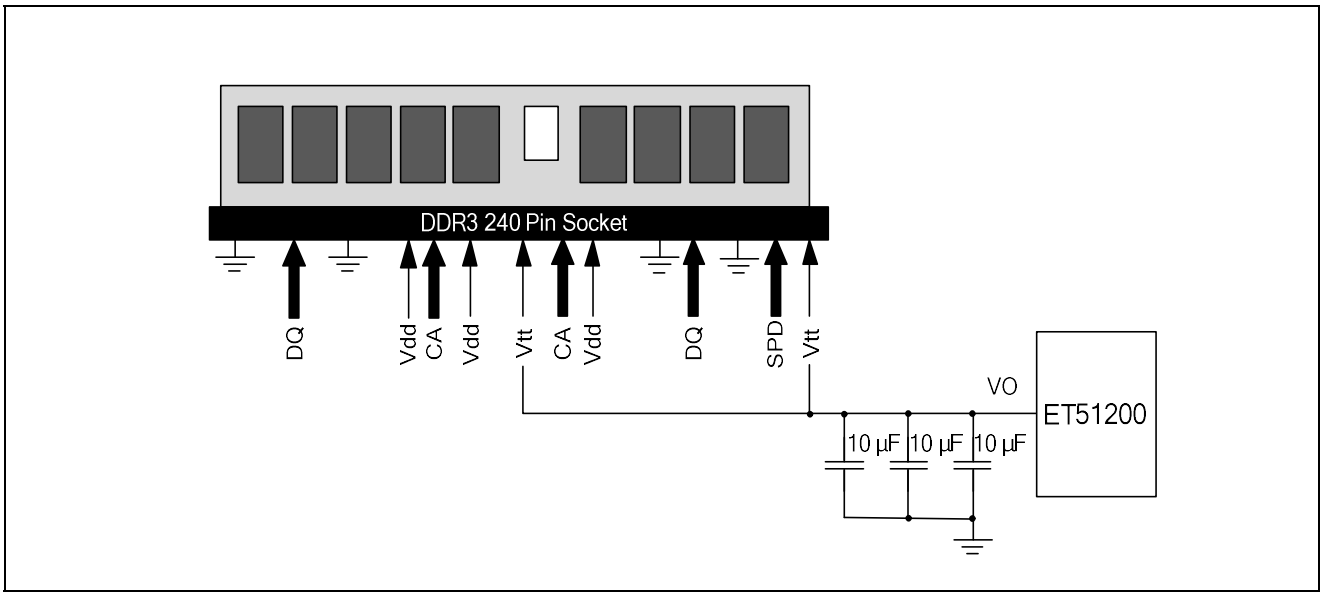


Figure 3. Typical Application Diagram for DDR3 VTT DIMM using ET51200

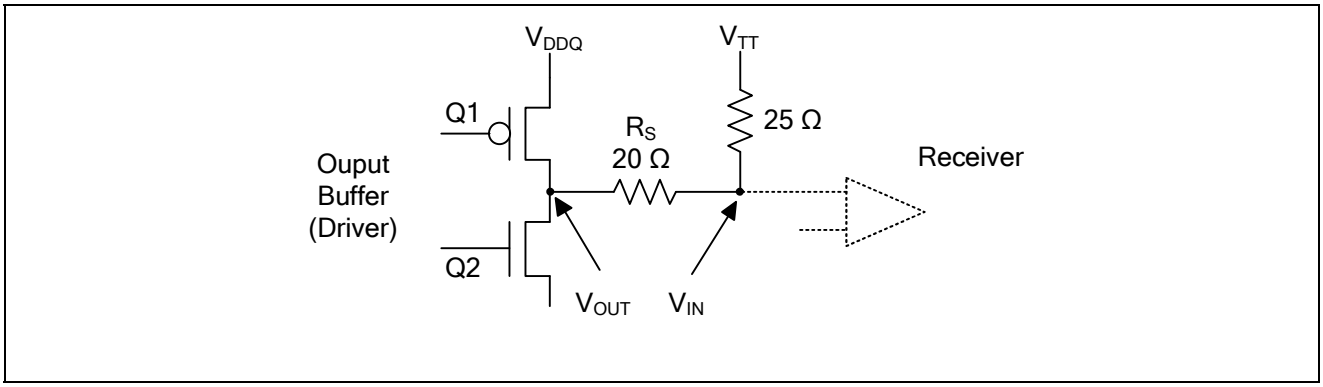


Figure 4. DDR Physical Signal System Bi-Directional SSTL Signaling

In Figure 4, when Q1 is on and Q2 is off:

• Current flows from VDDQ via the termination resistor to VTT

• VTT sinks current

In Figure 4, when Q2 is on and Q1 is off:

• Current flows from VTT via the termination resistor to GND

• VTT sources current

Because VTT accuracy has a direct impact on the memory signal integrity, it is imperative to understand the tolerance requirement on VTT. Equation 1 applies to both DC and AC conditions and is based on JEDEC VTT specifications for DDR and DDR2 (JEDEC standard: DDR JESD8-9B May 2002; DDR2 JESD8-15A Sept 2003).

$$V_{VTTREF} - 40mV < V_{VTT} < V_{VTTREF} + 40mV \quad (1)$$

The specification itself indicates that VTT must keep track of VTTREF for proper signal conditioning. The ET51200 ensures the regulator output voltage to be as shown in Equation 2, which applies to both DC and AC conditions.

$$V_{VTTREF} - 25mV < V_{VTT} < V_{VTTREF} + 25mV \quad (2)$$

where

$-2A < I_{VTT} < 2A$

The regulator output voltage is measured at the regulator side, not the load side. The tolerance is applicable to DDR, DDR2, DDR3, DDR3L, Low Power DDR3, and DDR4 applications (see Table 1 for detailed information). To meet the stability requirement, a minimum output capacitance of 20μF is needed. Considering the actual tolerance on the MLCC capacitors, three 10μF ceramic capacitors sufficiently meet the VTT accuracy requirement.

Table 1. DDR, DDR2, DDR3 and LP DDR3 Termination Technology

	DDR	DDR2	DDR3	LOW POWER DDR3
FSB Data Rates	200, 266, 333, and 400MHz	400, 533, 677, and 800MHz	800, 1066, 1330, and 1600MHz	
Termination	Motherboard termination to VTT for all signals	On-die termination for data group. VTT termination for address, command and control signals	On-die termination for data group. VTT termination for address, command and control signals	
Termination Current Demand	Maximum source/sink transient currents of up to 2.6A to 2.9A	Not as demanding	Not as demanding	
		Only 34 signals (address, command, control) tied to VTT	Only 34 signals (address, command, control) tied to VTT	
		ODT handles data signals	ODT handles data signals	
		Less than 1A of burst current	Less than 1A of burst current	
Voltage Level	2.5V Core and I/O 1.25V VTT	1.8V Core and I/O 0.9V VTT	1.5V Core and I/O 0.75V VTT	1.2V Core and I/O 0.6V VTT

The ET51200 uses transconductance (g_M) to drive the LDO. The transconductance and output current of the device determine the voltage droop between the reference input and the output regulator. The typical transconductance level is 250 S at 2A and changes with respect to the load in order to conserve the quiescent current (that is, the transconductance is very low at no load condition). The (gM) LDO regulator is a single pole system. Only the output capacitance determines the unity gain bandwidth for the voltage loop, as a result of the bandwidth nature of the transconductance (see Equation 3).

$$f_{UGBW} = \frac{g_M}{2 \times \pi \times C_{OUT}} \quad (3)$$

where

- f_{UGBW} is the unity gain bandwidth
- g_M is transconductance
- C_{OUT} is the output capacitance

Consider these two limitations to this type of regulator that come from the output bulk capacitor requirement.

In order to maintain stability, the zero-location contributed by the ESR of the output capacitors must be greater than the -3dB point of the current loop. This constraint means that higher ESR capacitors should not be used in the design.

In addition, the impedance characteristics of the ceramic capacitor should be well understood in order to prevent the gain peaking effect around the transconductance (g_M) -3dB point because of the large ESL, the output capacitor and parasitic inductance of the VO pin voltage trace.

REFOUT (VREF) Consideration for DDR2 Applications

During ET51200 tracking start-up, the REFIN voltage follows the rise of the V_{DDQ} rail through a voltage divider, and REFOUT (V_{REF}) follows REFIN once the REFIN voltage is greater than 0.39V. When the REFIN voltage is lower than 0.39V, V_{REF} is 0V.

The JEDEC DDR2 SDRAM Standard (JESD79-2E) states that VREF must track VDDQ/2 within ±0.3V accuracy during the start-up period. To allow the ET51200 device to meet the JEDEC DDR2 specification, a resistor divider can be used to provide the VREF signal to the DIMM. The resistor divider ratio is 0.5 to ensure that the VREF voltage equals VDDQ/2.

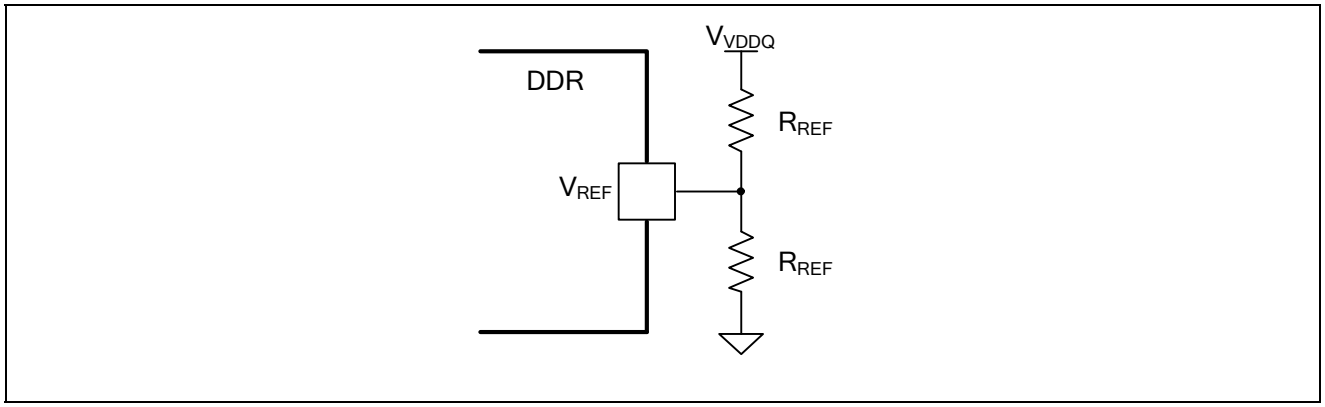


Figure 5. Resistor Divider Circuit

When selecting the resistor value, consider the impact of the leakage current from the DIMM VREF pin on the reference voltage. Use Equation 4 to calculate resistor values.

$$R_{REF} \leq \frac{2 \times \Delta V_{REF}}{I_{REF}} \quad \textbf{(4)}$$

where

- R_{REF} is the resistor value
- ΔV_{REF} is the VREF DC variation requirement
- I_{REF} is the maximum total VREF leakage current from DIMMs

Low Input Voltage Applications

ET51200 can be used in an application system that offers either a 2.5V rail or a 3.3V rail. The ET51200 device has a minimum input voltage requirement of 2.375V. If a 2.5V rail is used, ensure that the absolute minimum voltage (both DC and transient) at the device pin is be 2.375V or greater. The voltage tolerance for a 2.5V rail input is between ±5% accuracy, or better.

S3 and Pseudo-S5 Support

The ET51200 provides S3 support by an EN function. The EN pin could be connected to an SLP_S3 signal in the end application. Both REFOUT and VO are on when EN = high (S0 state). REFOUT is maintained while VO is turned off and discharged via an internal discharge MOSFET when EN = low (S3 state). When EN = low and the REFIN voltage is less than 0.390V, ET51200 enters pseudo-S5 state. Both VO and REFOUT outputs are turned off and discharged to GND through internal MOSFETs when pseudo-S5 support is engaged (S4 or S5 state). Figure 1 shows a typical start-up and shutdown timing diagram for an application that uses S3 and pseudo-S5 support.

Absolute Maximum Ratings

Symbol	Parameters (Items)	Value	Unit
V_{REFIN}	REFIN Voltage	-0.3 to 3.6	V
V_{IN}	VIN Voltage	-0.3 to 6.0	V
V_{LDOIN}	VLDOIN Voltage	-0.3 to 3.6	V
V_{OSNS}	VOSNS Voltage	-0.3 to 3.6	V
V_{EN}	EN Voltage	-0.3 to 6.5	V
V_{PGND}	PGND Voltage	-0.3 to 0.3	V
V_{REFOUT}	REFOUT Voltage	-0.3 to 3.6	V
V_O	VO Voltage	-0.3 to 3.6	V
V_{PGOOD}	PGOOD Voltage	-0.3 to 6.5	V
T_J	Maximum Operating Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_L	Lead Temperature (Soldering, 10 sec)	300	°C
V_{ESD}	Human Body Model (JESD22-A114)	±2000	V
	Charged Device Model (JESD22-C101)	±500	

Thermal Characteristics

Symbol	Ratings	Value	Unit
$R_{\theta JA}$	Junction-to-Ambient thermal resistance	56	°C/W
$R_{\theta JC(TOP)}$	Junction-to-Case(TOP) thermal resistance	86	°C/W
$R_{\theta JB}$	Junction-to-Board thermal resistance	30	°C/W
P_D	Max power dissipation	2.2	W

Recommended Operating Conditions

Symbol	Parameters	Rating	Unit
V_{IN}	VIN Voltage	2.375 to 5.5	V
V_{EN}	EN Voltage	-0.1 to 3.5V	V
V_{LDOIN}	VLDOIN Voltage	-0.1 to 3.5V	V
V_{OSNS}	VOSNS Voltage	-0.1 to 3.5V	V
V_{REFIN}	REFIN Voltage	0.5 to1.8	V
V_{PGOOD}	PGOOD Voltage	-0.1 to 3.5	V
V_O	VO Voltage	-0.1 to 3.5	V
V_{REFOUT}	REFOUT Voltage	-0.1 to 1.8	V
V_{PGND}	PGND Voltage	-0.1 to 0.1	V
T_A	Operating Free-air Temperature	-40 to 85	°C

Electrical Characteristics

Over recommended free-air temperature range, V_{IN} = 3.3V, V_{VLDOIN} = 1.8V, V_{REFIN} = 0.9V, V_{VOSNS} = 0.9V, V_{EN} = V_{IN}, C_{OUT} = 3 × 10μF (unless otherwise noted).

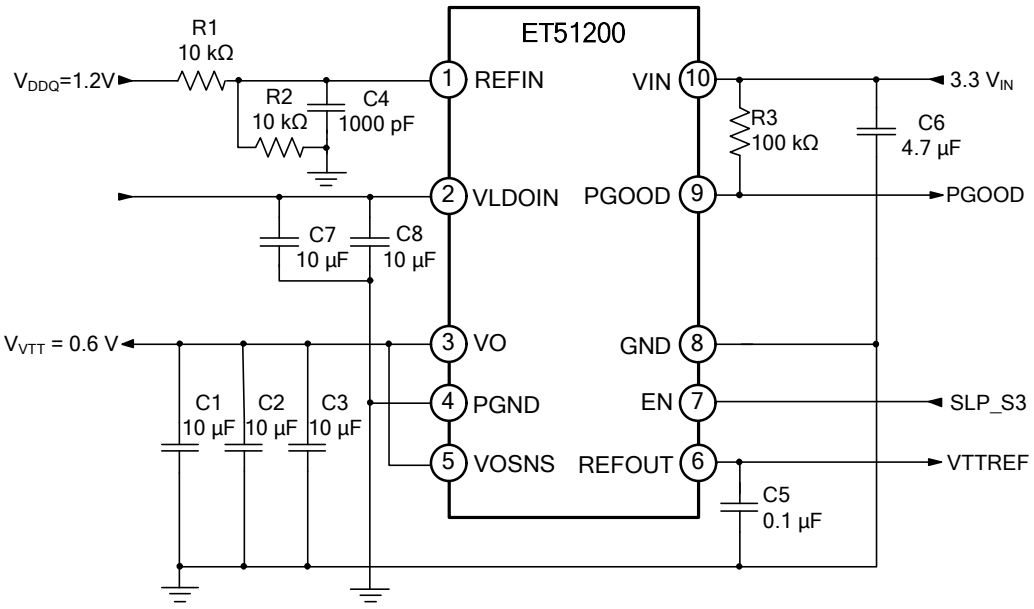
Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Operation Range		2.375		5.5	V
V_{VLDOIN}	Power Supply Voltage Operation Range		1.1		3.5	V
SUPPLY CURRENT						
I_{IN}	Supply Current	T_A = 25°C, V_{EN} = 3.3V, No Load	0.40	0.60	1.0	mA
I_{IN_SHDN}	Shutdown Current	T_A = 25°C, V_{EN} = 0V, V_{REFIN} = 0, No Load	35	55	80	μA
		T_A = 25°C, V_{EN} = 0V, V_{REFIN} > 0.4V, No Load	120	190	400	
I_{LDOIN}	Supply Current of VLDOIN	T_A = 25°C, V_{EN} = 3.3V, No Load		1	50	μA
I_{LDOIN_SHDN}	Shutdown Current of VLDOIN	T_A = 25°C, V_{EN} = 0V, No Load		0.1	50	
INPUT CURRENT						
I_{REFIN}	Input Current, REFIN	V_{EN} = 3.3V			1	μA
VO OUTPUT						
V_{VOSNS}	Output DC Voltage, VO	V_{REFOUT} = 1.25V (DDR1), I_O = 0A	-15		15	mV
		V_{REFOUT} = 0.90V (DDR2), I_O = 0A	-15		15	mV
		V_{REFOUT} = 0.75V (DDR3), I_O = 0A	-15		15	mV
		V_{REFOUT} = 0.675V (DDR3L), I_O = 0A	-15		15	mV
		V_{REFOUT} = 0.6V (DDR4), I_O = 0A	-15		15	mV
V_{VOTOL}	Output Voltage Tolerance to REFOUT	-2A < I_{VO} < 2A	-25		25	mV
I_{VOSRCL}	VO Source Current Limit	With reference to REFOUT, V_{OSNS} = 90% × V_{REFOUT}	3.0	4.5		A
I_{VOSNCL}	VO Sink Current Limit	With reference to REFOUT, V_{OSNS} = 110% × V_{REFOUT}	3.5	5.5		A
I_{DSCHRG}	Discharge Current, VO	V_{REFIN} = 0V, V_{VO} = 0.3V, V_{EN} = 0V, T_A = 25°C	8	15	25	Ω
POWERGOOD COMPARATOR						
V_{PG_TH}	VO PGOOD Threshold	PGOOD window lower threshold with respect to REFOUT	-23.5	-20	-17.5	%
		PGOOD window upper threshold with respect to REFOUT	17.5	20	23.5	
		PGOOD hysteresis		5		
V_{PG_OL}	Output Low Voltage	I_{SINK} = 4mA			0.4	V

Electrical Characteristics(Continued)

Over recommended free-air temperature range, V_{IN} = 3.3V, V_{VLDOIN} = 1.8V, V_{REFIN} = 0.9V, V_{VOSNS} = 0.9V, V_{EN} = V_{VIN}, C_{OUT} = 3 × 10μF (unless otherwise noted)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
POWERGOOD COMPARATOR (Continued)						
t_{PG_DELAY}	PGOOD Start-up Delay	Start-up rising edge, VOSNS within 15% of REFOUT		2		ms
t_{PG_BADDLY}	PGOOD Bad Delay	VOSNS is outside of the ±20% PGOOD window		10		μs
I_{PG_LKG}	PGOOD Leakage Current	V_{OSNS} = V_{REFIN} (PGOOD high impedance), V_{PGOOD} = V_{VIN} + 0.2V			1	μA
REFIN AND REFOUT						
V_{REFIN}	REFIN Voltage Range		0.5		1.8	V
V_{REFIN_UVLO}	REFIN Under-voltage Lockout	REFIN rising	360	390	420	mV
V_{REFIN_HYS}	REFIN Under-voltage Lockout Hysteresis		10	20	50	mV
V_{REFOUT}	REFOUT Voltage			V_{REFIN}		V
V_{REFOUT_OL}	REFOUT Voltage Tolerance to VREFIN	-1mA < I_{REFOUT} < 1mA, V_{REFIN} = 1.25V	-12		12	mV
		-1mA < I_{REFOUT} < 1mA, V_{REFIN} = 0.90V	-12		12	mV
		-1mA < I_{REFOUT} < 1mA, V_{REFIN} = 0.75V	-12		12	mV
		-1mA < I_{REFOUT} < 1mA, V_{REFIN} = 0.675V	-12		12	mV
		-1mA < I_{REFOUT} < 1mA, V_{REFIN} = 0.60V	-12		12	mV
I_{REFOUT_SRCL}	Source Current Limit	V_{REFOUT} = 0V	10	40		mA
I_{REFOUT_SNCL}	Sink Current Limit	V_{REFOUT} = 0V	10	40		mA
UVLO AND EN LOGIC THRESHOLD						
V_{VIN_UVLO}	UVLO Threshold	Wake up, T_A = 25°C	2.100	2.300	2.375	V
		Hysteresis		50		mV
V_{ENH}	High-level Input Voltage	Enable, V_{IN}= 3.3V	1.7			V
V_{ENL}	Low-level Input Voltage	Enable, V_{IN}= 3.3V			0.3	V
V_{ENHYS}	Hysteresis Voltage	Enable, V_{IN}= 3.3V		0.5		V
I_{EN_LKG}	Logic Input Leakage Current	EN, T_A = 25°C	-1		1	μA
THERMAL SHUTDOWN						
T_{TSD}	Thermal Shutdown Threshold	Shutdown temperature		150		°C
T_{TSH}		Hysteresis		25		

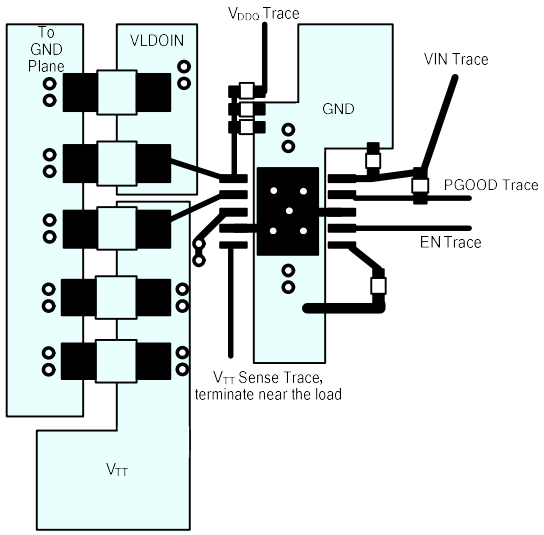
Application Circuits



*This design example describes a 3.3 VIN, DDR3 configuration.

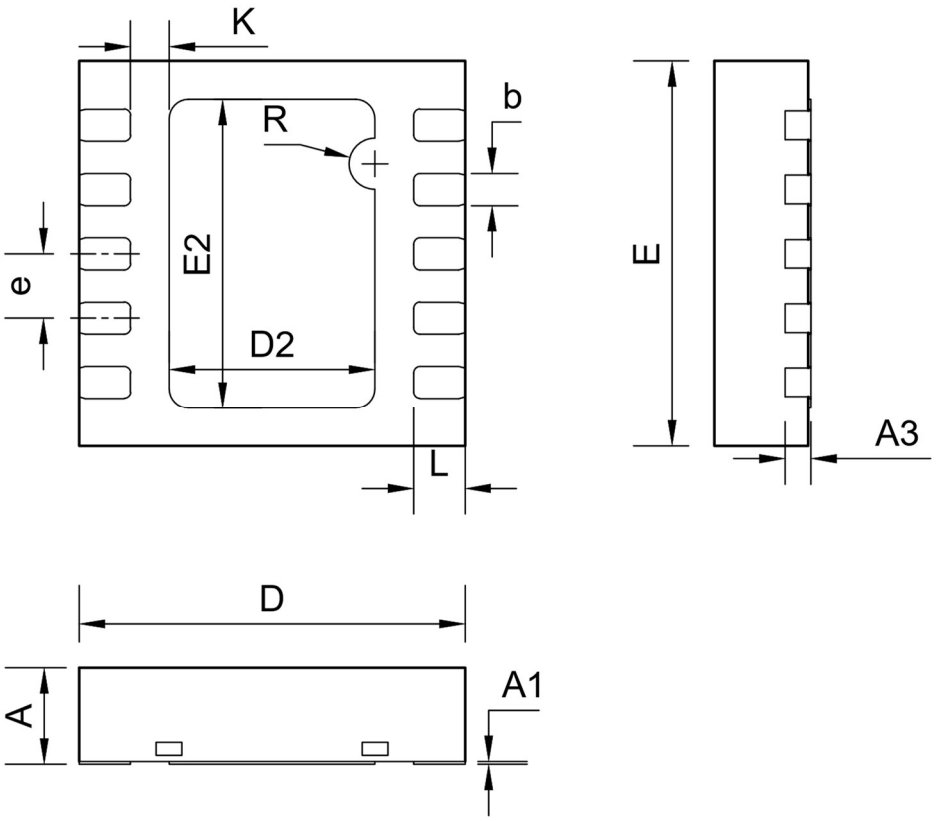
PCB Layout Guide

DFN10



Package Dimension

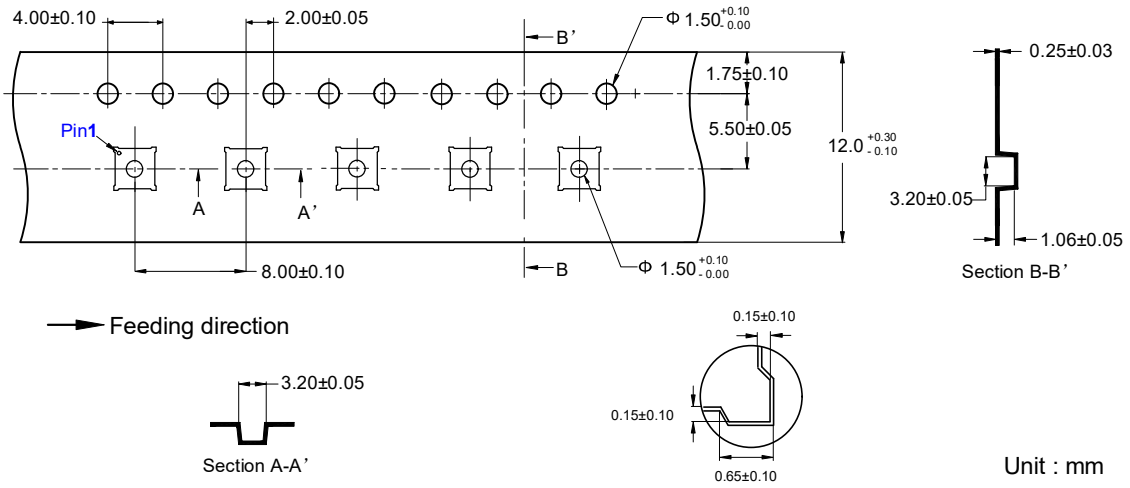
DFN10



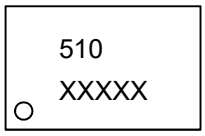
COMMON DIMENSIONS
(UNITS OF MEASURE = MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.55	1.65	1.75
E2	2.30	2.40	2.50
e	0.40	0.50	0.60
K	0.175	0.275	0.375
L	0.35	0.40	0.45
R		0.20REF	

Tape Information



Marking Information



510 - Part Number

XXXXX - Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2023-04-24	Preliminary Version	Dongsh,Tugz	Shib	Liujy
0.1	2023-12-12	Update Package Picture	Shibo	Shib	Liujy
1.0	2024-01-14	Official Version	Shibo	Shib	Liujy
1.1	2024-08-01	Update SPEC	Tugz	Liuxm	Liujy
1.2	2026-09-01	Update EC table	Xut	Liuxm	Liujy
1.2.a	2026-10-23	Update Format	Xut	Liuxm	Liujy