ET3166 - 6 CH Load Switch with I²C Control

General Description

The ET3166 is CMOS-based 6 channels integrated load switch with I²C Control. Load switch 1 to 6 contains P-Channel MOSFET that can operate over an input voltage of 1.2V to 5.5V and supports a maximum continuous current of 2A.

The ET3166 is available in small package: WLCSP16 (1.54mm×1.54mm,0.35mm pitch).

Features

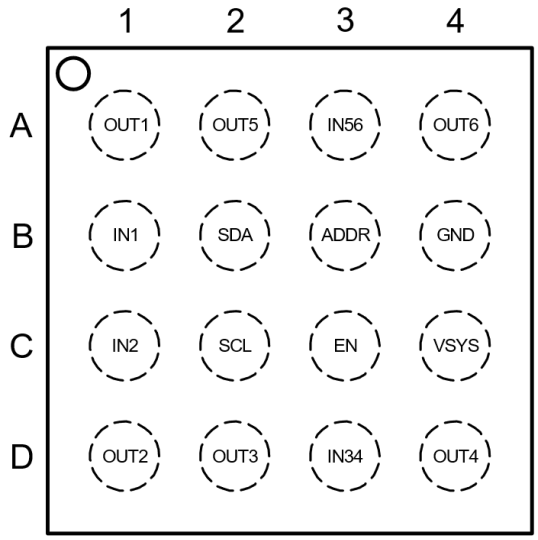
- Load switch 1 to 6 input voltage operating range: 1.2V to 5.5V
- Load switch 1 to 6 typical $R_{DS(ON)}$:
  - 52mΩ at V_{INX} = 5V
  - 120mΩ at V_{INX} = 1.8V
- V_{SYS} input voltage operation range: 1.6V to 5.5V
- I²C serial control to program each load switch on/off
- Part No. and package

Part No.	Package	MSL
ET3166	WLCSP16 (1.54×1.54mm,0.35mm pitch)	Level 1

Applications

- Constant-voltage power supply for battery-powered device
- Constant-voltage power supply for smartphones, tables
- Constant-voltage power supply for cameras, DVRs, STB and camcorders

Pin Configuration

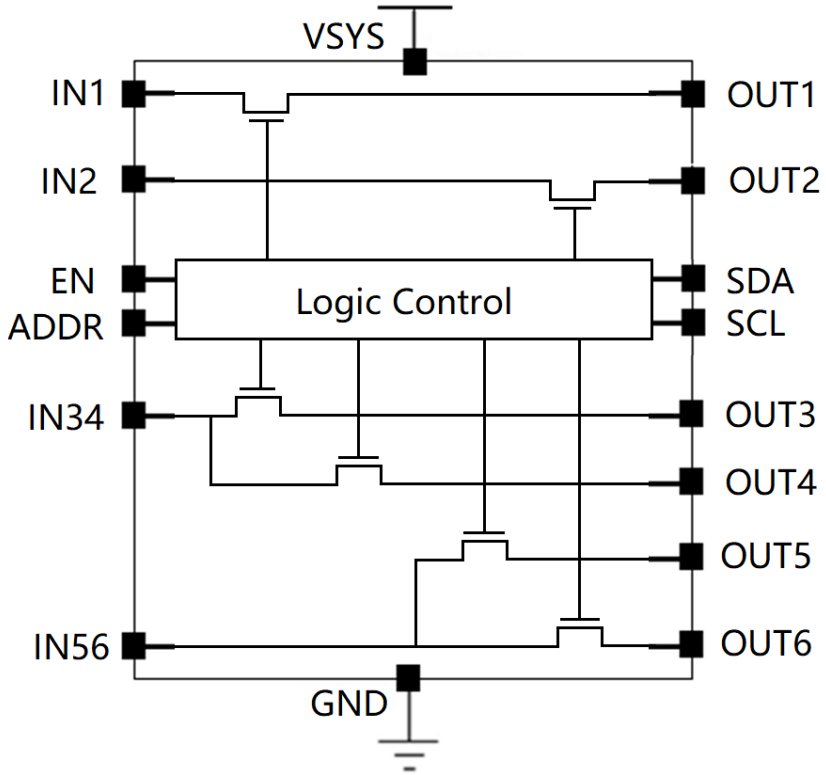


Top View

Pin Function

Pin No.	Pin Name	Pin Function
A1	OUT1	Load switch 1 output.
A2	OUT5	Load switch 5 output.
A3	IN56	Load switch 5 and 6 supply input.
A4	OUT6	Load switch 6 output.
B1	IN1	Load switch 1 supply input.
B2	SDA	I^2C interface.
B3	ADDR	I^2C address set pin.
B4	GND	Ground pin.
C1	IN2	Load switch 2 supply input.
C2	SCL	I^2C interface.
C3	EN	Load switch output Enable(active high), Device will reset all registers to default value when EN pin is low.
C4	VSYS	System Supply input.
D1	OUT2	Load switch 2 output.
D2	OUT3	Load switch 3 output.
D3	IN34	Load switch 3 and 4 supply input.
D4	OUT4	Load switch 4 output.

Block Diagram



Note：The OUTx port has fast turn-off discharge circuit. This function can be turned off by I²C command.

Functional Description

ET3166 has 6 channels load switch. Load switch 1 to 6 are using PMOSFET.

Startup

The ET3166 LDSW's can be enabled two ways using the I²C register bits if EN is high.

1. Setting LDSWX_SEQ = 000 in 0x05(LDSW12_SEQ) or 0x06(LDSW34_SEQ) or 0x07(LDSW56_SEQ) and the LDSWX_EN assigned to the LDSW in register, ENABLE to 1.

2. Setting LDSWX_SEQ > 000 in registers and then set seq_ctrl[1:0] = 2'b01 in SEQ_CTR register.

Power-up and shut down of each regulator can be controlled by an I²C register. It can be set at the registers ldswx_seq[2:0] (x=1 to 7) respectively. ldswx_en is an internal signal to enable one of regulators, if ldsw_seq[2:0] set to '000', that LDSWX channel can be controlled directly by a bit specified in register LDSW_EN.

3. Automatic Power Up/Down Sequence Control

ET3166 has seven SLOTs to which each regulator can be assigned;

They are started by seq_ctrl[1:0] signal. when seq_ctrl[1:0] is set '01'. Internal counter seq_cnt[2:0] starts increments from 0 ("000") to 7 ("111"). When seq_ctrl[1:0] is set '10', seq_cnt[2:0] decrements from 7 ("111") to 0 ("000"). Regulators assigned to one of SLOTs starts power-up or power-down.

The seq_cnt[2:0] matches the SLOT number, when seq_cnt[2:0]=000, it indicates that sequencing has completed or not started.

Internal logic signal seq_on=1 indicates that sequencing is executing and somewhere between the start of slot1 and the end of slot7, seq_on=0, it indicates that has completed or not started.

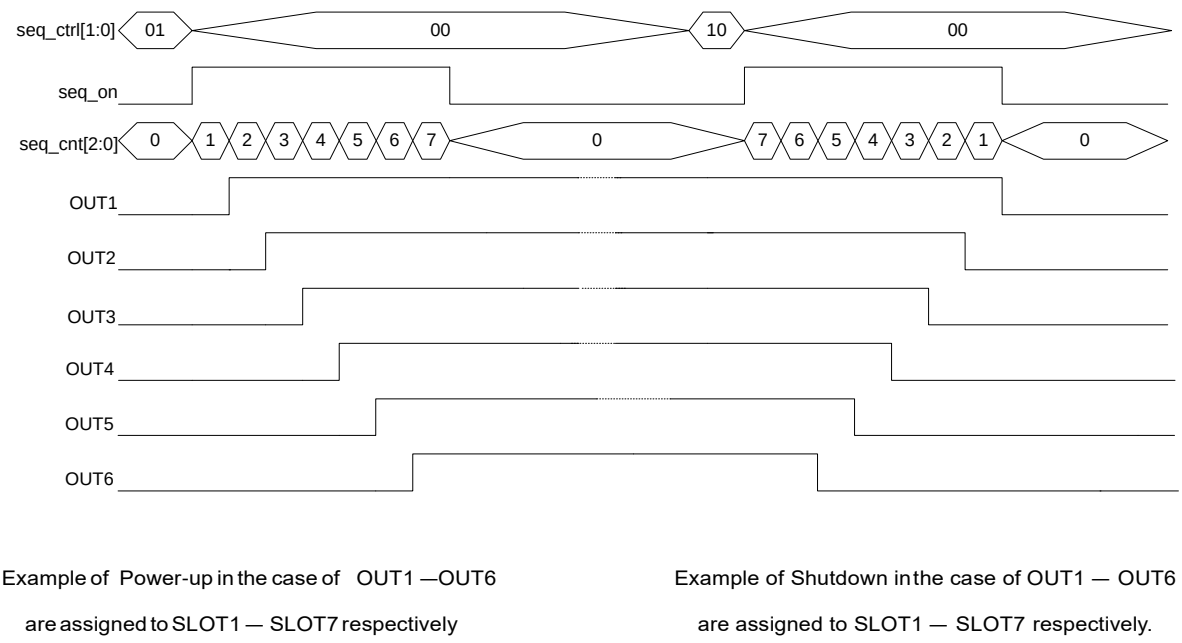


Figure 1.

4. EN Pin Control

When EN pin is in low level, the IC is shut down, all internal circuits are off, and all the parts draw very little current. In this state, all the registers will be reset to their default value, and I^2C cannot be written to or read.

Input and output Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between the V_{INX} and GND pins. A 1μF ceramic capacitor, C_{INX}, placed close to the pins is usually sufficient. Higher-value C_{INX} can be used to reduce the voltage drop in higher-current applications.

A 0.1μF capacitor, C_{OUTX}, should be placed between the V_{OUTX} and GND pins. This capacitor prevents parasitic board inductance from forcing V_{OUTX} below GND when the switch is on. C_{INX} greater than C_{OUTX} is highly recommended. C_{OUTX} greater than C_{IN} can cause V_{OUTX} to exceed V_{INX} when the system supply is removed. This could result in current flow through the body diode from V_{OUTX} to V_{INX}.

Recommended C_{VSYS}=1.0uF or greater.

Auto Discharging

For each channel, when shut down the output, the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of output pin in very short time. The Auto-Discharging function is optional. Set related bits to select output discharge function for Discharge

Resistor (LDSW_DIS Register), “0”: Disable. “1”: Enable.

RCB function

ET3166 has a true Reverse Current function that obstructs unwanted reverse current from OUTx to INx during both ON and OFF states. The RCB function can be set by I²C instruction(LDSW_RCB register).

LSWx state	ldswx_rcb	RCB function
OFF	0	Y
OFF	1	Y
ON	0	N
ON	1	Y

Note：x is 1~6.

LSWx state is controlled by EN pin or LDSW_EN Register.

Serial Port Interface (I²C)

Bus Interface

Baseband Processor can transmit data with ET3166 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is high, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET3166 will send a low level response signal with one period width to the SDA port. During the reading mode, ET3166 will not send response signal and the host will send a high response signal one period width to the SDA.

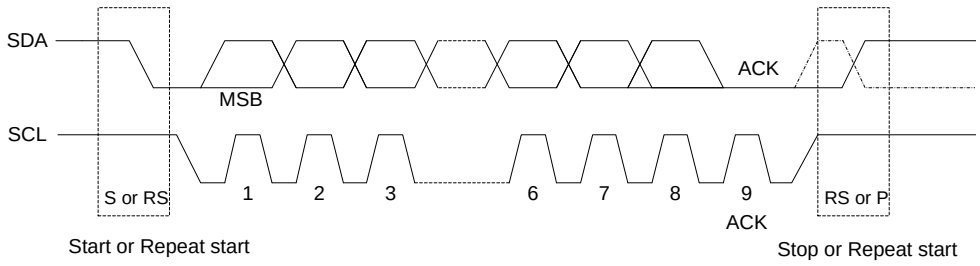


Figure 2. I²C write mode

ACK=Acknowledge

MSB=Most Significant Bit

S=Start Conditions RS=Restart Conditions P=Stop Conditions

Fastest Transmission Speed =400kHz

Restart: SDA-level turnover as expressed by the dashed line waveform

7bit Chip Address：

Address	ADDR Pin Set
0011000b	ADDR connect to GND
0011001b	ADDR connect to VSYS

I²C Writing Command Register Interface Protocol (continuous)：

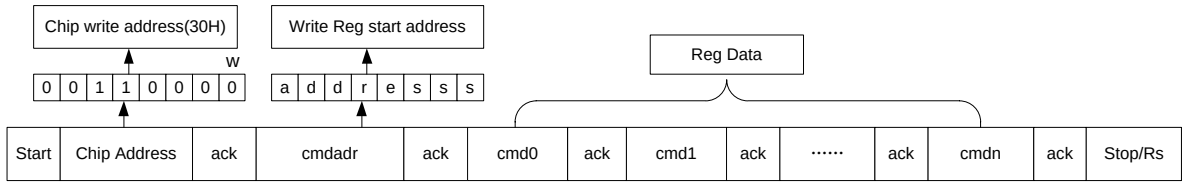


Figure 3. I²C Writing Command Register(continuous)

ACK=Acknowledge

Start=Start Conditions

Chip address=Write register address =0011000+0(w)b

ack=Acknowledge

Write Reg start address byte = cmdadr(x+ REG's 7bit address)

ack=Acknowledge

Reg data 0 = cmd0(Command data0)

ack=Acknowledge

……

Reg data n =cmdn(Command datan)

ack=Acknowledge

Stop/Rs=Stop Condition/Restart Condition

I²C Writing Command Register Interface Protocol (single)：

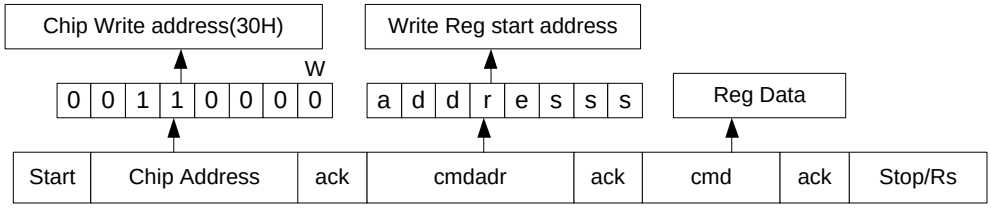


Figure 4. I²C Writing Command Register(single)

Start=Start Conditions

Chip address =Write register address=0011000+0(w)b

ack=Acknowledge

Write Reg start address byte = cmdadr(x + REG's 7bit address)

ack=Acknowledge

Reg data= cmd(Command data)

ack=Acknowledge

Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol (continuous)

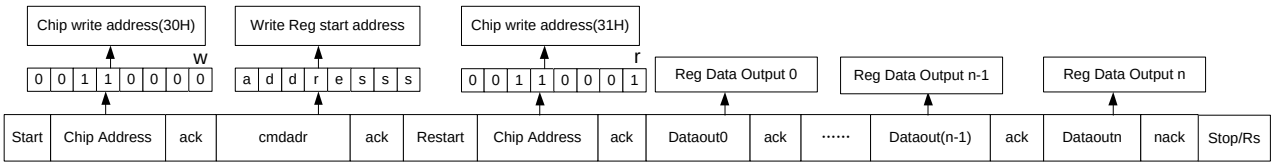


Figure 5. I²C Reading Command Register(continuous)

Start=Start Conditions

Chip address =Write register address=0011000+0(w)b

ack=Acknowledge from ET3166

Write Reg start address byte = cmdadr(x + REG's 7bit address)

ack=Acknowledge from ET3166

Restart=Restart condition

Chip address Read register address=0011000+1(r)b

ack=Acknowledge from ET3166

Dataout0=Register data output 0

ack=Acknowledge from Host

……

Dataoutn=Register data output n

nack=No Acknowledge from Host

Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol (single)

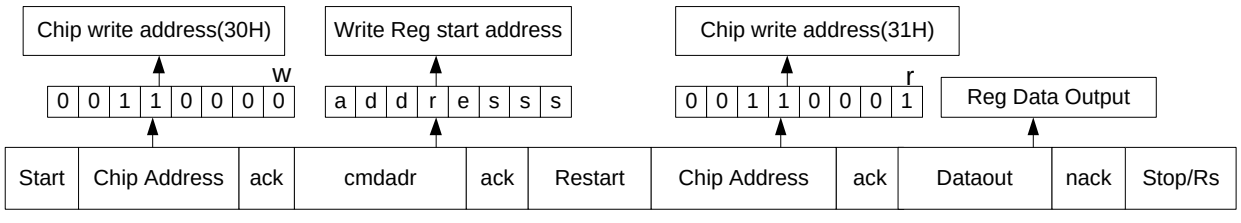


Figure 6. I²C Reading Command Register

Start=Start Conditions

Chip address =Write register address=0011000+0(w)b

ack=Acknowledge from ET3166

Write Reg start address byte = cmdadr(x + REG's 7bit address)

ack=Acknowledge from ET3166

Restart=Restart condition

Chip address Read register address=0011000+1(r)b

ack=Acknowledge from ET3166

Dataout=Register data output

nack=No Acknowledge from Host

Stop/Rs=Stop Condition/Restart Condition

Register Map

Addr	Name	RST	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	CHIPID	0x30	001100						chip_id[1:0]	
0x01	VERID	0x00	000000						ver_id[1:0]	
0x02	LDSW_EN	0x00	0	0	ldsw6_en	ldsw5_en	ldsw4_en	ldsw3_en	ldsw2_en	ldsw1_en
0x03	LDSW_DIS	0x3F	0	0	ldsw6_dis	ldsw5_dis	ldsw4_dis	ldsw3_dis	ldsw2_dis	ldsw1_dis
0x04	LDSW_TR0	0x00	0	0	ldsw6_tr0	ldsw5_tr0	ldsw4_tr0	ldsw3_tr0	ldsw2_tr0	ldsw1_tr0
0x05	LDSW12_SEQ	0x00	0	0	ldsw2_seq[2:0]			ldsw1_seq[2:0]		
0x06	LDSW34_SEQ	0x00	0	0	ldsw4_seq[2:0]			ldsw3_seq[2:0]		
0x07	LDSW56_SEQ	0x00	0	0	ldsw6_seq[2:0]			ldsw5_seq[2:0]		
0x08	SEQ_CTR	0x00	seq_speed[1:0]		seq_ctrl[1:0]		seq_on	seq_cnt[2:0]		
0x09	LDSW_TR1	0x00	0	0	ldsw6_tr1	ldsw5_tr1	ldsw4_tr1	ldsw3_tr1	ldsw2_tr1	ldsw1_tr1
0x0A	LDSW_RCB	0x00	0	0	ldsw6_rcb	ldsw5_rcb	ldsw4_rcb	ldsw3_rcb	ldsw2_rcb	ldsw1_rcb
0x0B	LDSW_STA	0x00	0	0	ldsw6_sta	ldsw5_sta	ldsw4_sta	ldsw3_sta	ldsw2_sta	ldsw1_sta
0x69	SOFTRST_CTR	0x00	Write B0H to this register can reset all the registers to their default value							

Note: Rev.—Reserve, keep "0".

Register description

0x00 CHIPID Register---- Indicates the product ID with revision. Default = 0x30

chip_id[1:0] Indicates the product ID with revision. Read only.

0x01 VERID Register---- Indicates the device ID with revision. Default = 0x00

ver_id[1:0] Indicates the device ID with revision. Read only.

0x02 LDSW_EN Register ----LDSWs enable control register. Default = 0x00

Load Switch enable control register by I^2C while the register value of ldswx_seq[2:0] are set to be default "000". This register can be written to enable or disable the corresponding LDSW regulator.

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	Rev.	0	R	Reserved
5	ldsw6_en	0	R/W	LDSW6 enable control : 0b:Disable 1b: Enable
4	ldsw5_en	0	R/W	LDSW5 enable control : 0b:Disable 1b: Enable
3	ldsw4_en	0	R/W	LDSW4 enable control : 0b:Disable 1b: Enable

2	ldsw3_en	0	R/W	LDSW3 enable control : 0b:Disable 1b: Enable
1	ldsw2_en	0	R/W	LDSW2 enable control : 0b:Disable 1b: Enable
0	ldsw1_en	0	R/W	LDSW1 enable control : 0b:Disable 1b: Enable

0x03 LDSW_DIS Register ----Discharge Resistor Selection. Default = 0x3F

Each LDSW regulators output discharge resistor enable control.

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	Rev.	0	R	Reserved
5	ldsw6_dis	1	R/W	LDSW6 Discharge Enabled/Disabled control : 0b: Disable Pull down will not be activated when LDSW6 is disabled by any event 1b: Enable Pull down will be activated when LDSW6 is disabled by EN going low or ldsw6_en=0 or a Sequenced shutdown
4	ldsw5_dis	1	R/W	LDSW5 Discharge Enabled/Disabled control : 0b: Disable Pull down will not be activated when LDSW5 is disabled by any event 1b: Enable Pull down will be activated when LDSW5 is disabled by EN going low or ldsw5_en=0 or a Sequenced shutdown
3	ldsw4_dis	1	R/W	LDSW4 Discharge Enabled/Disabled control : 0b: Disable Pull down will not be activated when LDSW4 is disabled by any event 1b: Enable Pull down will be activated when LDSW4 is disabled by EN going low or ldsw4_en=0 or a Sequenced shutdown
2	ldsw3_dis	1	R/W	LDSW3 Discharge Enabled/Disabled control : 0b: Disable Pull down will not be activated when LDSW3 is disabled by any event 1b: Enable Pull down will be activated when LDSW3 is disabled by EN going low or ldsw3_en=0 or a Sequenced shutdown
1	ldsw2_dis	1	R/W	LDSW2 Discharge Enabled/Disabled control : 0b: Disable Pull down will not be activated when LDSW2 is disabled by any event 1b: Enable Pull down will be activated when LDSW2 is disabled by

				EN going low or ldsw2_en=0 or a Sequenced shutdown
0	ldsw1_dis	1	R/W	LDSW1 Discharge Enabled/Disabled control : 0b: Disable Pull down will not be activated when LDSW1 is disabled by any event 1b: Enable Pull down will be activated when LDSW1 is disabled by EN going low or ldsw1_en=0 or a Sequenced shutdown

0x04/09H LDSW_TR0/1 Register ----Load Switch output voltage rise timing Selection.
Default = 0x00

V_{INX} =3.3V, R_L=150Ω, C_L=0.1μF

Bit	Name	Default	Type	Description
7	Rev.	00/00	R	Reserved
6	Rev.	00/00	R	Reserved
5	ldsw6_tr1 ldsw6_tr0	00	R/W	LDSW6 output voltage (from 10% to 90%) rise time setting control : 00b: 340us 01b: 32us 10b: 150us 11b: 1000us
4	ldsw5_tr1 ldsw5_tr0	00	R/W	LDSW5 output voltage (from 10% to 90%) rise time setting control : 00b: 340us 01b: 32us 10b: 150us 11b: 1000us
3	ldsw4_tr1 ldsw4_tr0	00	R/W	LDSW4 output voltage (from 10% to 90%) rise time setting control : 00b: 340us 01b: 32us 10b: 150us 11b: 1000us
2	ldsw3_tr1 ldsw3_tr0	00	R/W	LDSW3 output voltage (from 10% to 90%) rise time setting control : 00b: 340us 01b: 32us 10b: 150us 11b: 1000us
1	ldsw2_tr1 ldsw2_tr0	00	R/W	LDSW2 output voltage (from 10% to 90%) rise time setting control : 00b: 340us 01b: 32us 10b: 150us 11b: 1000us
0	ldsw1_tr1 ldsw1_tr0	00	R/W	LDSW1 output voltage (from 10% to 90%) rise time setting control : 00b: 340us 01b: 32us 10b: 150us 11b: 1000us

0x05 LDSW12_SEQ Register ---- Power sequence setting register. Default = 0x00

Power sequence setting register. there are 7 time slots defined as following table. The power-up sequence is start from slot1 to slot7, and shut down start from slot7 to slot1. Power-up and shut down of LDSW1/2 regulator can be set at any one of the slots.

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Type</th><th>Description</th></tr>
<tr><td>7:6</td><td>Rev.</td><td>00</td><td>R</td><td>Reserved</td></tr>
<tr><td>5:3</td><td>ldsw2_seq[2:0]</td><td>000</td><td>R/W</td><td>LDSW2 Control select table
<table>
<tr><th>ldsw2_seq[2:0]</th><th>VOUT2</th></tr>
<tr><td>000</td><td>Controlled by I²C register ldsw2_en</td></tr>
<tr><td>001</td><td>Slot1</td></tr>
<tr><td>010</td><td>Slot2</td></tr>
<tr><td>011</td><td>Slot3</td></tr>
<tr><td>100</td><td>Slot4</td></tr>
<tr><td>101</td><td>Slot5</td></tr>
<tr><td>110</td><td>Slot6</td></tr>
<tr><td>111</td><td>Slot7</td></tr>
</table></td></tr>
<tr><td>2:0</td><td>ldsw1_seq[2:0]</td><td>000</td><td>R/W</td><td>LDSW1 Control select table
<table>
<tr><th>ldsw1_seq[2:0]</th><th>VOUT1</th></tr>
<tr><td>000</td><td>Controlled by I²C register ldsw1_en</td></tr>
<tr><td>001</td><td>Slot1</td></tr>
<tr><td>010</td><td>Slot2</td></tr>
<tr><td>011</td><td>Slot3</td></tr>
<tr><td>100</td><td>Slot4</td></tr>
<tr><td>101</td><td>Slot5</td></tr>
<tr><td>110</td><td>Slot6</td></tr>
<tr><td>111</td><td>Slot7</td></tr>
</table></td></tr>
</table>

0x06 LDSW34_SEQ Register ---- Power sequence setting register. Default = 0x00

Power sequence setting register. there are 7 time slots defined as following table. The power-up sequence is start from slot1 to slot7, and shut down start from slot7 to slot1. Power-up and shut down of each LDSW3/4 regulator can be set at any one of the slots.

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Type</th><th>Description</th></tr>
<tr><td>7:6</td><td>Rev.</td><td>00</td><td>R</td><td>Reserved</td></tr>
<tr><td>5:3</td><td>ldsw4_seq[2:0]</td><td>000</td><td>R/W</td><td>LDSW4 Control select table
<table>
<tr><th>ldsw4_seq[2:0]</th><th>VOUT4</th></tr>
<tr><td>000</td><td>Controlled by I²C register ldsw4_en</td></tr>
<tr><td>001</td><td>Slot1</td></tr>
<tr><td>010</td><td>Slot2</td></tr>
<tr><td>011</td><td>Slot3</td></tr>
<tr><td>100</td><td>Slot4</td></tr>
<tr><td>101</td><td>Slot5</td></tr>
<tr><td>110</td><td>Slot6</td></tr>
<tr><td>111</td><td>Slot7</td></tr>
</table></td></tr>
<tr><td>2:0</td><td>ldsw3_seq[2:0]</td><td>000</td><td>R/W</td><td>LDSW3 Control select table
<table>
<tr><th>ldsw3_seq[2:0]</th><th>VOUT3</th></tr>
<tr><td>000</td><td>Controlled by I²C register ldsw3_en</td></tr>
<tr><td>001</td><td>Slot1</td></tr>
<tr><td>010</td><td>Slot2</td></tr>
<tr><td>011</td><td>Slot3</td></tr>
<tr><td>100</td><td>Slot4</td></tr>
<tr><td>101</td><td>Slot5</td></tr>
<tr><td>110</td><td>Slot6</td></tr>
<tr><td>111</td><td>Slot7</td></tr>
</table></td></tr>
</table>

0x07 LDSW56_SEQ Register ---- Power sequence setting register. Default = 0x00

Power sequence setting register. there are 7 time slots defined as following table. The power-up sequence is start from slot1 to slot7, and shut down start from slot7 to slot1. Power-up and shut down of each LDSW5/6 regulator can be set at any one of the slots.

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Type</th><th>Description</th></tr>
<tr><td>7:6</td><td>Rev.</td><td>00</td><td>R</td><td>Reserved</td></tr>
<tr><td>5:3</td><td>ldsw6_seq[2:0]</td><td>000</td><td>R/W</td><td>LDSW6 Control select table
<table>
<tr><th>ldsw6_seq[2:0]</th><th>VOUT6</th></tr>
<tr><td>000</td><td>Controlled by I²C register ldsw6_en</td></tr>
<tr><td>001</td><td>Slot1</td></tr>
<tr><td>010</td><td>Slot2</td></tr>
<tr><td>011</td><td>Slot3</td></tr>
<tr><td>100</td><td>Slot4</td></tr>
<tr><td>101</td><td>Slot5</td></tr>
<tr><td>110</td><td>Slot6</td></tr>
<tr><td>111</td><td>Slot7</td></tr>
</table></td></tr>
<tr><td>2:0</td><td>ldsw5_seq[2:0]</td><td>000</td><td>R/W</td><td>LDSW5 Control select table
<table>
<tr><th>ldsw5_seq[2:0]</th><th>VOUT5</th></tr>
<tr><td>000</td><td>Controlled by I²C register ldsw5_en</td></tr>
<tr><td>001</td><td>Slot1</td></tr>
<tr><td>010</td><td>Slot2</td></tr>
<tr><td>011</td><td>Slot3</td></tr>
<tr><td>100</td><td>Slot4</td></tr>
<tr><td>101</td><td>Slot5</td></tr>
<tr><td>110</td><td>Slot6</td></tr>
<tr><td>111</td><td>Slot7</td></tr>
</table></td></tr>
</table>

0x08 SEQ_CTR Register ---- Power sequence setting and status register. Default = 0x00

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Type</th><th>Description</th></tr>
<tr><td>7:6</td><td>seq_speed[1:0]</td><td>00</td><td>R/W</td><td>Define the slot period as following:
<table>
<tr><th>Register Value</th><th>Slot period(ms)</th></tr>
<tr><td>00</td><td>0.5</td></tr>
<tr><td>01</td><td>1.0</td></tr>
<tr><td>10</td><td>1.5</td></tr>
<tr><td>11</td><td>2.0</td></tr>
</table></td></tr>
<tr><td>5:4</td><td>seq_ctrl[1:0]</td><td>00</td><td>W/C</td><td>Enables power-up or shut down of SEQ:
<table>
<tr><th>Register Value</th><th>Slot period(ms)</th></tr>
<tr><td>00</td><td>Default</td></tr>
<tr><td>01</td><td>Starts an LDSW power up sequence</td></tr>
<tr><td>10</td><td>Starts an LDSW shutdown sequence</td></tr>
<tr><td>11</td><td>Bit configuration is ignored</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td></td><td>Note: The bits will always clear immediately when written to and always read back 00.</td></tr>
<tr><td>3</td><td>seq_on</td><td>0</td><td>R</td><td>Indicates the activation signal of SEQ.
0b: Indicates that the sequencing is not in process
1b: Indicates that the sequencing is executing and somewhere between the start of slot 1 and the end of slot 7. The bit remains a 1 until slot 7 has completed at start-up or slot 1 has finished at shutdown, regardless of what slots are used.</td></tr>
<tr><td>2:0</td><td>seq_cnt[2:0]</td><td>000</td><td>R</td><td>Indicates the slot number of SEQ at the moment:
<table>
<tr><th>Register Value</th><th>SEQ Counter</th></tr>
<tr><td>000</td><td>Sequencing has completed or not started.</td></tr>
<tr><td>001</td><td>Indicates was in slot 1 during register read</td></tr>
<tr><td>010</td><td>Indicates was in slot 2 during register read</td></tr>
<tr><td>011</td><td>Indicates was in slot 3 during register read</td></tr>
<tr><td>100</td><td>Indicates was in slot 4 during register read</td></tr>
<tr><td>101</td><td>Indicates was in slot 5 during register read</td></tr>
<tr><td>110</td><td>Indicates was in slot 6 during register read</td></tr>
<tr><td>111</td><td>Indicates was in slot 7 during register read</td></tr>
</table></td></tr>
</table>

0x0A LDSW_RCB Register ----RCB Function Selection. Default = 0x00

This register enables the function blocking the current of load switch when the output voltage is higher than input.

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	Rev.	0	R	Reserved
5	ldsw6_rcb	0	R/W	LDSW6 reverse current blocking function: 0b:Disable 1b: Enable
4	ldsw5_rcb	0	R/W	LDSW5 reverse current blocking function: 0b:Disable 1b: Enable
3	ldsw4_rcb	0	R/W	LDSW4 reverse current blocking function: 0b:Disable 1b: Enable
2	ldsw3_rcb	0	R/W	LDSW3 reverse current blocking function: 0b:Disable 1b: Enable
1	ldsw2_rcb	0	R/W	LDSW2 reverse current blocking function: 0b:Disable 1b: Enable
0	ldsw1_rcb	0	R/W	LDSW1 reverse current blocking function: 0b:Disable 1b: Enable

0x0B LDSW_STA Register ----LDSW Status Register. Default = 0x00

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	Rev.	0	R	Reserved
5	ldsw6_sta	0	R	LDSW6 Status Bit: 0b:Turn off Status 1b: Turn on Status
4	ldsw5_sta	0	R	LDSW5 Status Bit: 0b:Turn off Status 1b: Turn on Status
3	ldsw4_sta	0	R	LDSW4 Status Bit: 0b:Turn off Status 1b: Turn on Status
2	ldsw3_sta	0	R	LDSW3 Status Bit: 0b:Turn off Status 1b: Turn on Status
1	ldsw2_sta	0	R	LDSW2 Status Bit: 0b:Turn off Status 1b: Turn on Status
0	ldsw1_sta	0	R	LDSW1 Status Bit: 0b:Turn off Status 1b: Turn on Status

0x69 SOFTRST_CTR Register ----Software Reset Signal. Default = 0x00

Write B0H to this register will be produced a reset signal, this signal will reset all the registers to the default value.

Bit	Name	Default	Type	Description
7:0	softrst_ctr	00H	R/W	Write B0H to this register will reset all the registers to default value, the read value always keep “00H”.

Absolute Maximum Ratings

Items		Rating	Unit
POWER IN/OUT Pins Voltage (IN1,IN2,IN34,IN56,OUT1,OUT2,OUT3.OUT4,OUT5,OUT6,VSYS)		-0.3 to 6.0	V
Other Pin Voltage		-0.3 to V_{SYS}+0.3	V
Each Load Switch Maximum Load Current		2.0	A
Maximum Power Consumption		1200	mW
Operating Junction Temperature		-40 to 150	ºC
Storage Temperature		-65 to 150	ºC
Lead Temperature (Soldering, 10 sec)		300	ºC
ESD	HMB	±2000	V
	CDM	±500	V

Electrical Characteristics

Unless otherwise noted , C_{VSYS}=1uF , T_A = -40 ºC ~85 ºC. Typical values are at. T_A=25 ºC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{VSYS}	VSYS Voltage Range		1.6		5.5	V
I_{Q_ON}	VSYS Current	Active mode: V_{EN}=V_{VSYS} and Enable chip by I^2C			1	μA
I_{Q_OFF}		V_{EN}=0V and V_{ADDR}=V_{SCL}=V_{SDA}=0 or V_{ADDR}=V_{SCL}=V_{SDA}=V_{VSYS}			1	μA
R_{EN}	EN pin pull down Resistance		8	12		MΩ
I_{EN}	EN Leakage	V_{EN}=5V			0.6	μA
V_{ENH}	EN Input Voltage High		1.4			V
V_{ENH1}	EN Input Voltage High	V_{SYS}=1.8V	1.1			V
V_{ENL}	EN Input Voltage Low				0.3	V
V_{I2CH}	SCL/SDA Input Voltage High		1.4			V
V_{I2CH1}	SCL/SDA Input Voltage High	V_{SYS}=1.8V	1.1			V
V_{I2CL}	SCL/SDA Input Voltage Low				0.3	V
V_{OL}	SDA Logic Low Output	3mA Sink			0.4	V
I_{I2C}	SCL/SDA Input Current	EN=0 and V_{SCL}=V_{SDA}=V_{VSYS} or V_{SCL}=V_{SDA}=0		0.1		uA
F_{SCL}	SCL Clock Frequency				400	kHz

Electrical Characteristics(Continued)

Unless otherwise noted, V_{IN1}= V_{IN2}= V_{IN34}= V_{IN56}=1.2 to 5.5V, T_A= -40 to +85ºC;
Typical values are at V_{INX} = 3.3V and T_A = 25ºC. V_{VSYS}=1.6V to 5.5V

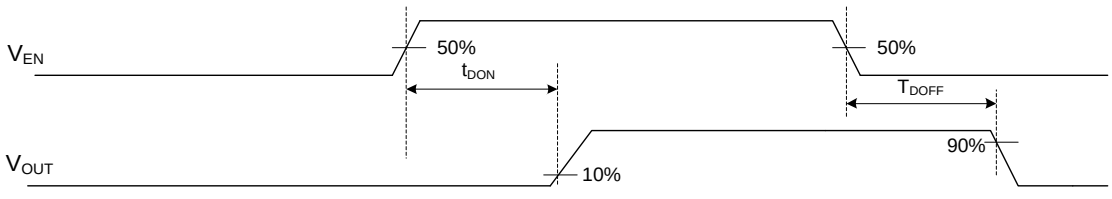
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Basic Operation						
V_{INX}	Input Voltage		1.2		5.5	V
$I_{QX(OFF)}$	Off Supply Current of one channel LS T_A=25ºC	V_{EN}=GND, V_{OUTX} floating, V_{INX}=5V			0.5	uA
		V_{EN} =GND, V_{OUTX} floating, V_{INX}=3.3V			0.5	
		V_{EN} =GND, V_{OUTX} floating, V_{INX}=1.8V			0.5	
I_{SD}	Shutdown Current of one channel LS T_A=25ºC	V_{EN} = GND, V_{OUTX}=0V, V_{INX}=5V			0.5	µA
		V_{EN} = GND, V_{OUTX}=0V, V_{INX}=3.3V			0.5	
		V_{EN} =GND, V_{OUTX}=0V, V_{INX}=1.8V			0.5	
I_Q	Quiescent Current of one channel LS T_A=25ºC（RCB off）	V_{EN} =V_{VSYS}, I_{OUTX}=0mA, V_{INX}=5 V			0.5	µA
		V_{EN} = V_{VSYS}, I_{OUTX}=0mA, V_{INX}=3.3V			0.5	
		V_{EN} = V_{VSYS}, I_{OUTX}=0mA, V_{INX}=1.8V			0.5	
I_{Q_R}	Quiescent Current of one channel LS T_A=25ºC(RCB on)	V_{EN} =V_{VSYS}, I_{OUTX}=0mA, V_{INX}=5 V		1.5	4	µA
		V_{EN} = V_{VSYS}, I_{OUTX}=0mA, V_{INX}=3.3V		0.9	2.5	
		V_{EN} = V_{VSYS}, I_{OUTX}=0mA, V_{INX}=1.8V		0.3	0.8	
R_{ON}	On-Resistance T_A=25ºC	V_{INX}=5V, I_{OUTX}=200mA		52	70	mΩ
		V_{INX}=3.3V, I_{OUTX}=200mA		66	85	
		V_{INX}=1.8V, I_{OUTX}=200mA		120	150	
R_{PD}	OUT pin Discharge Resistance（default）	V_{INX}= 3.3V, EN = 0V, V_{OUTX}=1V, T_A = 25°C		66	100	Ω
True Reverse Current Blocking						
V_{T_RCB}	RCB Protection Trip Point	V_{OUT} - V_{INX}		60		mV
V_{R_RCB}	RCB Protection Release Trip Point	V_{INX} - V_{OUT}		65		mV
	RCB Hysteresis			125		mV
I_{SD_OUT}	VOUT Shutdown Current	LSW off, V_{OUT}=5.0V, V_{IN} =Short to GND		1.4		uA
T_{RCB_ON}	RCB Response Time when Device ON(1)	V_{OUT} - V_{IN} =200mV, V_{ON}=High		3		uS
T_{RCB_OFF}	RCB Response Time Device OFF(1)	V_{IN} - V_{OUT} =200mV, V_{ON}=High		4		uS
Dynamic Characteristics: See Definitions Below（default mode）						
t_{DON}	Turn-On Delay(1,2)	V_{INX} =3.3V, R_L=150Ω, C_L=0.1µF,T_A=25℃		270		us
t_R	V_{OUT} Rise Time(1,2)			340		
t_{DON}	Turn-On Delay (1,2)	V_{INX} =3.3V, R_L=500Ω, C_L=0.1µF,T_A=25℃		250		
t_R	V_{OUT} Rise Time(1,2)			320		

t_{DOFF}	Turn-Off Delay (1,2)	V_{INX} =3.3V, R_L=150Ω,		0.8		us
t_F	V_{OUT} Fall Time(1,2)	C_L=0.1μF,T_A=25℃		10.5		
t_{DOFF}	Turn-Off Delay (1,2)	V_{INX} =3.3V, R_L=500Ω,		1.1		
t_F	V_{OUT} Fall Time(1,2)	C_L=0.1μF,T_A=25℃		14		
t_{DON}	Turn-On Delay(1,2)	V_{INX} =1.8V, R_L=150Ω,		560		us
t_R	V_{OUT} Rise Time(1,2)	C_L=0.1μF,T_A=25℃		560		
t_{DOFF}	Turn-Off Delay (1,2)	V_{INX} =1.8V, R_L=150Ω,		0.9		
t_F	V_{OUT} Fall Time(1,2)	C_L=0.1μF,T_A=25℃		12.6		

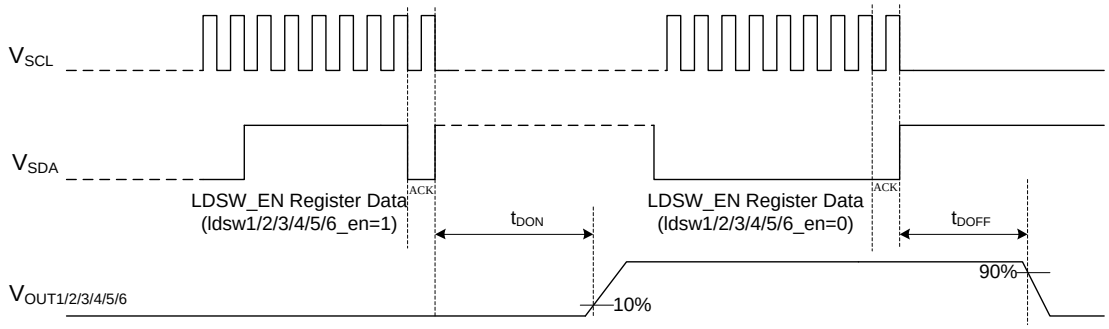
Notes:

1. This parameter is guaranteed by design and characterization; not production tested.
2. t_{DON} / t_{DOFF} / t_R / t_F are defined in Figure 3.

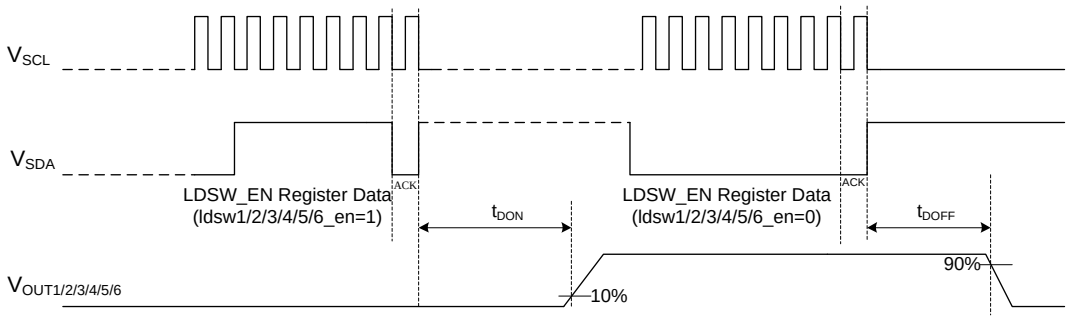
Timing Diagram



EN Pin Control V_{OUT} when LDSW_EN register had already enabled



EN Pin Control V_{OUT} when LDSW_EN register had already enabled



LDSW_EN register Control V_{OUT} when EN Pin had already set to high level

V_{OUT} T_R T_F Waveform

Figure 7.

I²C Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCL}	SCL Clock Frequency	0	-	400	KHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	1.3	-	-	μs
$t_{HD:STA}$	Hold Time(Repeated) START Condition	0.6	-	-	μs
t_{LOW}	Low Period of SCL Clock	1.3	-	-	μs
t_{HIGH}	HIGH Period of SCL Clock	0.6	-	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	0.6	-	-	μs
$t_{HD:DAT}$	Data Hold Time	-	-	0.9	μs
$t_{SU:DAT}$	Data Setup Time	100	-	-	ns
t_R	Data Hold Time2	20+0.1Cb(3)	-	300	ns
t_F	Data Hold Time2	20+0.1Cb(3)	-	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	0.6	-	-	μs

Note3: Cb=total capacitance of one bus line in PF.

I²C mode Timing Diagram

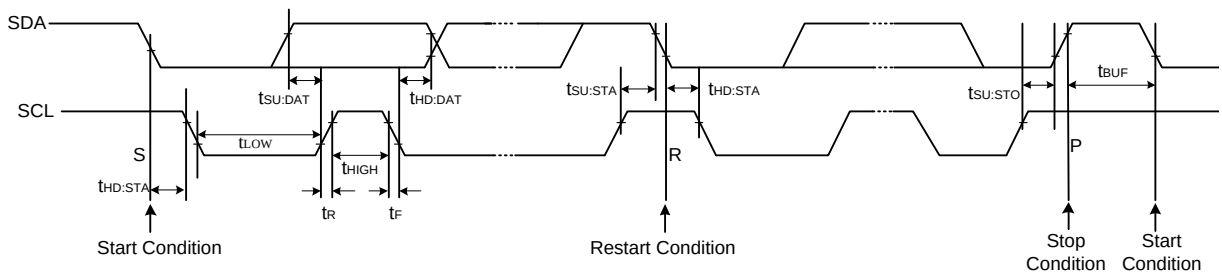
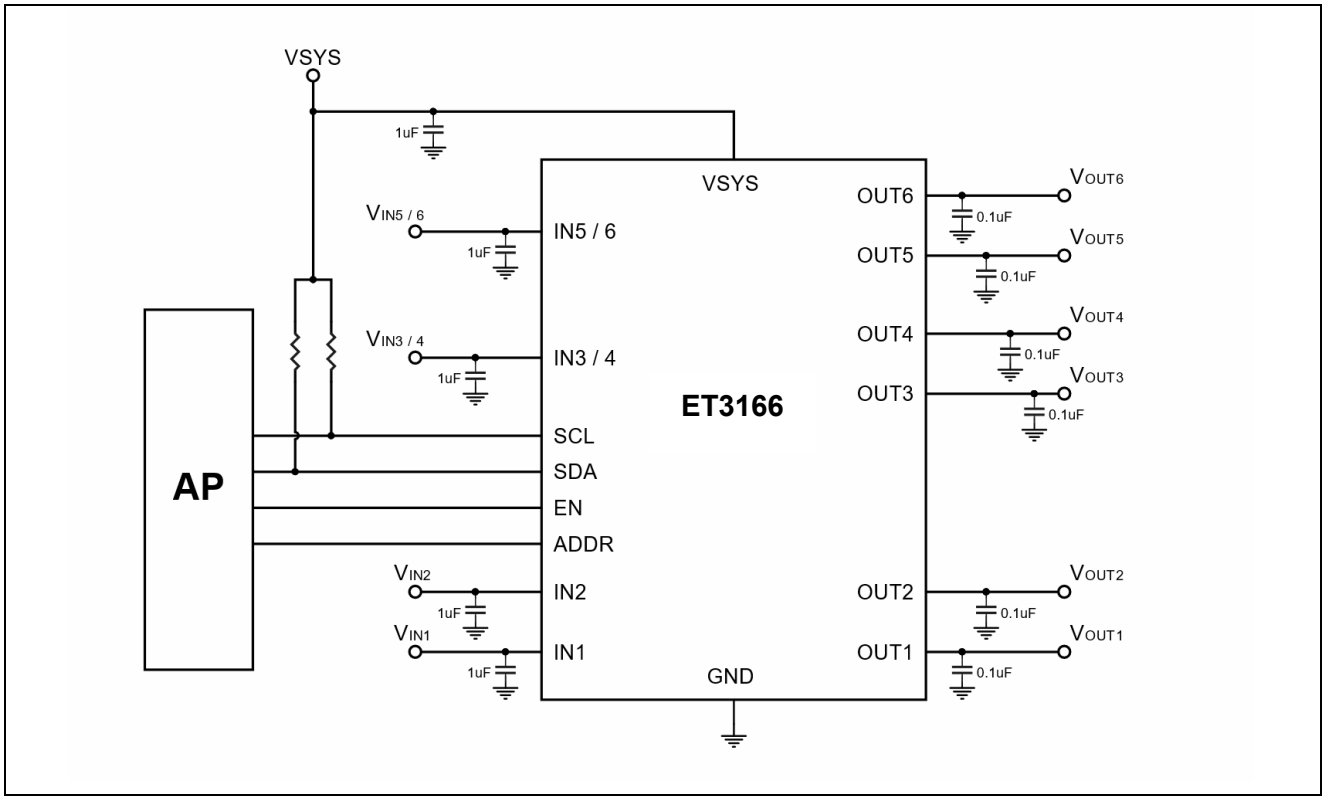


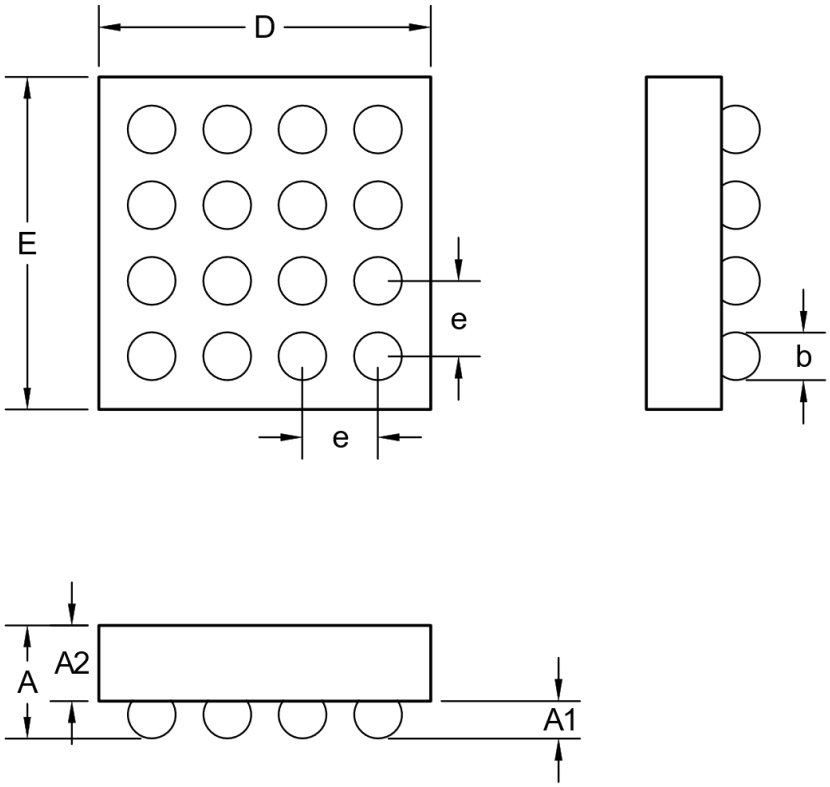
Figure 8.

Application Circuits



Package Dimension

WLCSP-16

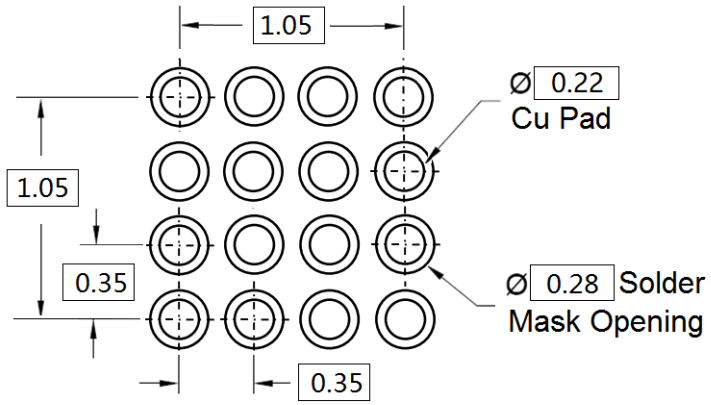


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.430	0.480	0.530
A1	0.110	0.130	0.150
A2	0.320	0.350	0.380
b	0.140	0.160	0.180
D	1.520	1.540	1.560
E	1.520	1.540	1.560
e	0.350BSC		

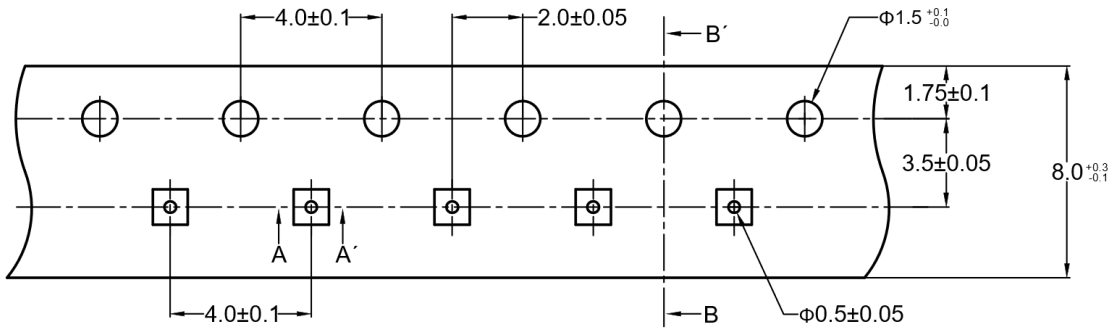
Recommended PCB Layout

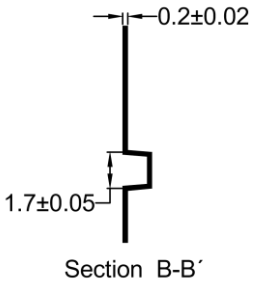


Recommended Land Pattern

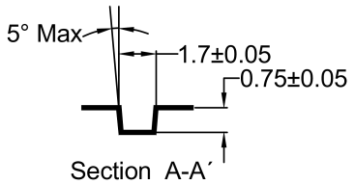
Unit: mm

Tape Information





Section B-B´



Section A-A´

Unit: mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2021-5-31	Initial Version	Wuxj	Wuxj	Liujy
1.1	2021-11-4	Add VIH@VSYS =1.8V	Wuxj	Wuxj	Liujy
1.2	2022-8-21	Update Typeset	ShiB	Wuxj	Liujy