# 0.4Ω Dual SPDT Negative Signal Handing Analog Switch

## General Description

The ET5228 is an advanced CMOS analog switch fabricated in Sub-micron silicon gate CMOS technology. The part also features guaranteed Break Before Make (BBM) switching, assuring the switches never short the driver. The switches can handle negative signal down to -2V.

ET5228 is offered QFN10L and MSOP10 package, which is ideal for small form factor portable equipment .

## Features

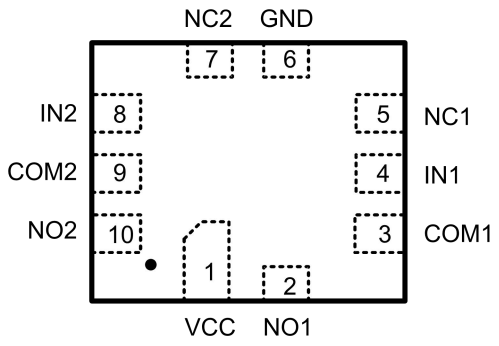
- Low $R_{ON}$ is typical 0.4Ω @ $V_{CC}$ =3.3V
- Single supply operation from 1.65V to 5.5V
- Full -2V to $V_{CC}$ signal handling capability
- High off-channel isolation
- Very low standby current
- Very low distortion
- Break-Before-Make(BBM) switching
- High continuous current capability is ±300mA through each switch
- Package information:

| Part No. | Package | MSL |
|---|---|---|
| ET5228 | QFN10L (1.8mm×1.4mm) | Level 1 |
| ET5228M | MSOP10 | Level 1 |

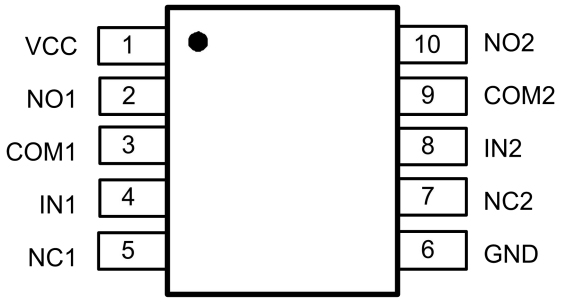
## Application

- Smart Phones and Cellular Phones
- Cell Phone Audio Block/ Speaker
- Earphone Switching Ring-Tone Chip
- Amplifier Switching/Modems

## Pin Configuration




ET5228 (QFN10L)




ET5228M (MSOP10)

TOP VIEW

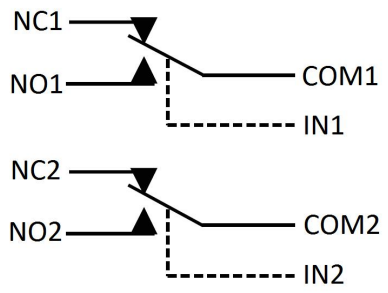
## Pin Function

| Pin NO. | Pin Name | Description |
|---|---|---|
| 1 | VCC | Power supply |
| 2 | NO1 | Independent Channels |
| 3 | COM1 | Common Channels |
| 4 | IN1 | Controls |
| 5 | NC1 | Independent Channels |
| 6 | GND | Ground (V) |
| 7 | NC2 | Independent Channels |
| 8 | IN2 | Controls |
| 9 | COM2 | Common Channels |
| 10 | NO2 | Independent Channels |

## Truth Table

| IN1/2 | NO1/2 to COM1/2 | NC1/2 to COM1/2 |
|---|---|---|
| 0 | OFF | ON |
| 1 | ON | OFF |

## Analog Symbol




Analog Symbol

## Absolute Maximum Ratings

| Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | -0.5～+6.5 | V |
| Analog Input Voltage | | $V_{IS}$ | -2.5～$V_{CC}$+0.3<br>$\|V_{CC}-V_{IS}\|$ <6.5V | V |
| Digital Select Input Voltage | | $V_{IN}$ | -0.5～+6.5 | V |
| Output Voltage | | $V_O$ | -2.5～$V_{CC}$+0.3<br>$\|V_{CC}-V_O\|$ <6.5V | V |
| Continuous DC Current from COM to NC/NO | | $I_{AN1}$ | ±300 | mA |
| Peak Current from COM to NC/NO, 10 duty cycle (1) | | $I_{AN-PK1}$ | ±500 | mA |
| Continuous DC Current into COM/NO/NC with respect to $V_{CC}$ | | $I_{CLMP}$ | ±100 | mA |
| Maximum Junction Temperature | | $T_{J(MAX)}$ | 150 | °C |
| Storage Temperature | | $T_S$ | -55 to 150 | °C |
| ESD | Human Body Model | HBM | ±6000 | V |
| | Charge-Device Mode | CDM | ±1500 | V |
| Latch Up (Current Maximum Rating) | | $I_{LU}$ | 200 | mA |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

***Note1***.Defined as 10% ON, 90% off duty cycle.

## Recommended Operating Conditions

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC Supply Voltage | $V_{CC}$ | 1.65 | 5.5 | V |
| Digital Select Input Voltage | $V_{IN}$ | GND | 5.5 | V |
| Analog Input Voltage | $V_{IS}$ | -2 | VCC | V |
| Operating Temperature Range | $T_A$ | -40 | +85 | °C |
| Input Rise or Fall Time, SELECT | tr, tf<br>$V_{CC}$=1.6V~2.7V<br>$V_{CC}$=3.0V~5.5V | <br>0<br>0 | <br>20<br>10 | ns/V |

## Electrical Characteristics

| Symbol | Parameter | Test Conditions | | $T_A$=25°C | | | $T_A$=-40~85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | High-Level Input Voltage, Select Inputs | $V_{CC}$ = 1.65~5.5 | 1.65 | 0.9 | | | 1.0 | | V |
| | | | 3.3 | 1.6 | | | 1.7 | | |
| | | | 5.5 | 2.2 | | | 2.3 | | |
| $V_{IL}$ | Low-Level Input Voltage, Select Inputs | $V_{CC}$= 1.65~5.5 | 1.65 | | | 0.4 | | 0.35 | V |
| | | | 3.3 | | | 0.5 | | 0.45 | |
| | | | 5.5 | | | 0.6 | | 0.55 | |
| $I_{IN}$ | Maximum Input Leakage Current, Select Inputs | $V_{IN}$ =$V_{CC}$ or GND<br>$V_{CC}$ =5.5V | | | | ±0.3 | | ±1.0 | uA |
| $I_{OFF}$ | Power Off Leakage Current | $V_{IN}$ =5.5V<br>$V_{CC}$ =0V | | | | ±0.5 | | ±1.0 | uA |
| $I_{CC}$ | Maximum Quiescent Supply Current (2) | $V_{CC}$ =5.5V, $I_{OUT}$ =0<br>$V_{IN}$ = $V_{CC}$ or GND | | | | ±0.5 | | ±1.0 | uA |
| $I_{CCT}$ | Increase in $I_{CC}$ per Input | IN1=2.6V, IN2=0V, or IN2=2.6V, IN1=0V,<br>$V_{CC}$ =4.3V | | | 1.5 | 3.0 | | 10 | uA |
| | | IN1=1.8V, IN2=0V, or IN2=1.8V, IN1=0V,<br>$V_{CC}$ =4.3V | | | 4.5 | 7.0 | | 20 | |
| $I_{COM(ON)}$ | COM ON leakage Current (3) | $V_{IN}$ = $V_{IL}$ or $V_{IH.}$,<br>$V_{NO}$=0.3V or 4.7V<br>$V_{NC}$ floating<br>$V_{NC}$=0.3V or 4.7V<br>$V_{NO}$ floating<br>$V_{COM}$=0.3Vor 4.7V<br>$V_{CC}$ =5.5V | | -20 | | 20 | -100 | 100 | nA |
| $R_{ON}$ | On−Resistance (2) (3) | $I_{COM}$ = 20mA<br>$V_{IS}$=-0.5V~0.5V,<br>$V_{CC}$ =4.3V | | | 0.4 | 0.8 | | 1.0 | Ω |
| | | $I_{COM}$ = 20mA,<br>$V_{IS}$=-0.5V~0.5V,<br>$V_{CC}$ =3.3V | | | 0.5 | 1.0 | | 1.3 | |
| $R_{FLAT}$ | On−Resistance Flatness (2) (3) (5) | $I_{COM}$=20mA<br>$V_{IS}$=-0.5V~0.5V,<br>$V_{CC}$ =4.3V | | | | 0.4 | | 0.5 | Ω |
| $\Delta R_{ON}$ | On−Resistance Match Between Channels (2) (3) (4) | $I_{COM}$=20mA<br>$V_{IS}$=0.5V<br>$V_{CC}$ =4.3V | | | 0.1 | 0.2 | | 0.3 | Ω |

## Electrical Characteristics (Continued)

| Symbol | Parameter | Test Conditions | $T_A$=25°C | | | $T_A$=-40~85°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{ON}$ | Turn−On Time (2) (Figure 1) | $V_{IS}$=0.5V, $V_{CC}$ =2.5~3.3V | | 35 | 55 | | | ns |
| | | $V_{IS}$=0.5V, $V_{CC}$ =3.3~5.5V | | 25 | 45 | | | |
| $t_{OFF}$ | Turn−Off Time (2) (Figure 1) | $V_{IS}$=0.5V, $V_{CC}$ =2.5~3.3V | | 26 | 50 | | | ns |
| | | $V_{IS}$=0.5V, $V_{CC}$ =3.3~5.5V | | 20 | 40 | | | |
| $t_{BBM}$ | Break-Before-Make Time (2) (Figure 2) | $C_L$=35pF, $R_L$=50Ω $V_{IS}$=0.5V, $V_{CC}$ =2.5~3.3V | | 15 | | 7 | | ns |
| | | $C_L$=35pF, $R_L$=50Ω $V_{IS}$=0.5V, $V_{CC}$ =3.3~5.5V | | 7 | | 3 | | |
| BW | On-Channel -3dB Bandwidth or Frequency Response (2) (Figure 4) | $R_{IS}$=50Ω | | 65 | | | | MHz |
| $V_{ISO}$ | Off−Channel Isolation (2) (Figure 5) | $F_{IS}$ = 100kHz, $V_{IN}$ =GND to $V_{CC}$ $C_L$=5pF， $R_L$= 50Ω $V_{IS}$=1V $V_{PP}$ | | -65 | | | | dB |
| Q | Charge Injection Select Input to Common I/O (2) (Figure 3) | $V_{IN}$ = 0 or $V_{CC}$ $R_{IS}$=0Ω,$C_L$=100pF $R_L$=1MΩ $Q=C_L \times \Delta V_{OUT}$ | | 25 | | | | pC |
| THD | Total Harmonic Distortion THD +Noise (4) | $F_{IS}$=20Hz to 20KHz $R_L$=50Ω,$C_L$=5pF $V_{IS}$=2V RMS $V_{CC}$ =3.6V | | 0.06 | | | | % |
| $V_{CT}$ | Channel−to−Channel Crosstalk (2) (Figure 6) | $F_{IS}$= 100KHz, $V_{IN}$ =GND to $V_{CC}$ $R_L$= 50Ω,$C_L$=5pF $V_{IS}$=1V $V_{PP}$ | | -90 | | | | dB |

## Electrical Characteristics (Continued)

| Symbol | Parameter | Test Conditions | $T_A$=25°C | | | $T_A$=-40~85°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $C_{IN}$ | Control Pin Input Capacitance (2) | $V_{CC}$ =3.6V | | 4.5 | | | | pF |
| $C_{NC}/C_{NO}$ | NC/NO Port Capacitance (2) | $V_{CC}$ =3.6V | | 15.0 | | | | pF |
| $C_{COM}$ | COM Port Capacitance When Switch is Enabled (2) | $V_{CC}$ =3.6V | | 56.0 | | | | pF |

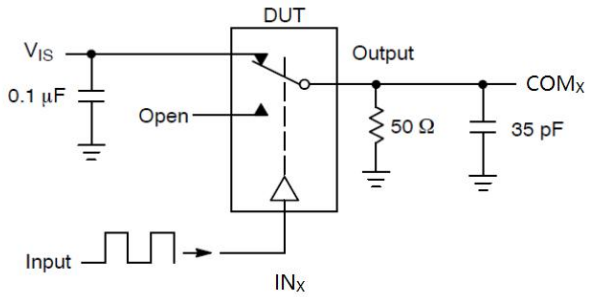
***Note2***. Guaranteed by design

***Note3***. Guaranteed by design. Resistance measurements do not include test circuit or package resistance

***Note4***. $\Delta R_{ON} = R_{ON(NC1)} - R_{ON(NC2)}$ or $R_{ON(No1)} - R_{ON(No2)}$ when $V_{IS}$ is same.

***Note5***. Flatness is defined as the difference between the maximum and minimum value of on−resistance as measured over the specified analog signal ranges.

## Test Circuit



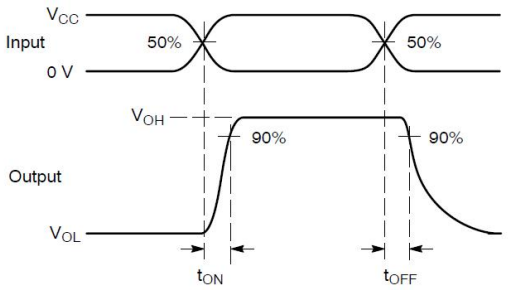
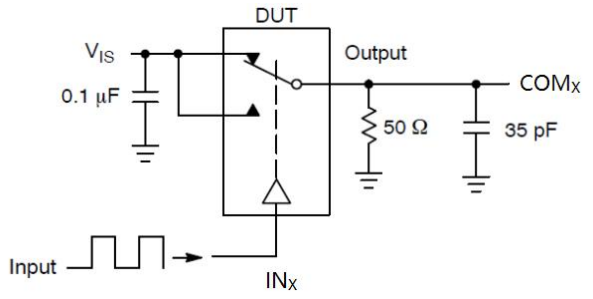




Figure1. $t_{ON}$ /$t_{OFF}$



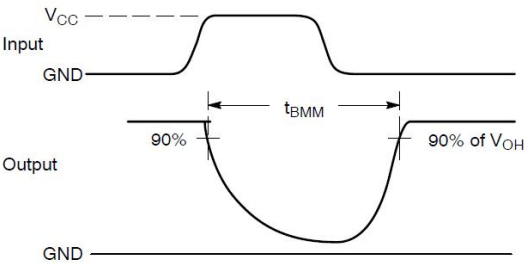
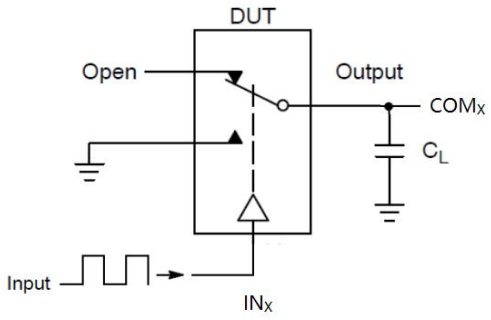




Figure2. $t_{BBM}$



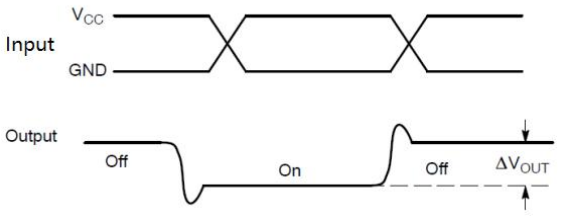




Figure3. Charge Injection

## Test Circuit (Continued)

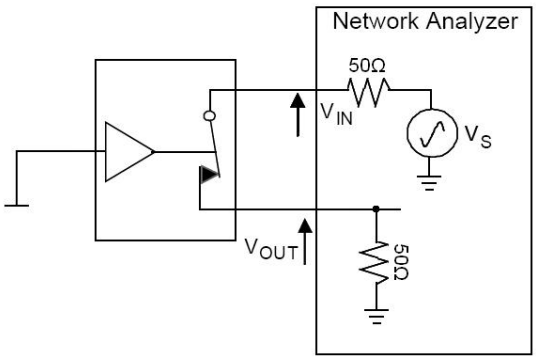



Figure4. Bandwidth

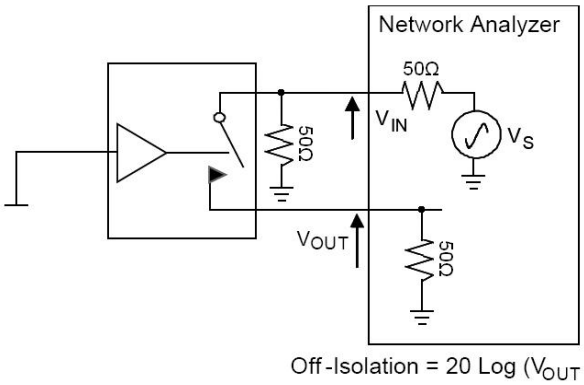



Figure5. Channel Off Isolation

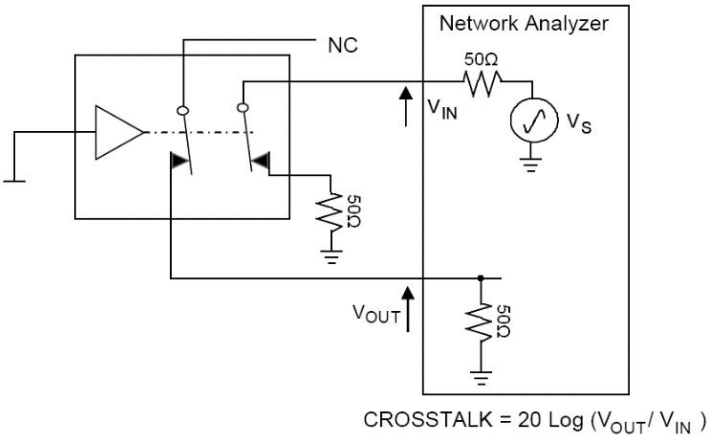
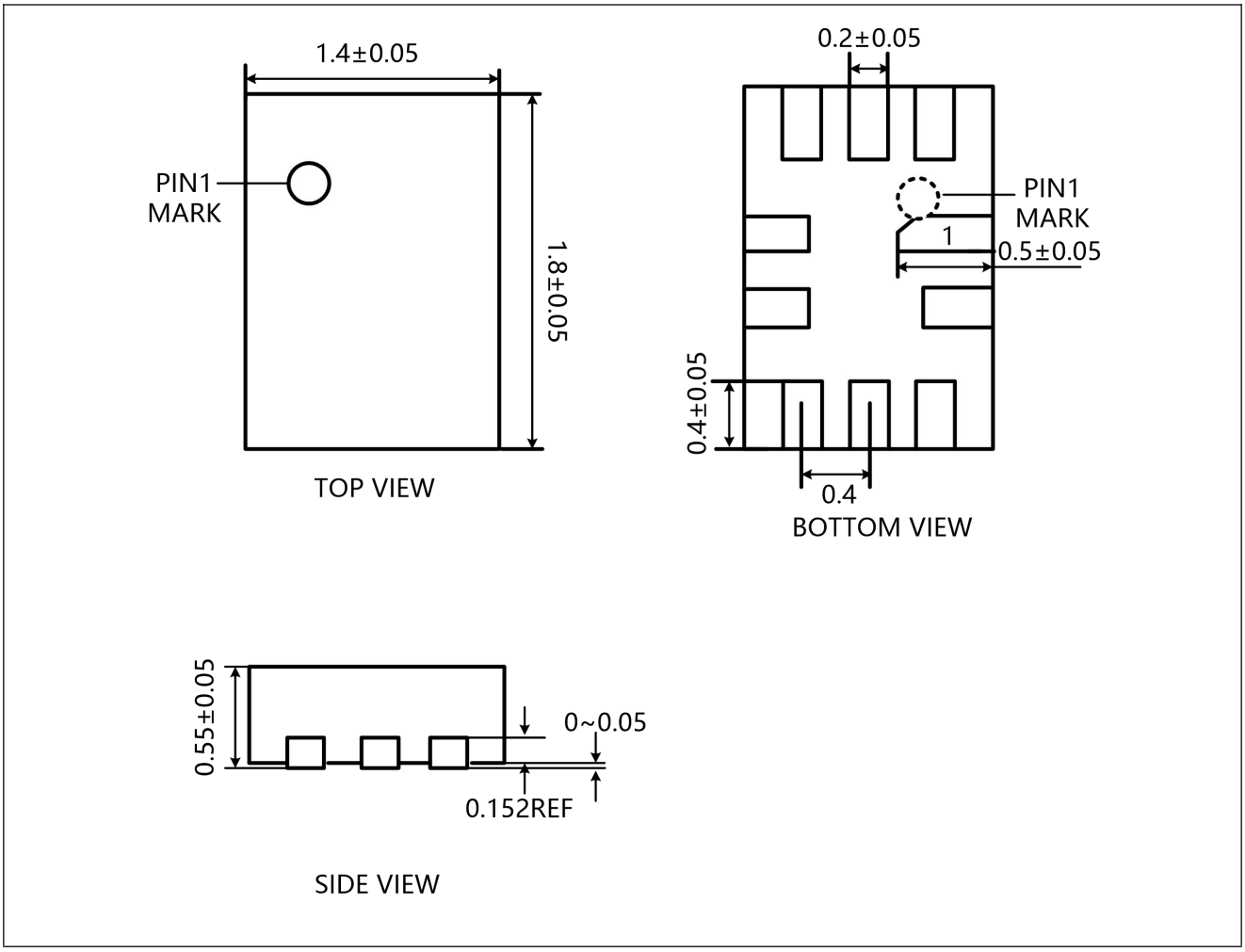



Figure6. Non-Adjacent Channel-to-Channel Crosstalk

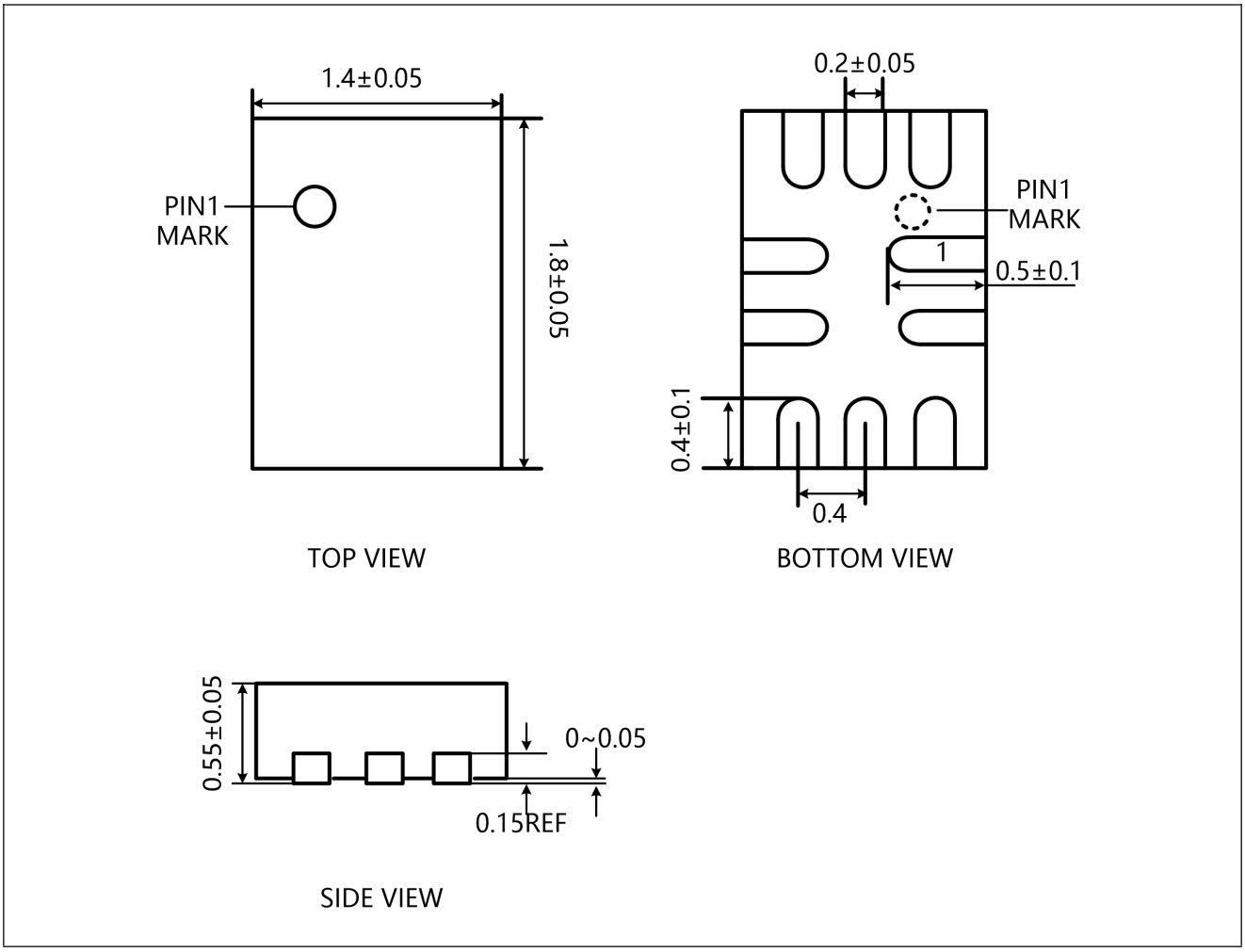
## Package Dimension

QFN10L(1)



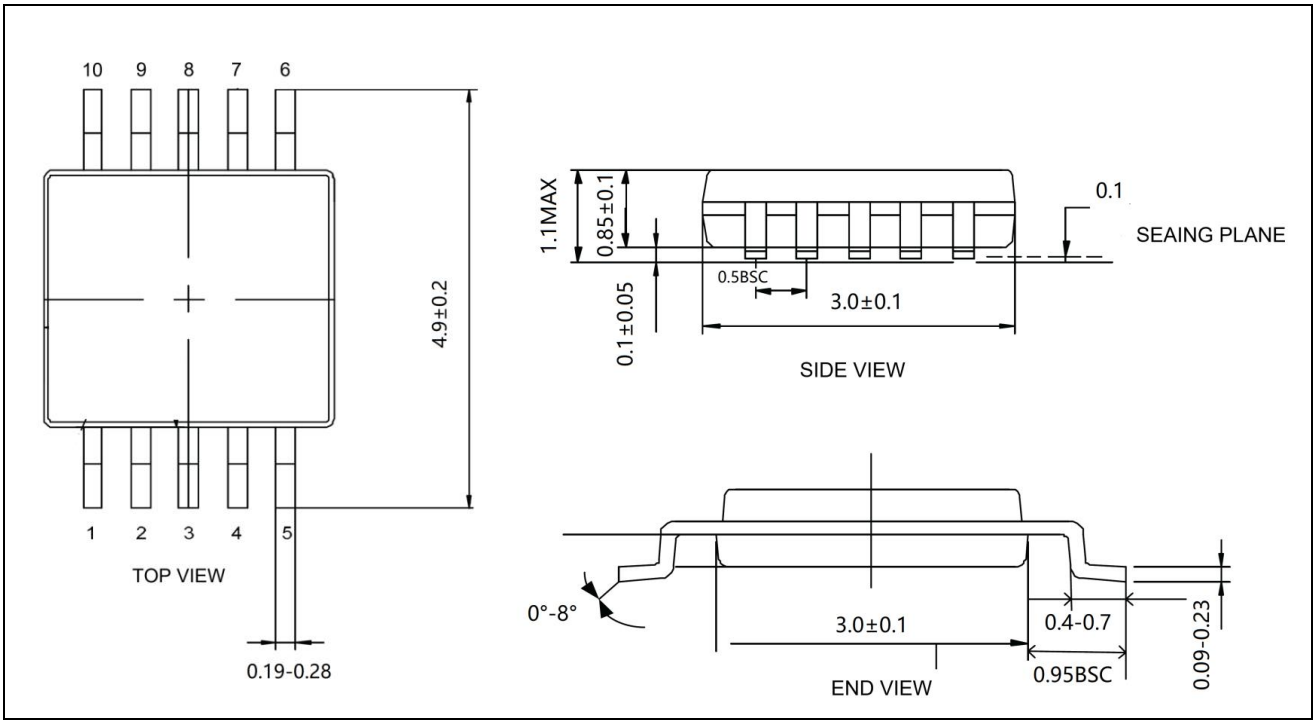
## Package Dimension(Continued)

QFN10L(2)

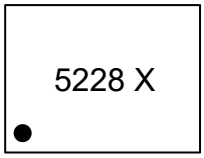


## Package Dimension(Continued)

MSOP10




## Marking Information




5228 - Part Number

X - Tracking Number

***Note***：X (Tracking Number) is variable, according to the wafer lot number.

## Revision History and Checking Table

| Version | Date | Revision Item | Modifier | Function & Spec Checking | Package & Tape Checking |
|---|---|---|---|---|---|
| 1.0 | 2015-08-18 | Original Version | Wuxj | Zhujl | Zhujl |
| 1.1 | 2018-06-25 | Add MSOP10 pin configuration | Wuxj | Liujy | Liujy |
| 1.2 | 2019-01-31 | Adjust test condition of DC characteristic | Wuxj | Liujy | Liujy |
| 1.3 | 2019-04-16 | Clear test condition of some item | Wuxj | Zhujl | Zhujl |
| 1.4 | 2020-03-13 | Documents check and formalize | Shib | Liujy | Liujy |
| 1.5 | 2022-08-12 | Update Typeset | Huyt, Yinp | Liujy | Liujy |
| | | | | | |