

Matrix LED Driver Control Special Circuit

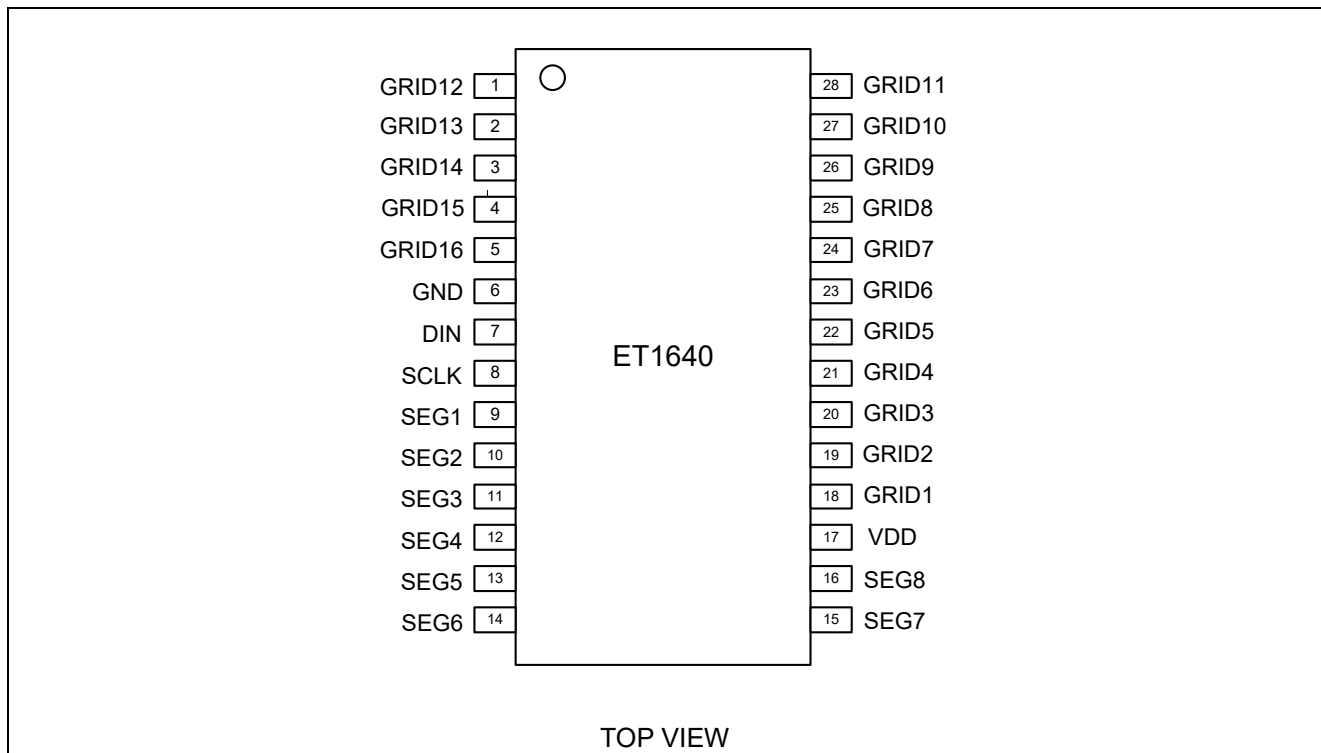
General Description

ET1640 is an matrix LED driver IC, it has 8 segment outputs and 16 grid outputs. It inherits MCU digital interface, data latch and LED driver module. It is suitable for small LED display driver.

Features

- Display mode: 8 SEGs × 16 Grids
- Global brightness adjustment : 8 step
- Two wire serial interface
- Built in RC oscillation
- Built in power on reset
- Package is SOP28

Pin Assignments



ET1640

Pin Description

Symbol	Pin No.	Description
DIN	7	Serial data input port
SCLK	8	Serial clock input port
SEG1~SEG8	9~16	Segment output port, connect to LED positive pole
GRID1~GRID11 GRID12~GRID16	18~28 1~5	Grid output port, connect to LED negative pole
VDD	17	Power supply port
GND	6	Ground

Functions Description

1. Display Register Address and Display Mode

This registers stores the data transferred from external device to ET1640 through serial interface, and the address is from 00H -0FH , which is total 16 byte unit. It corresponds to the LED connected to SEG and GRID pins respectively. When writing LED display data, it operates from low bit to high bit of display address and from low bit to high bit of digital byte.

The Display registers format is as following:

SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	
XXHL (Low four bits)				XXHU (High four bits)				
B0	B1	B2	B3	B4	B5	B6	B7	
00HL				00HU				GRID1
01HL				01HU				GRID2
02HL				02HU				GRID3
03HL				03HU				GRID4
04HL				04HU				GRID5
05HL				05HU				GRID6
06HL				06HU				GRID7
07HL				07HU				GRID8
08HL				08HU				GRID9
09HL				09HU				GRID10
0AHL				0AHU				GRID11
0BHL				0BHU				GRID12
0CHL				0CHU				GRID13
0DHL				0DHU				GRID14
0EHL				0EHU				GRID15
0FHL				0FHU				GRID16

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2. Instruction introduction

The user sets the display mode and LED driving state with the command. After the instruction start is valid, the first byte input by DIN is regarded as an instruction, after decoding, the highest B7 and B6 bits are selected to distinguish instruction.

B7	B6	Instruction
0	1	Data command setup
1	0	Display control command setup
1	1	Address command setup

If end is valid during instruction or data transmission, serial communication is initialized and the instruction or data being transmitted is invalid.

Configure Command Register settings

This instruction is used to set the data write and read, B1 and B0 bits are not allowed to set 01 or 11.

MSB

LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
0	1	Irrelevant items, fill in 0				0	0	Data read/write mode setting	Write data into Register.
0	1				0			Address increase mode setting	Automatic address increase
0	1				1				Fixed address
0	1			0				Test mode setting	Normal mode
0	1			1					Test mode

Display Address Command Setting

B7	B6	B5	B4	B3	B2	B1	B0	Display Address
1	1	Irrelevant items, fill in 0		0	0	0	0	00H
1	1			0	0	0	1	01H
1	1			0	0	1	0	02H
1	1			0	0	1	1	03H
1	1			0	1	0	0	04H
1	1			0	1	0	1	05H
1	1			0	1	1	0	06H
1	1			0	1	1	1	07H
1	1			1	0	0	0	08H
1	1			1	0	0	1	09H
1	1			1	0	1	0	0AH
1	1			1	0	1	1	0BH
1	1			1	1	0	0	0CH
1	1			1	1	0	1	0DH
1	1			1	1	1	0	0EH
1	1			1	1	1	1	0FH

This instruction is used to set the address of the display register.

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If the address is set to 10H or high, the data is ignored until the valid address is set. When power on, the address is 00H by default.

Display Control

MSB

LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
1	0	Irrelevant items, fill in 0			0	0	0	Duty cycle setting	Duty cycle 1/16
1	0				0	0	1		Duty cycle 2/16
1	0				0	1	0		Duty cycle 4/16
1	0				0	1	1		Duty cycle 10/16
1	0				1	0	0		Duty cycle 11/16
1	0				1	0	1		Duty cycle 12/16
1	0				1	1	0		Duty cycle 13/16
1	0				1	1	1		Duty cycle 14/16
1	0			0				Display On/Off	Display ON
1	0			1					Display OFF

Interface Description

The data of MCU communicates with ET1640 through two_wire bus interface. When input data, when SCLK is high level, the signal on DIN must remain unchanged; only when the clock signal on SCLK is low level, the signal on DIN can be changed. The input of data is always low in the front and high in the back. The start condition of data input is that DIN changes from high to low when SCLK is high, and the end condition is that DIN changes from low to high when SCLK is high.

The instruction transmission format is as following :

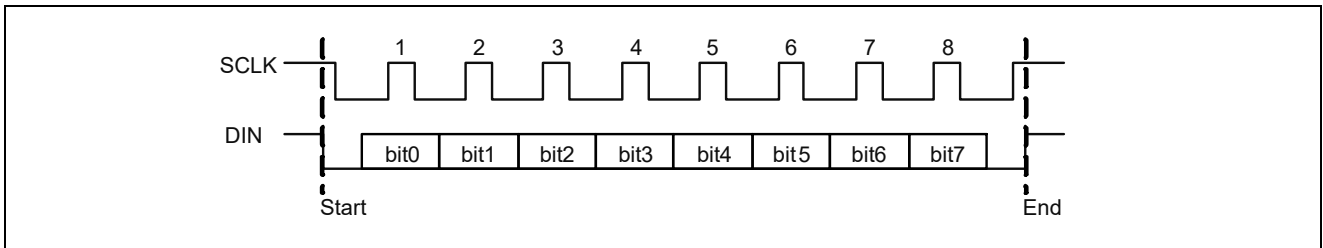


Figure 1. Instruction Transmission

Data address automatic increase mode

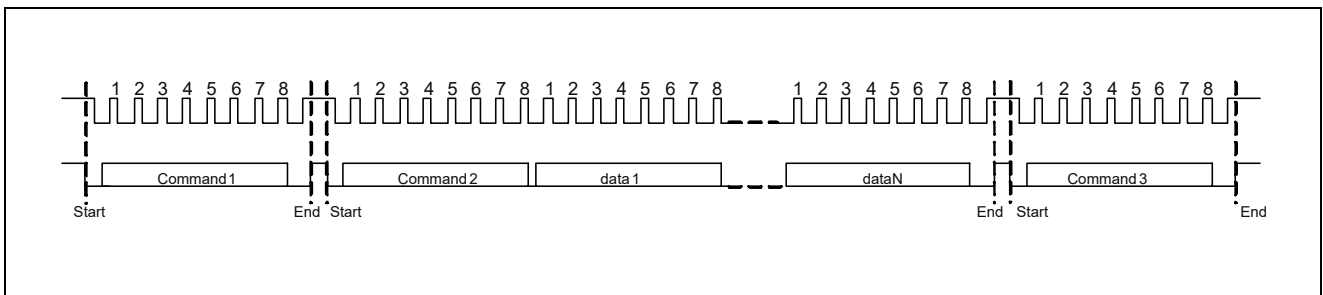


Figure 2. Automatic address write data mode

Command1: configure data command

Command2: configure address

data1~N: Transfer the display data to the address after the command2 address (up to 16bytes)

Command3: Display control command

Fixed Address Write Data Mode

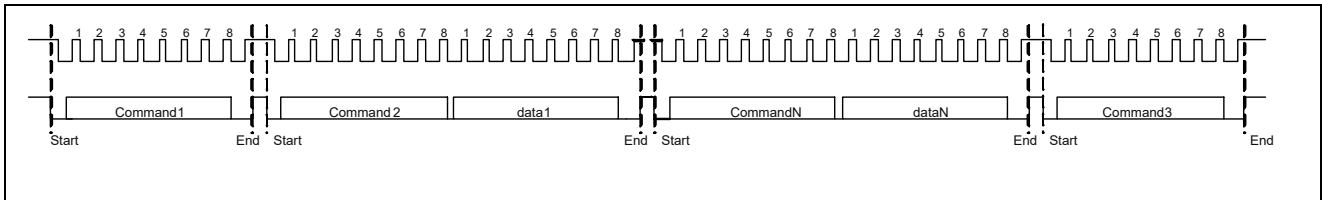


Figure 3. Fixed address write data mode

Command1: configure data command

Command2: configure display address

data1: Transfer the display data to the address after the command2 address

CommandN: configure display address

dataN: Transfer the display data to the address after the commandN address

Command3: Display control command

Display Cycle

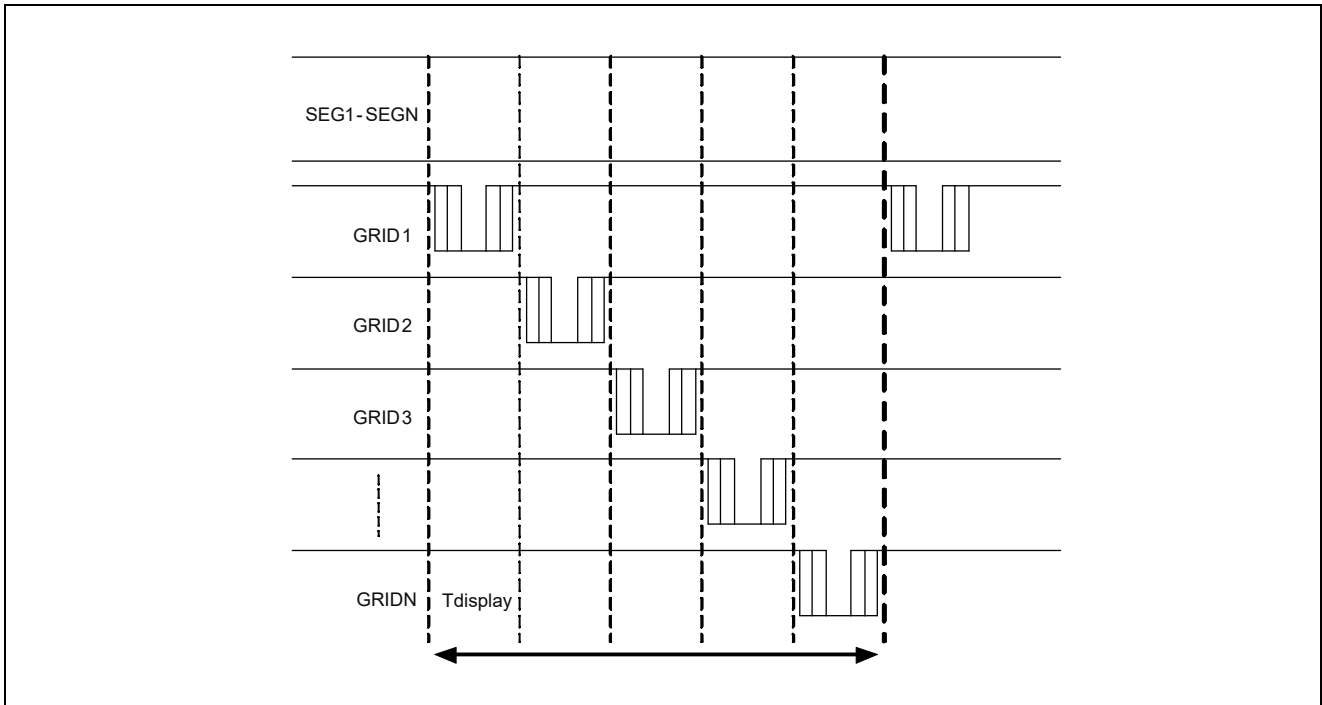


Figure 4. Data display cycle

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Absolute Maximum Ratings

Symbol	Characteristic	Condition	Rating	Unit
V _{DD}	Supply Voltage		-0.5~6.0	V
I _{O1}	SEG Output Current	V _{DD} =5V, T _A =25°C	-75	mA
I _{O2}	GRID Output Current	V _{DD} =5V, T _A =25°C	200	mA
P _D	Max Power Dissipation		400	mW
T _J	Junction Temperature		-40~150	°C
T _{STG}	Storage Temperature		-65~150	°C

Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V _{DD}	Supply Voltage	3.0	5.0	5.5	V
V _{IH}	Input High Voltage	0.7V _{DD}	-	V _{DD}	V
V _{IL}	Input Low Voltage	0	-	0.25V _{DD}	V
T _A	Operating Temperature	-40		+85	°C

Electrical Characteristics

(Unless otherwise noted, V_{DD}=5V, T_A=25°C)

Symbol	Characteristic	Test Condition	Min	Typ	Max	Unit
I _{SEG}	High Voltage Output current	V _{DD} =5V, V _O =V _{DD} -2V	-45	-50	-60	mA
		V _{DD} =5V, V _O =V _{DD} -3V	-60	-65	-75	mA
I _{GRID}	Low Voltage Output Current	V _O =V _{DD} -0.3V	80	140	-	mA
I _{IN}	Input current	V _I =V _{DD} / GND	-	-	±1	uA
V _{IH}	Input High Voltage	SCLK, DIN	0.7V _{DD}	-	-	V
V _{IL}	Input Low Voltage	SCLK, DIN	-	-	0.25V _{DD}	V
I _{DD_DYN}	Dynamic current deterioration	No Load, Display off	-	-	500	uA

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Switch Characteristics

(Unless otherwise noted, $V_{DD}=5V$, $T_A=25^{\circ}C$)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Transmission delay time	T_{PLZ}	SCLK→DIN	-	-	300	ns
	T_{PZL}	SCLK=15pF, RL=10K Ω		-	100	ns
Rising time	T_{TZH1}	SEG1~8, CL=300pF	-	-	2	us
	T_{TZH2}	GRID1~16, CL=300pF	-	-	0.5	us
Dropping time	T_{THZ}	CL=300pF, SEGn, GRIDn	-	-	120	us
Max clock Frequency	F_{MAX}	Duty=50%	-	-	1	MHz
Input capacitance	C_{IN}	-	-	-	15	pF

Timing Characteristics

(Unless otherwise noted, $V_{DD}=5V$, $T_A=25^{\circ}C$)

Symbol	Characteristic	Test Condition	Min	Unit
PW_{SCLK}	Clock Pulse Width	-	400	ns
T_{SETUP}	Data setup Time	-	100	ns
T_{HOLD}	Data Hold Time	-	100	ns
T_{WAIT}	Waiting Time	SCLK↑→SCLK↓	1	us

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Application Example

Connection principle of common cathode digital tube

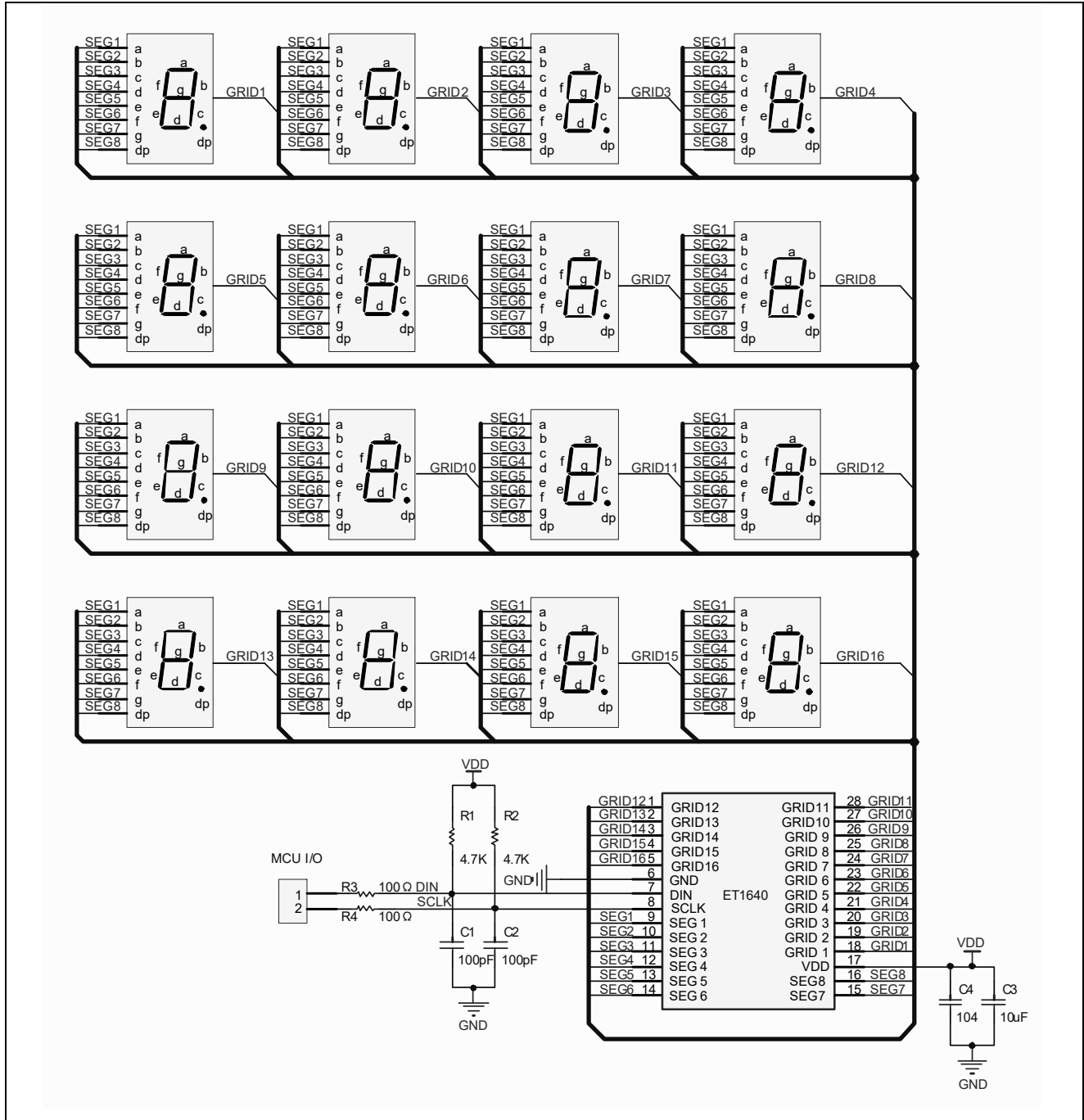


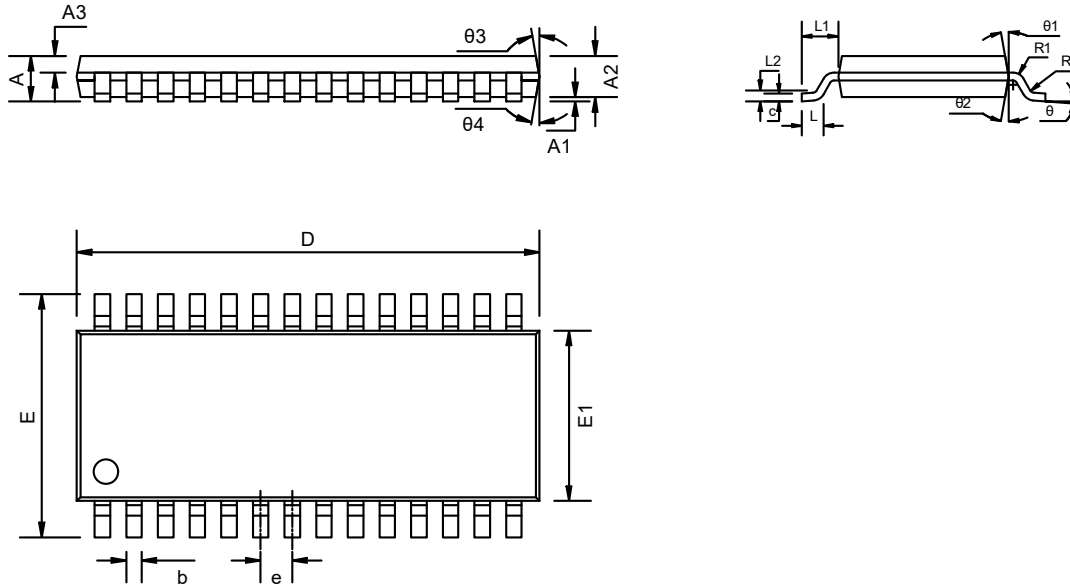
Figure 5. Schematic diagram of ET1640 driving common cathode digital tube

Resistance and capacitance parameters of circuit are for reference only.

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Package

SOP28



Dimensions Table (Units: mm)

Symbol	Min	Typ	Max
A	--	--	2.95
A1	0.10	0.20	0.30
A2	2.25	2.45	2.65
A3	1.20	1.30	1.40
b	0.41	--	0.54
c	0.15	--	0.20
D	17.40	17.50	17.60
E	10.20	10.40	10.60
E1	7.50	7.60	7.70
e	1.27 BSC		
L	0.40	0.60	0.80
L1	1.30 REF		
L2	0.25 BSC		
R	0.10	--	--
R1	0.10	--	--
θ	0°	--	8°
θ_1	13°	15°	17°
θ_2	6°	8°	10°
θ_3	9.5°	11.5°	13.5°
θ_4	6°	8°	10°

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Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2018-01-19		ShiLiangJun	ShiLiangJun	ZhuJunLi
1.1	2018-12-07	Parameter adjustment	ShiLiangJun	ShiLiangJun	ZhuJunLi
1.2	2021-3-18	Update Graph and spec	ShiLiangJun	ShiLiangJun	ZhuJunLi
1.3	2022-08-31	Update Typeset	Shibo	ShiLiangJun	ZhuJunLi
1.4	2023-3-8	VIL to 0.25VDD	Shibo		
1.5	2024-2-9	IDD_DYN change to 500uA max	Shibo	Licx	Liujy