Low-Voltage 500mA LDO

General Description

The ET540XX Series are low voltage 500mA voltage regulator. The input voltage is as low as Min. 1.1V and the output voltage can be set from 0.7V. The output voltage accuracy has been improved to ±0.8% and due to a built-in transistor with low on-resistance. Each of these ICs consists of a voltage reference unit, an error amplifier, a resistor-net for voltage setting, and a current limit circuits for over-current for the destruction prevention by the over-current.

The ET540XX series use a type of outstanding CMOS process to minimize the supply current. A low on-resistance PMOS pass device is equipped for lower dropout voltage. ET540XX also possess the EN function to save more energy and extend the battery life. The EN pin can switch the regulator to standby mode.

Features

- Wide Input Voltage Range: 1.1V to 5V
- Very Low I_Q: 50μA typ
- Max Output Current: 500mA
- Output Voltage Range: 0.7V to 3.8V
- Dropout Voltage 525mV Typical (500mA) @0.8V Output
- Excellent Load/Line Transient Response
- Line Regulation: 0.1%/V (typical)
- Built-in Fold Back Protection Circuit
- Built-in Constant Slope Circuit
- Built-in Auto-discharging Circuit
- MSL: Level1(DFN6,DFN4), Level3(SOT23-5)

Applications

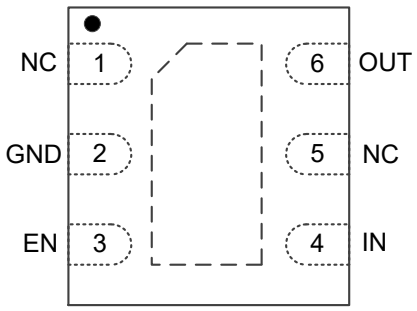
- Constant-Voltage Power Supply for Battery-Powered Device
- Constant-Voltage Power Supply for TV, Notebook PC and Home Electric Appliance
- Constant-Voltage Power Supply for Portable Equipment

Device information

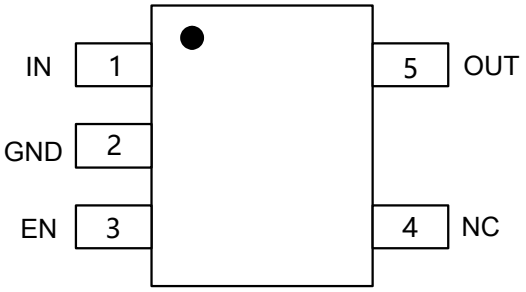
ET 540 XX X B

XX Output Voltage		**X** Package		**B** Auto-discharge Function	
Fixed output	0.7~3.8V	Y	DFN6-1.2×1.2	B	Auto-discharge
		Y1	DFN4-1.0×1.0		
		/	SOT23-5		

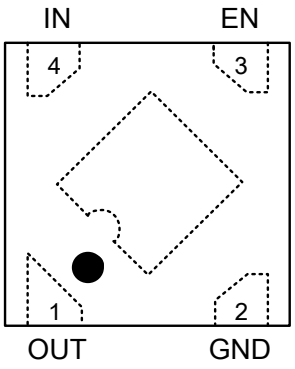
Pin Configuration



DFN6(1.2×1.2)



SOT23-5



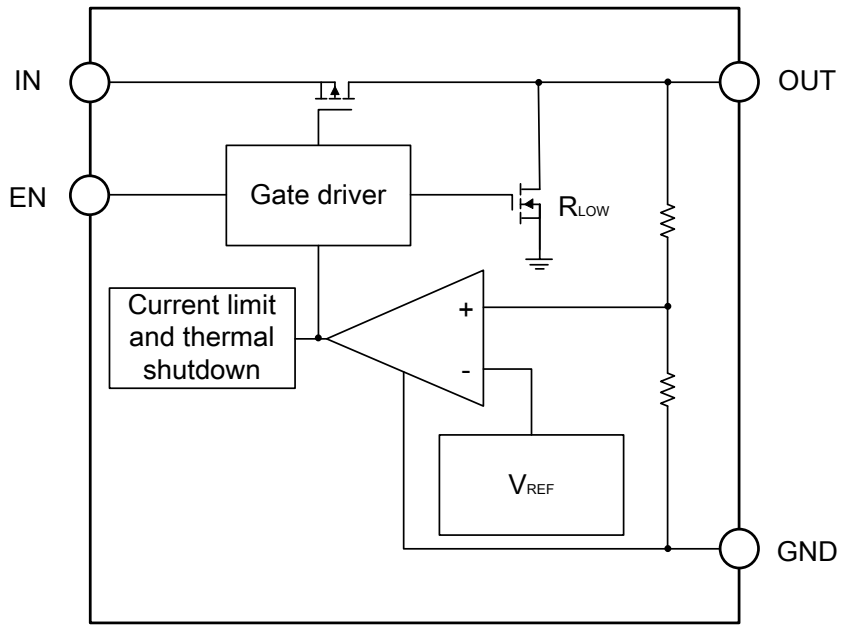
DFN4

TOP VIEW

Pin Function

Pin No.			Symbol	Pin Description
DFN6	DFN4	SOT23-5		
1	-	4	NC	No Connection
2	2	2	GND	Ground Pin
3	3	3	EN	Chip Enable Pin,"H" Enable
4	4	1	IN	Input Pin
5	-	-	NC	No Connection
6	1	5	OUT	Output Pin

Block Diagram



Functional Description

Input Capacitor

A 1μF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO.The recommended output capacitance is 1μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

EN Pin Operation

The ET540XX is turned on by setting the EN pin to “H”. Since the EN pin is neither pulled down nor pulled up internally, do not set it in floating status. When the EN pin is not used, connect the EN pin with V_{IN} to keep the LDO in operating mode.

Current Limit Protection

When output current of OUT pin is higher than current limit threshold or the OUT pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent

over-current and thermal damage.

Auto Discharging

When the EN pin set to “L”, the output circuit will be disable immediately, and the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of V_{OUT} in very short time. The Auto-Discharging function is optional.

Absolute Maximum Ratings

Symbol	Parameter		Rating	Unit
V_{IN}	Input Voltage Range		-0.3 to +6	V
V_{EN}	Enable Voltage Range		-0.3 to +6	V
V_{OUT}	Output Voltage Range		-0.3 to (V_{IN} + 0.3) ≤ 6	V
I_{OUT}	Maximum Load Current		500	mA
T_J	Maximum Junction Temperature		-40 to +150	°C
T_{STG}	Storage Temperature		-65 to +150	°C
T_{SLOD}	Lead Temperature (Soldering, 10 sec)		300	°C
V_{ESD}	HBM (EIA/JESD22-A114-A)		±4.0	KV
	CDM (EIA/JESD22-C101-A)		±1.5	KV
I_{LU}	Latch up Current Maximum Rating (JESD78E)		±200	mA
P_{DMAX}[(1)]	Maximum Power Dissipation	DFN1.2×1.2-6	625	mW
		DFN1.0×1.0-4	400	
		SOT23-5	420	

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{IN}	Input voltage range	V_{OUT} +V_{DO} to 5.5	V
I_{OUT}	Output Current	0 to 500	mA
T_A	Operating Ambient Temperature	-40 to +85	ºC
C_{IN}	Effective Input Ceramic Capacitor Value	0.47 to 10	µF
C_{OUT}	Effective Output Ceramic Capacitor Value	0.47 to 10	µF
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

Electrical Characteristics

$V_{IN}=V_{SET}+1.0V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$,unless otherwise noted.$T_A=25$ ºC

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN} (1)		1.1		5	V
Output Voltage	V_{OUT}	$V_{SET}\geq1.0$,$T_A=25$ºC	×0.98		×1.02	V
		$V_{SET}<1.0$,$T_A=25$ºC	×0.98		×1.02	V
		$V_{SET}\geq1.0$,-40ºC≤T_A≤+85ºC	×0.975		×1.025	V
		$V_{SET}<1.0$,-40ºC≤T_A≤+85ºC	×0.975		×1.025	V
Output Current	I_{OUT}	$V_{IN}=V_{SET}+1V$	500			mA
Load Regulation	RegLoad	$V_{IN}=V_{SET}+1V$,1mA≤I_{OUT}≤500mA		25	45	mV
Line Regulation	RegLine	$V_{SET}+0.5V\leq V_{IN}\leq3.6V$ ($V_{IN}\geq1.4V$)		0.10	0.25	%/V
Dropout Voltage	V_{DROP} (2)	$V_{SET}=0.8V$,$I_{OUT}=500mA$, V_{OUT} dropping to 0.98×V_{SET}		525		mV
		Other refer to the following table				
Supply Current	I_{Q_ON}	$I_{OUT}=0mA$		50		μA
Standby Current	I_{Q_OFF}	$V_{EN}=0V$		0.1	5	μA
Power Supply Ripple Rejection	PSRR (3)	f=1kHz, Ripple 0.2Vp-p $V_{IN}=V_{SET}+1V$, $I_{OUT}=30mA$		70		dB
Short Current Limit	I_{SC}	$V_{OUT}=0V$		110		mA
CE Pull-down Current	I_{CE}				1	μA
CE Input Voltage High	V_{CEH}	V_{IN}=1.1~5.5V	0.9			V
CE Input Voltage Low	V_{CEL}	V_{IN}=1.1~5.5V			0.4	V
Output Noise	e_N (3)	BW=10Hz to 100kHz $I_{OUT}=30mA$,$V_{OUT}=0.8V$		40		μVrms
Auto-Discharge Resistance	R_{DIS}	$V_{IN}=2.0V$,$V_{EN}=0V$		40		Ω

Notes:

1: The maximum input voltage should take into account the maximum power consumption ($P_{D(MAX)}$).The calculation formula is as follows:

$$\mathbf{P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT}}$$

The maximum power consumption of the DFN4 is 400mW.

$$\mathbf{V_{IN(MAX)} = 400mW / I_{OUT} + V_{OUT}}$$

For example:

If V_{OUT}= 1.2V, I_{OUT}=400mA, The maximum input voltage is $V_{IN(MAX)}$=400mW / 400mA+1.2=2.2V

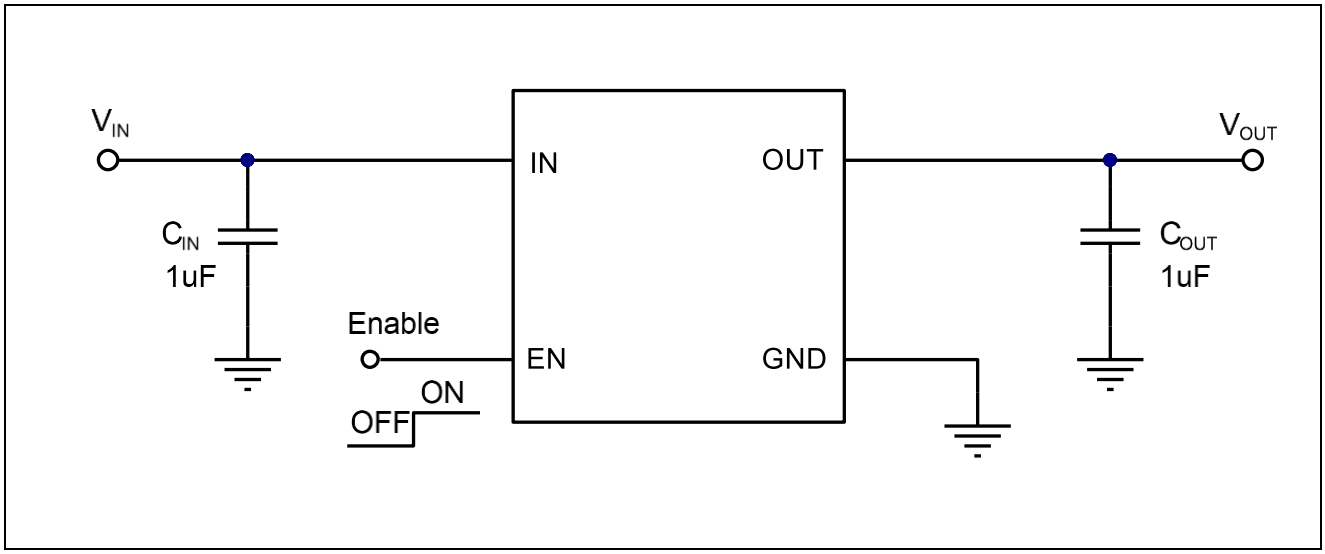
2: V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET} +$V_{DROPMAX}$ with output current.

3: Guaranteed by design and characterization. not a FT item.

Dropout Voltage by Output Voltage

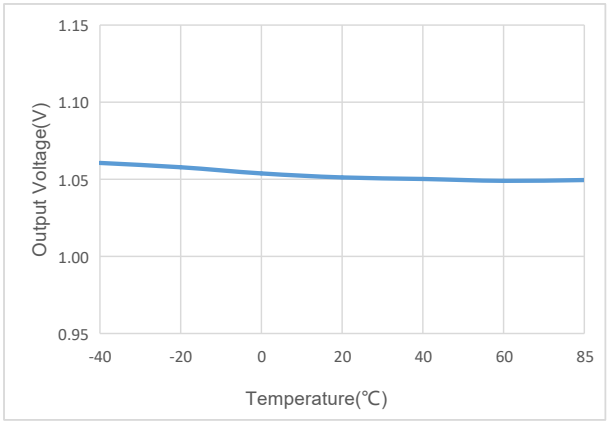
Output Voltage V_{OUT}(V)	Dropout Voltage V_{DROP} (V)		
	Condition	Typ	Max
0.7 ≤ V_{OUT} < 0.8	I_{OUT}=500mA	0.55	0.78
0.8 ≤ V_{OUT} < 0.9		0.50	0.65
0.9 ≤ V_{OUT} < 1.0		0.42	0.55
1.0 ≤ V_{OUT} < 1.2		0.38	0.48
1.2 ≤ V_{OUT} < 1.5		0.34	0.44
1.5 ≤ V_{OUT}		0.25	0.35

Application Circuits

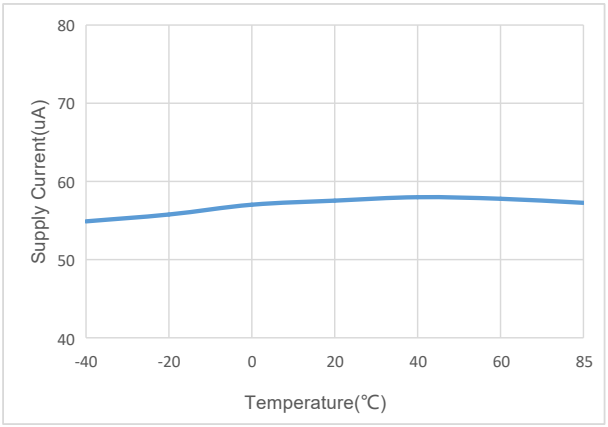


Typical Characteristics

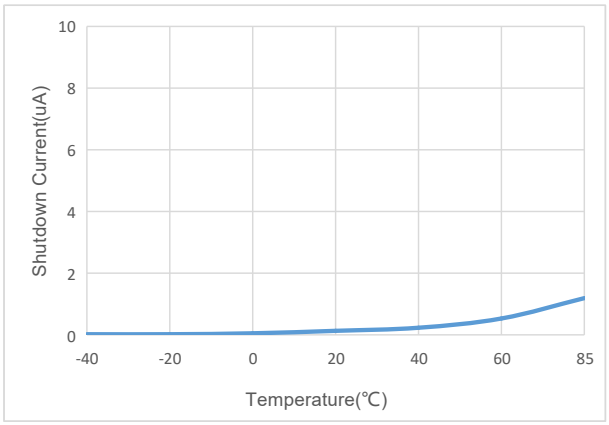
(V_{OUT}=1.05V,V_{IN}=2.05V,C_{IN}=C_{OUT}=1μF,T_A= -40ºC~+85ºC)



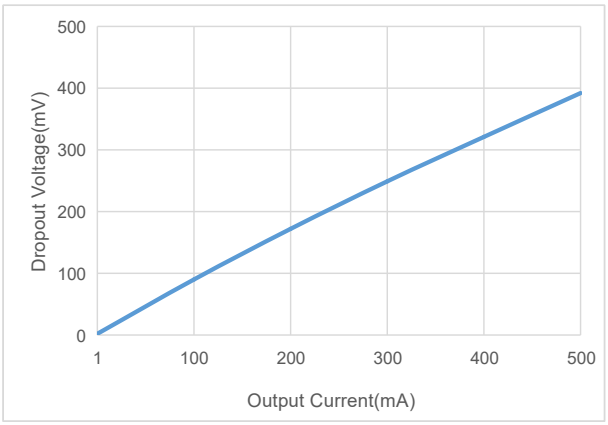
Output Voltage VS Temperature



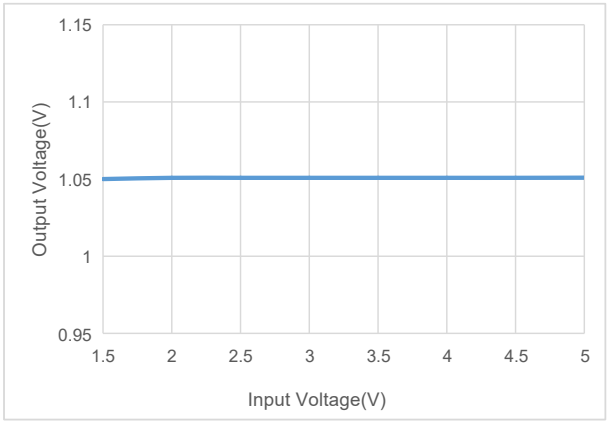
Supply Current VS Temperature



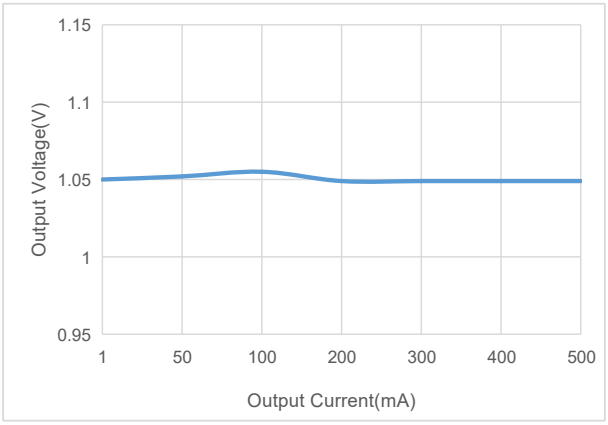
Shutdown Current VS Temperature



Dropout Voltage VS Output Current



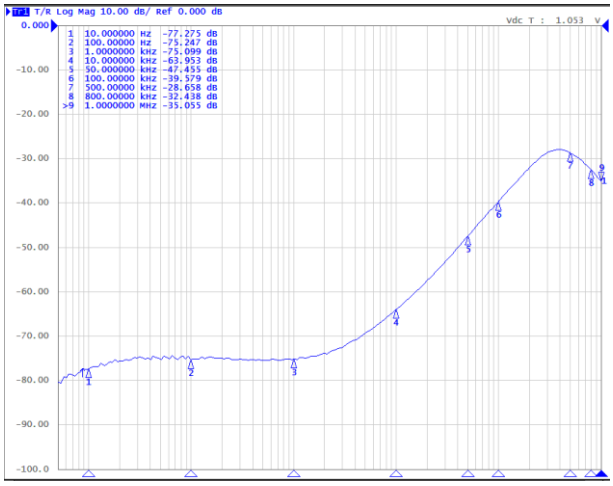
Output Voltage VS VIN Input Voltage



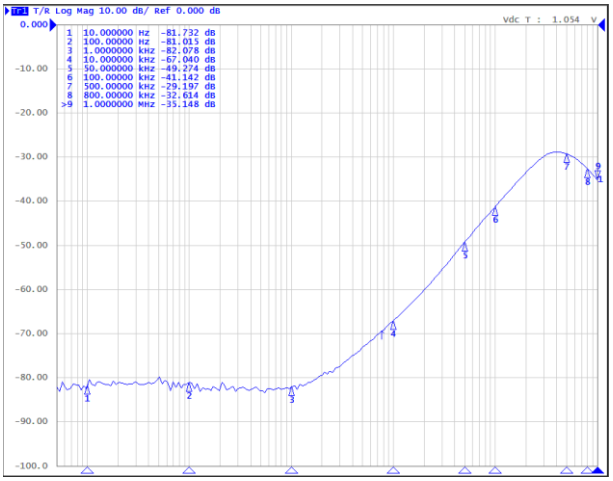
Output Voltage VS Output Current

Typical Characteristics(Continued)

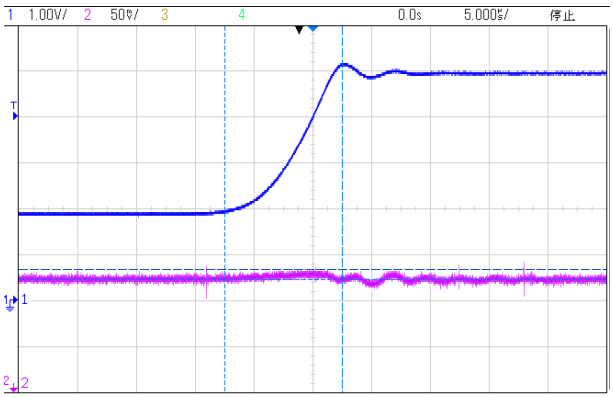
(V_{OUT}=1.05V,V_{IN}=2.05V,C_{IN}=C_{OUT}=1μF,T_A= -40ºC~+85ºC)



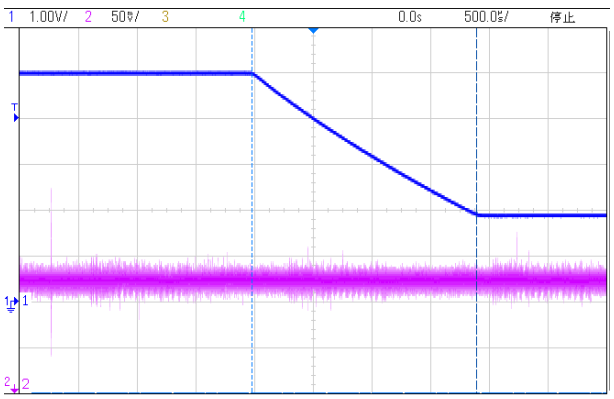
VIN=2.0V PSRR



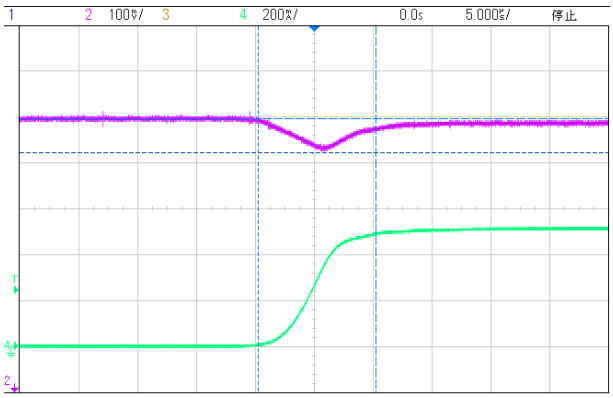
VIN=2.5V PSRR



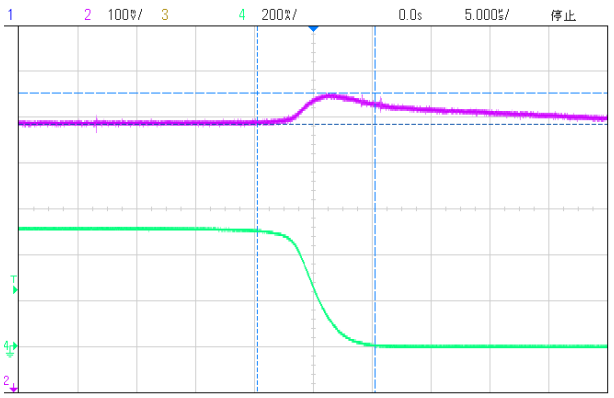
Line Transient(2.05V~5.0V 10us)



Line Transient(5V~2.05V 10us)



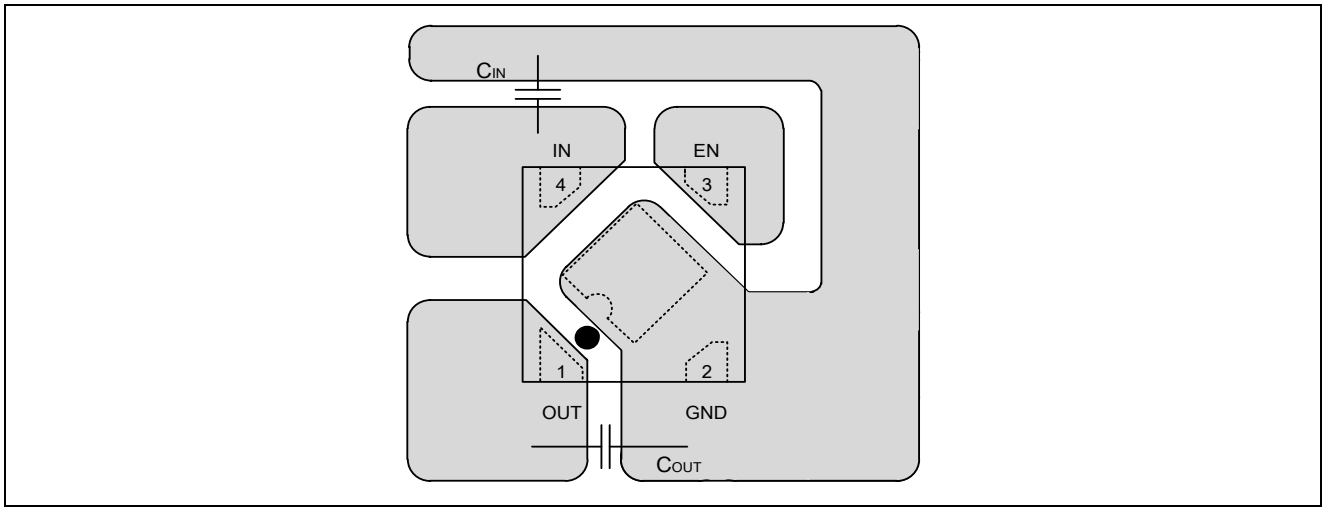
Load Transient(1mA~0.5A 10us)



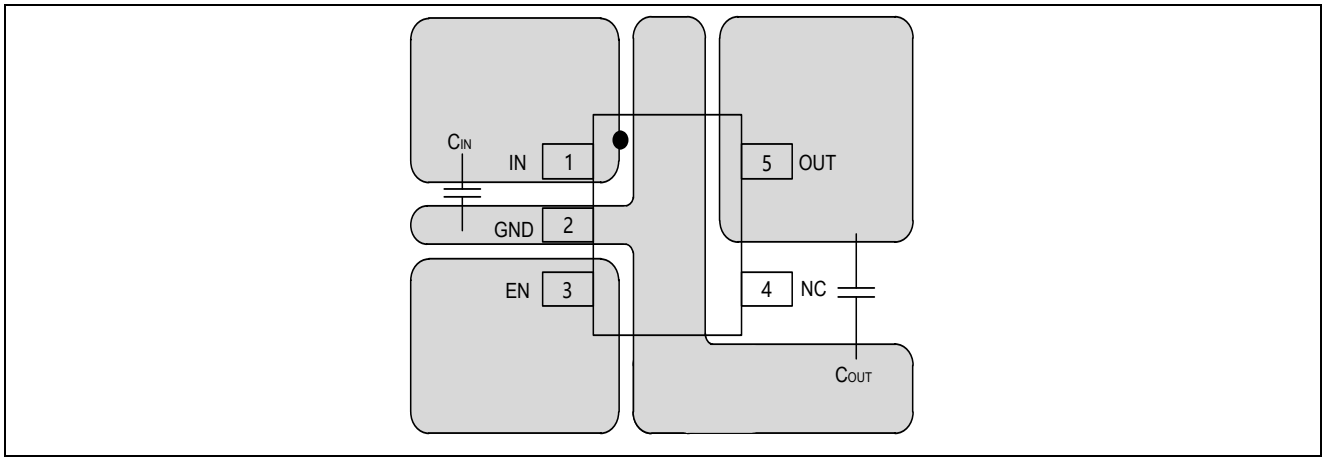
Load Transient(0.5A~1mA 10us)

PCB Layout Guide

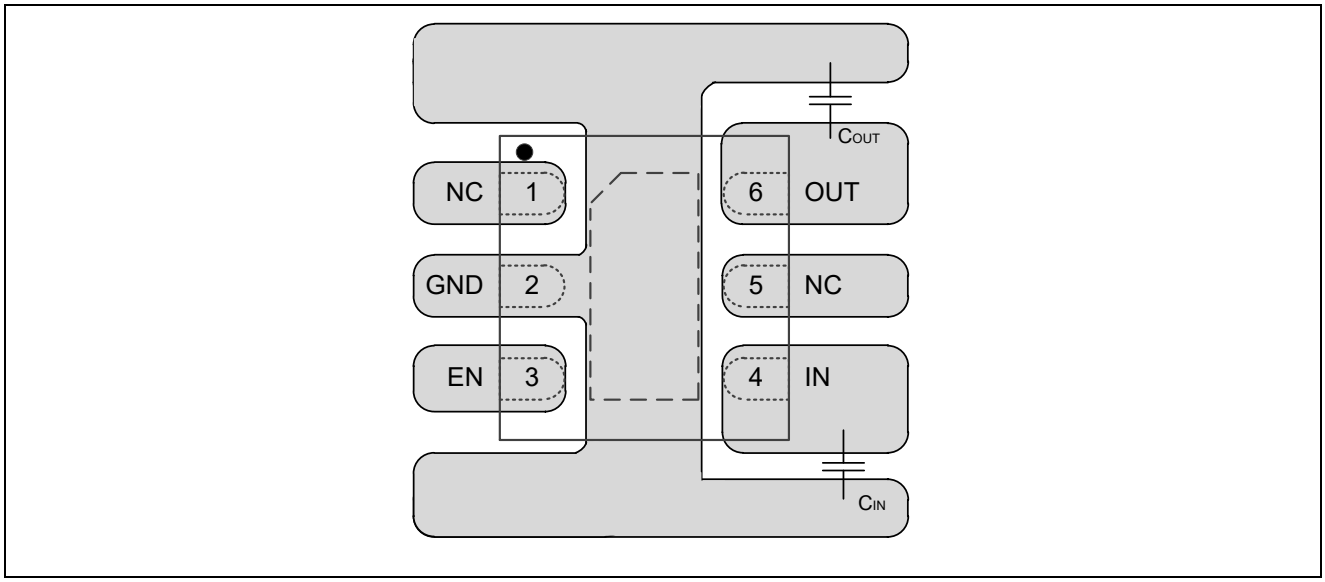
DFN4



SOT23-5

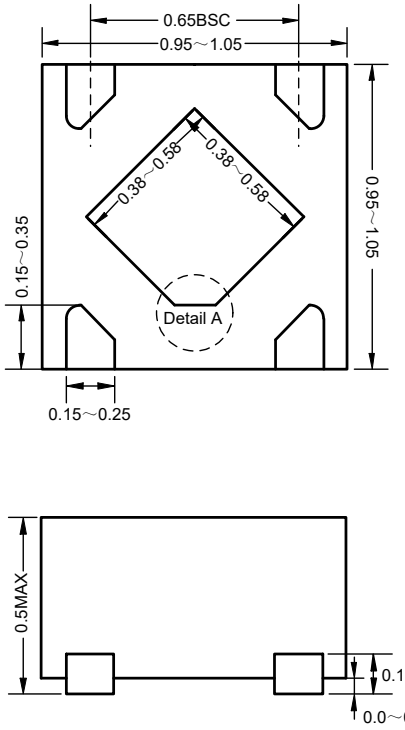


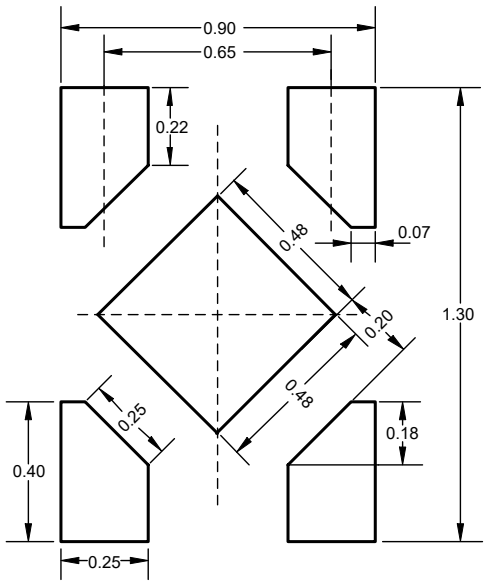
DFN6



Package Dimension

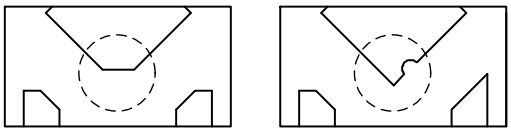
DFN4





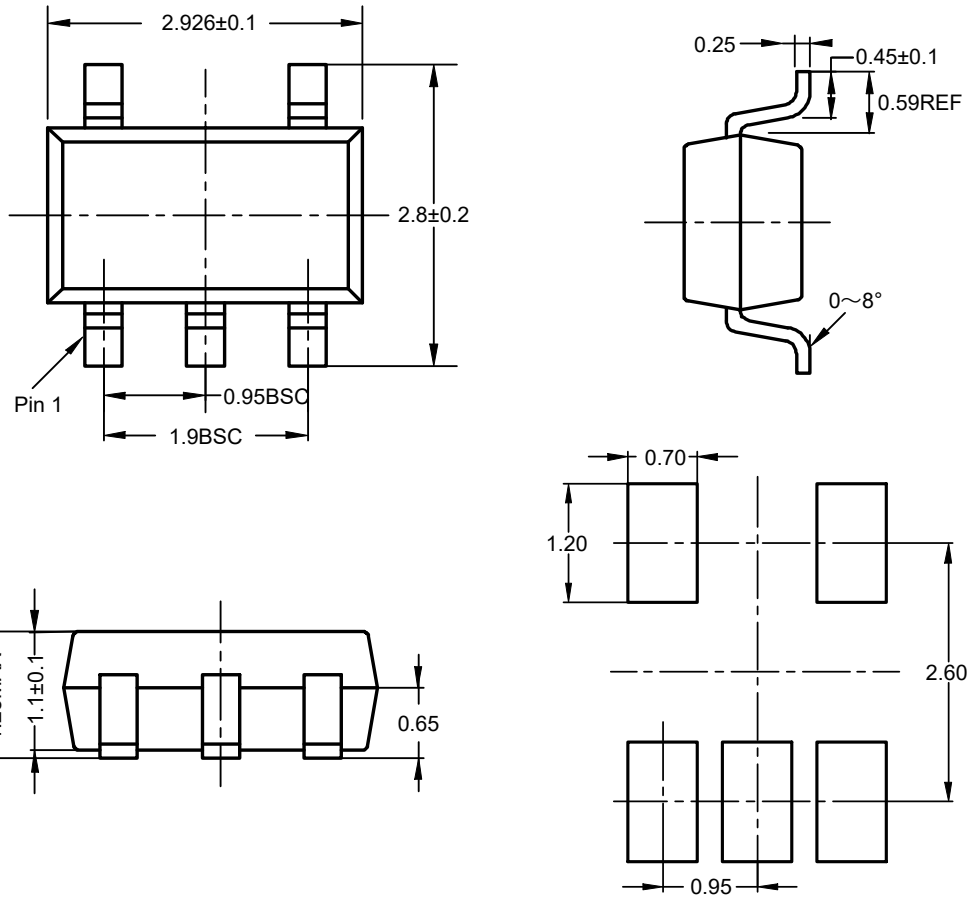
Recommended Land Pattern

Detail A: (PIN1 shape)



Unit: mm

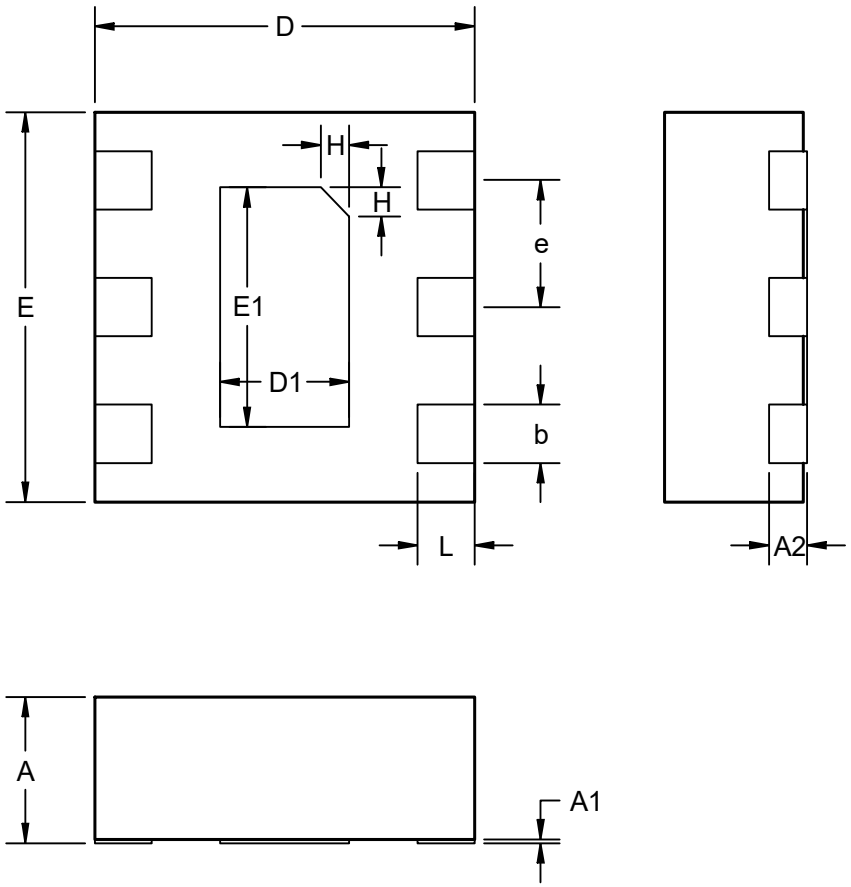
SOT23-5



Recommended Land Pattern

Unit: mm

DFN6



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.34	0.37	0.40
A1	0	0.02	0.05
A2		0.10REF	
b	0.13	0.18	0.23
D	1.10	1.20	1.30
D1	0.25	0.30	0.35
E	1.10	1.20	1.30
E1	0.89	0.94	0.99
e	0.30	0.40	0.50
H		0.15REF	
L	0.15	0.20	0.25

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2017-08-10	Original version	Liuyg	Liuyg	Zhujl
1.1	2017-11-22	Add Mark Specification	Liuyg	Liuyg	Zhujl
1.2	2017-12-01	Add DFN4,SOT23-5 package	Liuyg	Liuyg	Zhujl
1.3	2018-06-21	Change the AMR VIN to 6V	Liuyg	Liuyg	Liujy
1.4	2019-09-05	Revise Vout in label information	Wuxj	Wuxj	Liujy
1.5	2022-7-20	Update Typeset	Tugz	Liuyg	Liujy
1.6	2023-10-11	Update package picture/500mA	Shibo	Liuyg	Liujy