Constant Current RGB LED Driver with I²C Control

General Description

The ET6326 is a constant current RGB LED drivers with I²C interface. The devices are ideally powered from one-cell lithium-ion/polymer, 3-cell NiCd/NiMH/Alkaline batteries, or 3.3V~5V supplies. The independent programmable constant current sinks operate without external components.

By the nine internal registers programming, the three LED channels can work in variety modes, a total of 192 current levels are available for each channel from 0.125mA to 24mA with a 0.125mA step.

The device has design three kinds of interconnected threads, each channel can carry on any thread. With an on-chip timing control unit, LED blink rate, fade-in and fade-out are user-adjustable resulting in unique color lighting patterns.In shutdown mode, the quiescent current is reduced to less than 1μA.

The driver is available in a small DFN8 package. The package is Pb-free and RoHS compliant.

Features

- Ultra low dropout regulated current sinks
- 75mV typical at 10mA per channel
- Programmable LED setting with I²C control
- Individual channel control
  - On/Off Interval Time Control
  - Dimming Up/Down Time
  - Current Level Setting
  - RGB LED Color Control
- 192 current levels: 24mA max, 0.125mA step
- ±5% current matching for max current
- No noise, non-pulsating LED current
- Fast, smooth start-up
- VIN Range: 2.7V to 5.5V
- Low supply current of 200μA typ.
- 0.1 μA Shutdown Current
- Pb-free Package: DFN8 (1.5mm × 1.5mm × 0.45mm)
- Inside Temperature protection
- -40 to +85 C° Temperature Range
- MSL 1

Application

- RGB indicator LEDs
- Flashing LEDs
- Mobile Phones
- Handheld Devices
- Digital Cameras

Pin Configuration

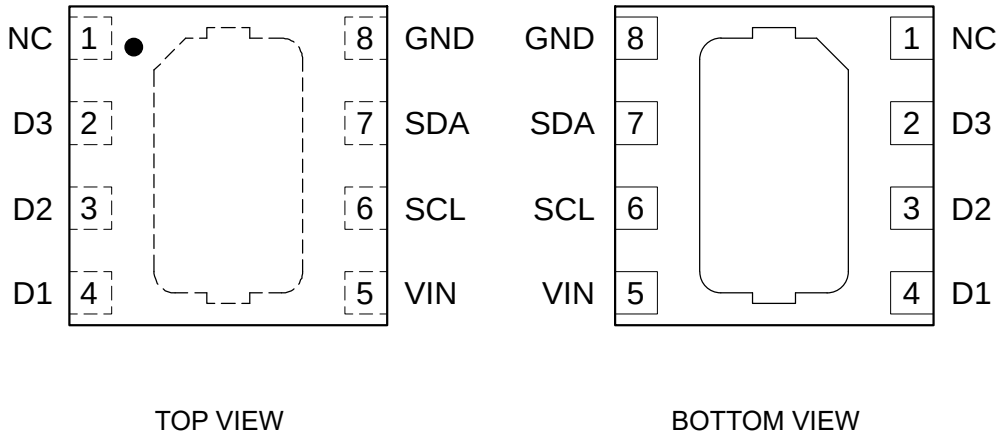


Figure 1. Pin Assignment

Pin Function

Pin No.	Pin Name	Description
1	NC	No connect.
2	D3	Regulated output current sink D3. Current level and ON/OFF selections are controlled by I²C interface.
3	D2	Regulated output current sink D2. Current level and ON/OFF selections are controlled by I²C interface.
4	D1	Regulated output current sink D1. Current level and ON/OFF selections are controlled by I²C interface.
5	VIN	Input power for the IC.
6	SCL	Clock of the I²C interface.
7	SDA	Data of the I²C interface.
8	GND	Ground pin.

Block Diagram

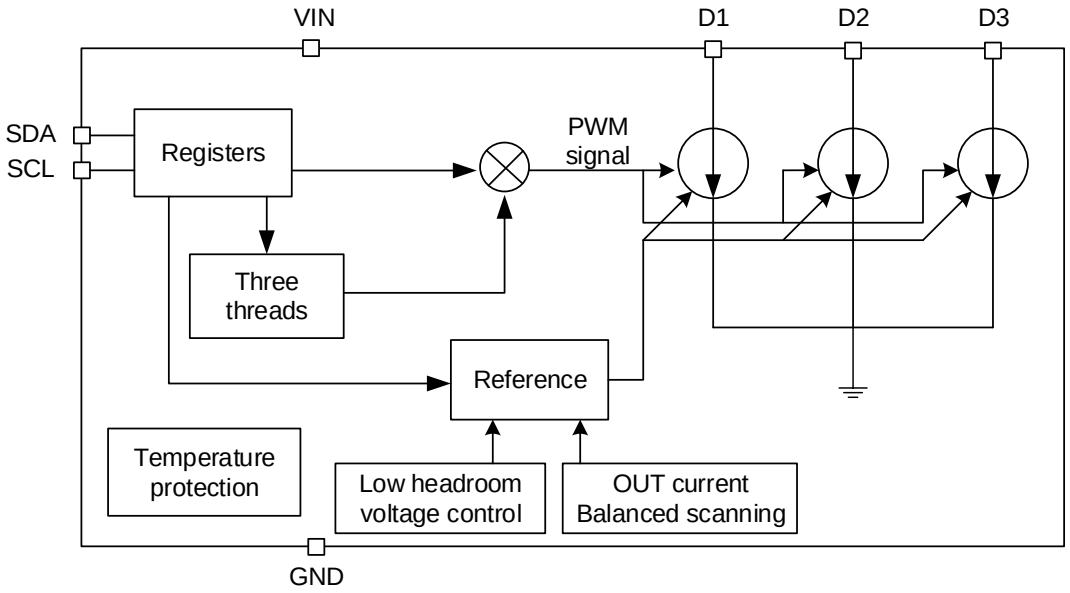


Figure 2. Function Block

Functional Description

The ET6326 is a 3-channel output current sink device, offering constant current regulation with high efficiency and ultra low internal voltage drop. High integration and small size makes it ideal for driving RGB LEDs from a one-cell lithium-ion/polymer battery. With a supply voltage range of 2.7V to 5.5V, the ET6326 is equally suitable for 3- or 4-cell NiCd/NiMH/Alkaline devices or systems with 3.3V or 5V supplies.

The ET6326 can be programmed by I^2C compatible interface. Each current sink can be configured independently to one of the 192-step current levels or turned off.

LED current programming

Each channel’s brightness is controlled by the LEDx Iout registers Reg6 to Reg8. Each channel has a dedicated 8-bit register for setting the current value. The LED channel current is constant, non-pulsing, except when it is being ramped-up and down.

The ramp up and down are automatically generated using a PWM scheme where the duty cycle is continuously changing (either increasing or decreasing) to provide a smooth LED current transition between the ON and OFF states. The ramp times, for rise and fall, are separately programmable through an internal Ramp register Reg5 with 4 bits for rise and 4 bits for fall. The ramping can be configured to linear or quasi-logarithmic/s-curve by setting register Reg1 bit 7.

Flashing LEDs can be performed by programming the time period (Tflash) between two consecutive flashes in the Flash Period register Reg1. Two Flash On Timer 1/2 registers, Reg2 and Reg3, allow to set the LED on time as a percentage of the Flash period. The on time (Ton), shown in Figure 1, includes the ramp-up Trise and the full on time. Two timer registers are available to support two or more LEDs to flash independently. Each channel can be configured to timer1 or timer2 with the Channel Control register Reg4.

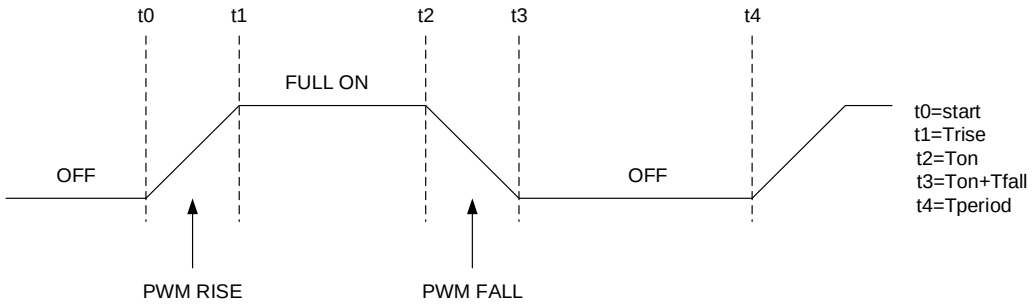


Figure 3. Channel Timing Diagram

Timer Mode Control

The timing diagrams for the four time modes are illustrated below.

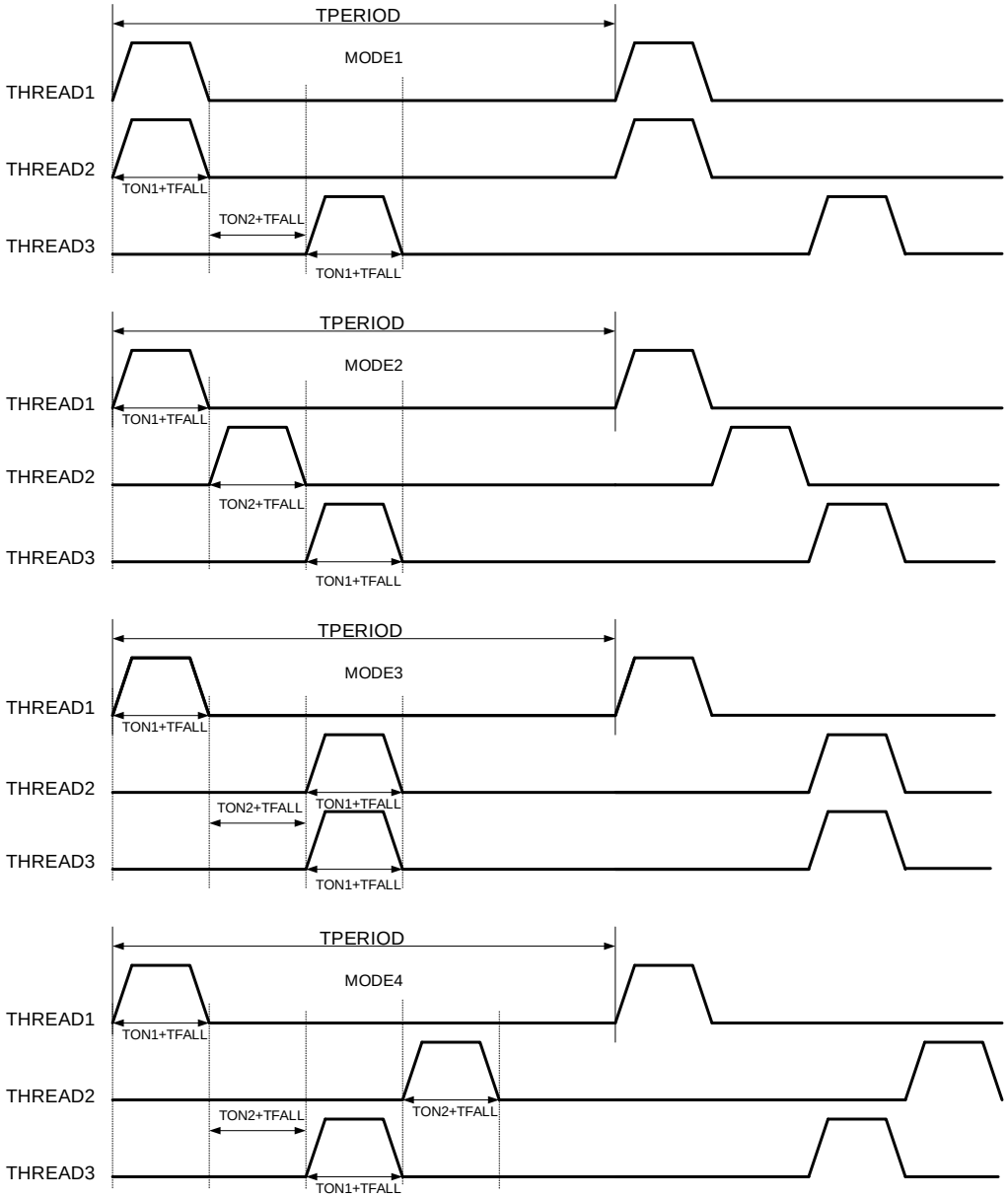


Figure 4. Four Mode Timing Diagram

Each channel can be assigned to one of the 3 time threads, or always OFF or always ON. The Timer Mode Control define the timing as figure2.

The Duty Cycle of each flash waveform is set by the timer and can be set with 8-bit resolution (256 steps) between 0 and 100%. The period of the flash repetition rate can also be set with a 7-bit resolution up to 16 seconds. The Flash repetition period is the same for all outputs. If the programmed total time of the Timers exceed the Flash repetition rate then the ThreadN mode will be terminated and the Timers reset to start position. This may cause the ThreadN signal to be instantly reduced to zero. If $T_{ON}<T_{RISE}$, the waveform fade-in will not reach maximum(FFH).

Rise/Fall Times

The Ramp-Up and Ramp-Down can be linear or S-shaped profile. The S-shape is the default. The ramp-up transitions from 0% to 100% of the Iset value (ON state) and ramp-down to 0% (OFF state).

LED Current Control

The brightness setting of each channel is internally controlled by 48 current units of 0.5mA. Output current resolution is increased to an effective 0.125mA steps by interpolation based time division multiplexing (similar to PWM) by a digital interpolator and works on the 2 LSB units of the current setting.

Register Map

REG	Addr	7	6	5	4	3	2	1	0	Reset Values
Reg0 Status	00H	-	Rise/Fall Time Scaling		Enable Control		Reset	Timer Mode Control		X00
Reg1 Flash Period	01H	Ramp Line	Flash Period							x00
Reg2 Flash Ton1	02H	Flash TON1								x01
Reg3 Flash Ton2	03H	Flash TON2								x01
Reg4 LED Work Mode	04H	LED3 Thread 3EN	LED2 Thread 3EN	LED3 Work Mode		LED2 Work Mode		LED1 Work Mode		x00
Reg5 Ramp Rate	05H	Tfall				Trise				x00
Reg6 LED1 Iout	06H	LED1 current								x4F
Reg7 LED2 Iout	07H	LED2 current								x4F
Reg8 LED3 Iout	08H	LED3 current								x4F
Reg10	0AH	Shutdown mode select								x00

Note: LEDx corresponding the port of device Dx.

Reg0 [2:0] Timer Mode Control and Reset Control

Reg0 [2:0]	Function
000	mode1
001	mode2
010	mode3
011	mode4
100	Do nothing
101	Reset registers only
110	Reset all Digital circuit
111	Reset the whole device

Reg0 [4:3] Enable Control

Reg0[4:3]	Device ON Condition		Enter Shutdown(sleep) mode communication
	SCL	SDA	
00	1	1	Either SCL or SDA become 0
01	1	toggling	SCL=0, or SDA stop toggling
10	1	Don't care	SCL=0
11	Always On		Device always ON

Note: Device enter shutdown(sleep) mode need a delay time(600us typical) after the last rise edge of SDA.

Reg0 [6:5] Rise/Fall Time Scaling

These two bits allow to scale the rise and fall times defined in Reg5 ramp rate register.

For example, Reg0[6:5] = 01 (2x slower scaling) and Reg5 = 1, then the rise time =128ms x 2 = 256ms.

Reg0[6:5]	Function
00	1x Normal
01	2x Slower
10	4x Slower
11	8x Faster

Note: Bit Reg0[7] must be kept to 0 and is not used in normal operation (reserved for factory test).

Reg1 Flash Period and Reg2/Reg3 Flash On Time

The three registers Reg1, Reg2 and Reg3 allow configuration of the blinking time for the two timers TON1 and TON2. Reg2 and Reg3 define the LED ON time as a percentage of the period defined in Reg1. The ON time (Ton) includes the ramp rise time and ON hold time as shown in Figure 1.

For example, for Reg1 =4 and Reg2 = 5, ON timer 1 is equal to 2% of 0.64s = 12.8ms

Reg1[6-0] Flash Period		
Dec	**Binary**	**Period[s]**
0	0000000	0.128
1	0000001	0.256
2	0000010	0.384
3	0000011	0.512
4	0000100	0.640
5	0000101	0.768
6	0000110	0.896
7	0000111	1.024
8	0001000	1.152
9	0001001	1.28
10	0001010	1.408
11	0001011	1.536
12	0001100	1.664
13	0001101	1.792
……	……	……
111	1101111	14.33
112	1110000	14.46
113	1110001	14.59
114	1110010	14.72
115	1110011	14.85
116	1110100	14.98
117	1110101	15.10
118	1110110	15.23
119	1110111	15.36
120	1111000	15.49
121	1111001	15.62
122	1111010	15.74
123	1111011	15.87
124	1111100	16.0
125	1111101	16.13
126	1111110	16.26
127	1111111	16.38

Reg1[7] Ramp Linear

The default setting, bit Reg1[7] = 0, provides with a logarithmic-like S ramp up and down curve. By setting this bit to 1, the ramp becomes a simple linear up and down waveform.

Reg2/Reg3 Flash ON Timer 1/2		
Dec	**Binary**	**Percentage of Period[%]**
0	00000000	0.0%
1	00000001	0.4%
2	00000010	0.8%
3	00000011	1.2%
4	00000100	1.6%
5	00000101	2.0%
6	00000110	2.3%
7	00000111	2.7%
8	00001000	3.1%
9	00001001	3.5%
10	00001010	3.9%
11	00001011	4.3%
12	00001100	4.7%
13	00001101	5.1%
……	……	……
239	11101111	93.4%
240	11110000	93.8%
241	11110001	94.1%
242	11110010	94.5%
243	11110011	94.9%
244	11110100	95.3%
245	11110101	95.7%
246	11110110	96.1%
247	11110111	96.5%
248	11111000	96.9%
249	11111001	97.3%
250	11111010	97.7%
251	11111011	98.0%
252	11111100	98.4%
253	11111101	98.8%
254	11111110	99.2%
255	11111111	99.6%

Reg4 LED Work Mode Control

Register Reg4 sets the mode of each LED channel to either always ON/OFF or Thread1/Thread2/Thread3. For example Reg4 = 00000001(binary), sets LED1 ON and other channels OFF.

Note: LED1 can't carry on Thread3, and Reg4[7] and Reg4[6] become 1, LED2 and LED3 will carry on Thread3.

Reg4 LED Work Mode Control			
Bit	**Binary**	**LEDX**	**Function**
[7],[5:4]	000	LED3	Always OFF
	001		Always ON
	010		Thread1
	011		Thread2
	1xx		Thread3
[6],[3:2]	000	LED2	Always OFF
	001		Always ON
	010		Thread1
	011		Thread2
	1xx		Thread3
[1:0]	00	LED1	Always OFF
	01		Always ON
	10		Thread1
	11		Thread2

Reg5 Ramp Times

The register Reg5 sets the rise and fall time durations for the LED current ramp transitioning between 0mA and the nominal current. The rise and fall ramp times are defined by 4 bits Reg5[3-0] and Reg5[7-4] respectively.

For example, Reg5 = 4 and Reg0[6,5] = 0 (1x ramp scaling), then the rise time is equal to 512ms.

T_{rise} Reg5[3-0]		Ramp Time [ms]			
T_{fall} Reg5[7-4]		Ramp Scaling			
Dec	Binary	00 1x	01 2x slower	10 4x slower	11 8x faster
0	0000	2	2	2	2
1	0001	128	256	512	16
2	0010	256	512	1024	32
3	0011	384	768	1536	48
4	0100	512	1024	2048	64
5	0101	640	1280	2560	80
6	0110	768	1536	3072	96

7	0111	896	1792	3584	112
8	1000	1024	2048	4096	128
9	1001	1152	2304	4608	144
10	1010	1280	2560	5120	160
11	1011	1408	2816	5632	176
12	1100	1536	3072	6144	192
13	1101	1664	3328	6656	208
14	1110	1792	3584	7168	224
15	1111	1920	3840	7680	240

Note: There is only one Tramp Scaling register for both the rise and fall times.

Reg6, Reg7, Reg8 LED Current Setting

Registers Reg6 to Reg8 define the LED current setting for the channels D1 to D3 respectively. The LED current can be programmed with 192 steps between 0.125mA minimum and 24mA maximum.

For example, 24mA is set by the code BF hexadecimal (191 decimal, 1011 1111 binary) or any higher code value. 10mA current is set by the code 4F hexadecimal (79 decimal, 0100 1111 binary)

Data Dec	Data Hex	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Iout (mA)
0	00h	0	0	0	0	0	0	0	0	0.125
1	01h	0	0	0	0	0	0	0	1	0.25
2	02h	0	0	0	0	0	0	1	0	0.375
3	03h	0	0	0	0	0	0	1	1	0.50
……	……	……	……	……	……	……	……	……	……	……
79	4Fh	0	1	0	0	1	1	1	1	10.00
80	50h	0	1	0	1	0	0	0	0	10.13
……	……	……	……	……	……	……	……	……	……	……
159	9Fh	1	0	0	1	1	1	1	1	20.00
160	A0h	1	0	1	0	0	0	0	0	20.13
……	……	……	……	……	……	……	……	……	……	……
190	BEh	1	0	1	1	1	1	1	0	23.88
191	BFh	1	0	1	1	1	1	1	1	24.00
192	C0h	1	1	0	0	0	0	0	0	24.00
……	……	……	……	……	……	……	……	……	……	……
254	FEh	1	1	1	1	1	1	1	0	24.00
255	FFh	1	1	1	1	1	1	1	1	24.00

Note: The 2 LSB’ s are timed division multiplexed (similar to PWM) by a digital interpolator. Minimum Iout unit is 0.5mA.

Reg10 Shutdown mode select

Reg10[1:0]	Function
X0	Through SDA/SCL state to achieve shutdown function(reference Reg0[4:3])
01	Shielding SDA/SCL state achieve shutdown function and device always ON
11	Device enter shutdown(sleep) mode by software

Reg10[7:2]	Function
Reserved	NC

Serial Port Interface (I^2C)

Bus Interface

Baseband Processor can transmit data with ET6326 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET6326 will send a low level response signal with one period width to the SDA port. During the reading mode, ET6326 will not send response signal and the host will send a high response signal one period width to the SDA.

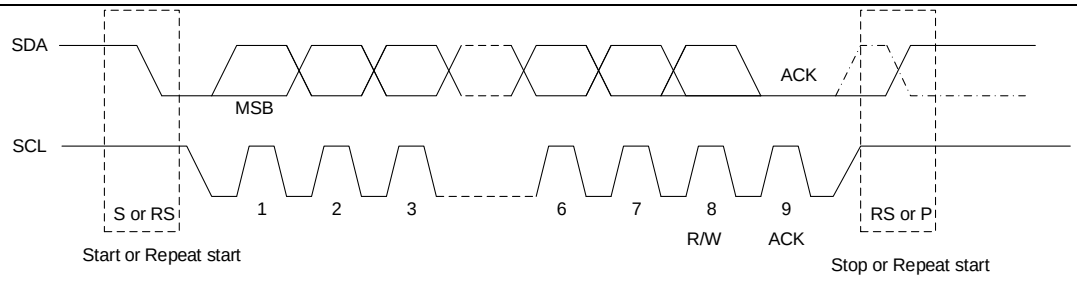


Figure 5. I^2C write mode

- ACK=Acknowledge
- MSB=Most Significant Bit
- S=Start Conditions RS=Restart Conditions P=Stop Conditions
- Fastest Transmission Speed =400KBITS/S
- Restart: SDA-level turnover as expressed by the dashed line waveform

Chip-Address

Chip-Address	Description
60H/61H	Writing/ Reading Reg mode

I²C Writing Command Register Interface Protocol (continuous):

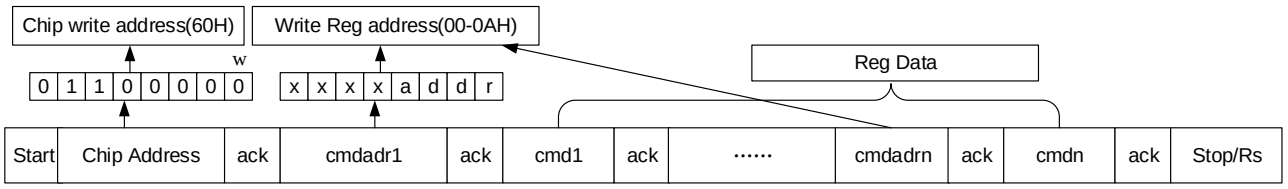


Figure 6. I²C Writing Command Register(continuous)

- Start Cond=Start Conditions
- Chip Addr=Chip Address=01100000b
- ACK=Acknowledge
- REG address= cmdadr1=(xxxx + REG's 4bit addr)
- ACK Acknowledge
- Command Reg data 1=(Command data cmd1)
- ACK= Acknowledge
- ……
- REG address= cmdadrn=(xxxx + REG's 4bit addr)
- ACK Acknowledge
- Command Reg data n=(Command data cmdn)
- ACK= Acknowledge
- Stop

I²C Writing Command Register Interface Protocol (single):

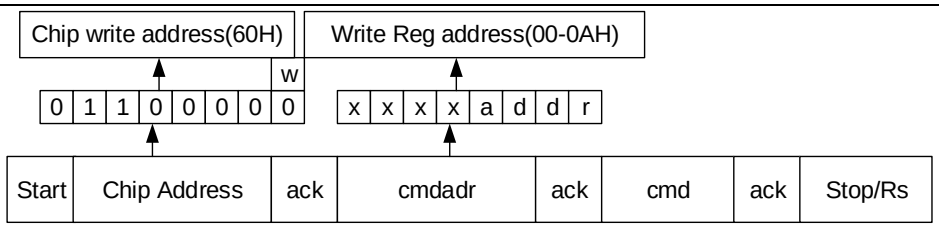


Figure 7. I²C Writing Command Register(single)

- Start Cond=Start Conditions
- Chip Addr=Chip Address=01100000b
- ACK=Acknowledge
- REG address = cmdadr(xxxx + REG's 4bit address)
- ACK Acknowledge
- Command Reg data=(Command data cmd)
- ACK Acknowledge
- Stop

I²C Reading Command Register Interface Protocol

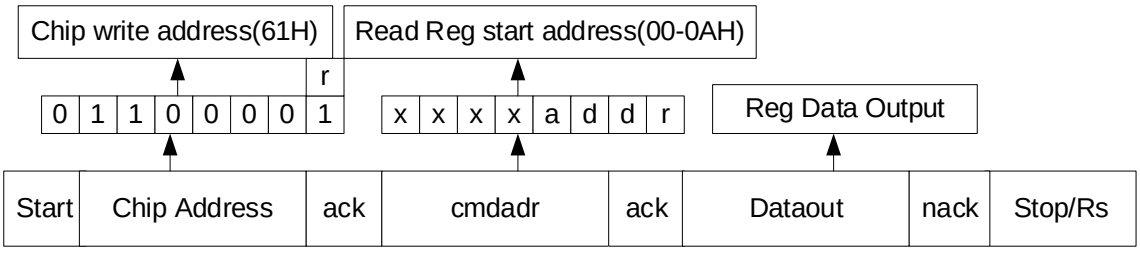


Figure 8. I²C Reading Command Register

- Start Cond=Start Conditions
- Chip Addr=Chip Address=01100001b
- ACK=Acknowledge
- REG address = cmdadr (xxxx + REG's 4bit addr）
- ACK Acknowledge
- DATAOUT=(Reg data output)
- NACK=NO ACK Acknowledge
- Stop

Voltage Headroom

The lowest headroom voltage is critical for systems with supply voltages nearing 3V, such as battery operated or regulated 3.3V systems. The advancement of LED technologies has made possible lower LED current and lower forward voltage drop (VF). For example, the majority of vendors' LED3's VF at 5mA is 3.15V or below. With the cut-off voltage for most 1-cell Li+ powered systems set between 3.3V and 3.5V, it is possible to drive RGB LEDs without voltage step-up as long as the internal voltage drop for the driver circuit is specially designed for the lowest voltage possible.

Each current sink of the ET6326 is designed to allow the lowest operating input voltage without voltage step-up while maintaining current regulation, thus extending the battery run time. When input voltage is low, the internal low impedance current sink adds merely 75mV (typical) headroom on top of the LED forward voltage at 24mA per channel.

The formula is: $V_{IN(MIN)} = V_{F(MAX)} + V_{SINK(MIN)}$

When V_{IN} is the driving voltage applied to the anode of each LED, VF is the forward voltage drop of the LED, and V_{SINK} is the voltage at each Dx. When V_{IN} is high, V_{SINK} is internally regulated to take the voltage difference between V_{IN} and VF. For instance, if V_{IN} is 4V and VF for LED1 is 3.1V, then V_{SINK} at D1 pin is 0.9V.

When V_{IN} decreases (as the battery discharges), $V_{IN(MIN)}$ governs the lowest supply voltage for the LEDs without losing regulation. The design rule of thumb is to make sure the cut-off voltage is higher than $V_{IN(MIN)}$ for all conditions. It is important to emphasize the definition of "losing regulation"; in this datasheet it is defined as when the LED current drops to 90% of the nominal programmed current level.

At 24mA, the typical V_{SINK} can be as low as 75mV for each Dx pin. Since every LED has a slightly different VF at a given current, the minimum VIN is determined by the highest VF plus 75mV typical. For the case of 24mA programmed current and highest VF of 3.2V, V_{IN} in can go as low as 3.275V without losing LED current regulation. When V_{IN} drops further while the $V_{SINK(MIN)}$ remains constant, VF will be forced lower. As a result, the LED current will reduce according to each LED's V-I curve.

Absolute Maximum Ratings

Parameter		Range	Unit
VIN, D3, D2, D1		-0.3 to 6.0	V
SCL, SDA		-0.3V to V_{IN}+0.3	V
Storage Temperature		-65 to 150	°C
Junction Temperature		-40 to 150	°C
Operating Temperature		-40 to 85	°C
ESD	Human Body Model (JESD22-A114)	±2000	V
	Charged Device Model (JESD22-C101)	±1000	V

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied.
Only one Absolute Maximum rating should be applied at any one time.

Electrical Characteristics

D.C. Characteristics, V_{IN}=3.6V, T_A=25°C (Unless otherwise specified)

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
V_{IN}	Operating Voltage		2.7		5.5	V
V_{DPO}	Dx Pin Dropout Voltage (90% Of nominal current)	All Channels set to 20mA Reg6-8=9Fh		75	120	mV
I_{SINK}	Out Current Accuracy	All Channels set to 20mA Reg6-8=9Fh	-5		5	%
		All Channels set to 0.125mA Reg6-8=0h	-5		5	%
	Out Current Matching	All Channels set to 20mA Reg6-8=9Fh	-5		5	%
I_{IN}	Supply Current	All 3 Channels set to 20mA Reg6-8=9Fh		300		μA
		1 Channel set to 20mA Other channels OFF		260		μA
I_Q	IC Quiescent Current	Device on, All LEDs OFF, Reg4=0		190		μA
I_{SHDN}	Shutdown Current	Shutdown Mode		0.1	1.0	uA
V_{IH}	Input high Voltage	V_{IN}=3.6V, SDA, SCL	1.2			V
		VIN=5.0V, SDA, SCL	1.8			V
V_{IL}	Input Low Voltage	SDA, SCL			0.4	V
V_{OL_SDA}	SDA Output Low Level	I_{OL}=3mA	-	0.1	0.3	V
Fosc	OSC Frequency	Fosc=1MHz	-5		5	%
T_{ST}	Thermal Shutdown Threshold			140		°C
T_{SH}	Thermal Shutdown Hysteresis			15		°C

I²C mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCL}	SCL Clock Frequency	0	-	400	KHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	1.3	-	-	μs
$t_{HD:STA}$	Hold Time(Repeated) START Condition	0.6	-	-	μs
t_{LOW}	Low Period of SCL Clock	1.3	-	-	μs
t_{HIGH}	HIGH Period of SCL Clock	0.6	-	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	0.6	-	-	μs
$t_{HD:DAT}$	Data Hold Time	-	-	0.9	μs
$t_{SU:DAT}$	Data Setup Time	100	-	-	ns
t_R	Data Hold Time2	-	20+0.1Cb(1)	300	ns
t_F	Data Hold Time2	-	20+0.1Cb(1)	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	0.6	-	-	μs

Note1: Cb=total capacitance of one bus line in PF.

I²C mode Timing Diagram

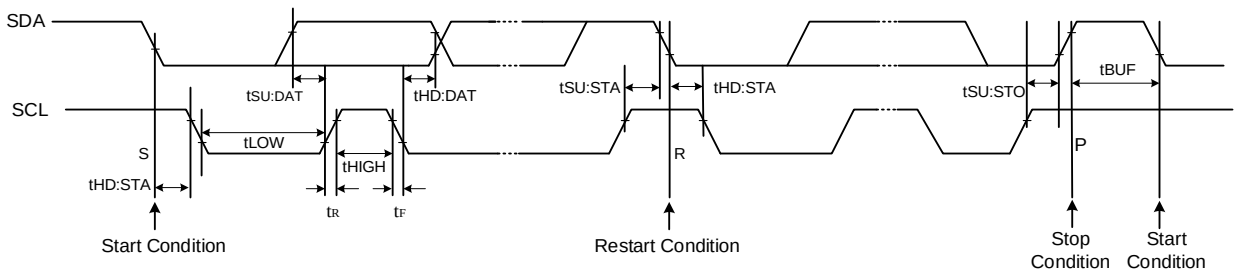
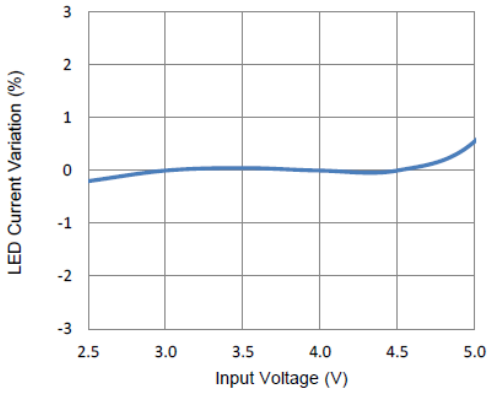


Figure 9. I²C mode time

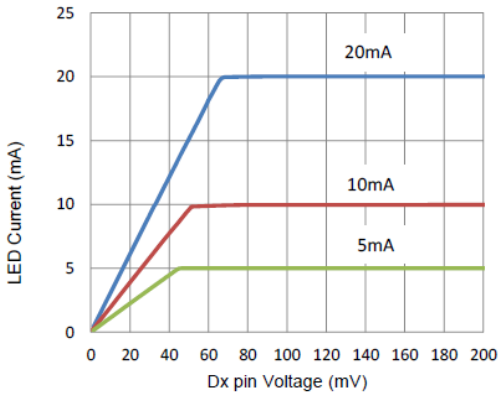
Typical Characteristics

V_{IN}=3.6V, C1=1μF, T_A=25°C (Unless otherwise specified)

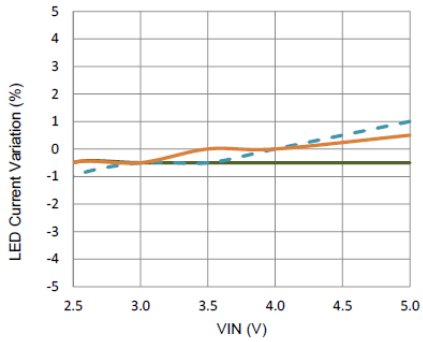
LED Current Regulation (at 20mA)



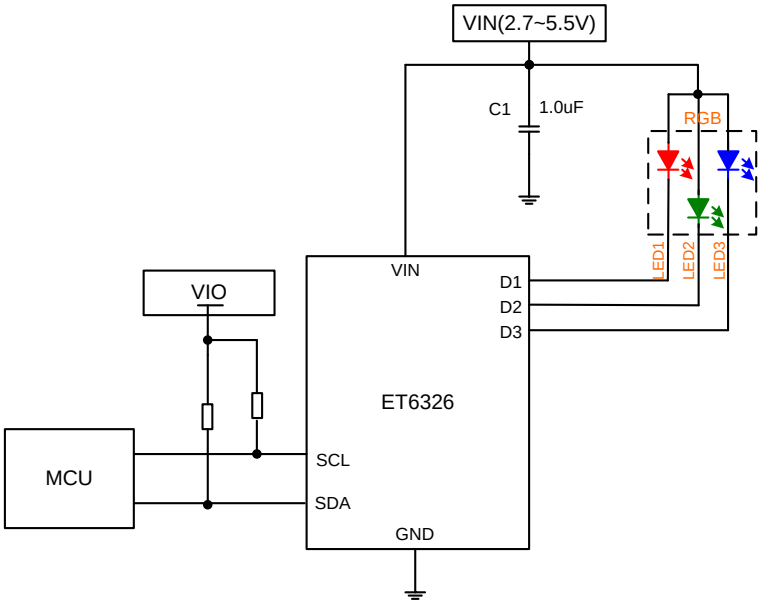
Dropout Voltage



LED Current Matching (2mA per channel)

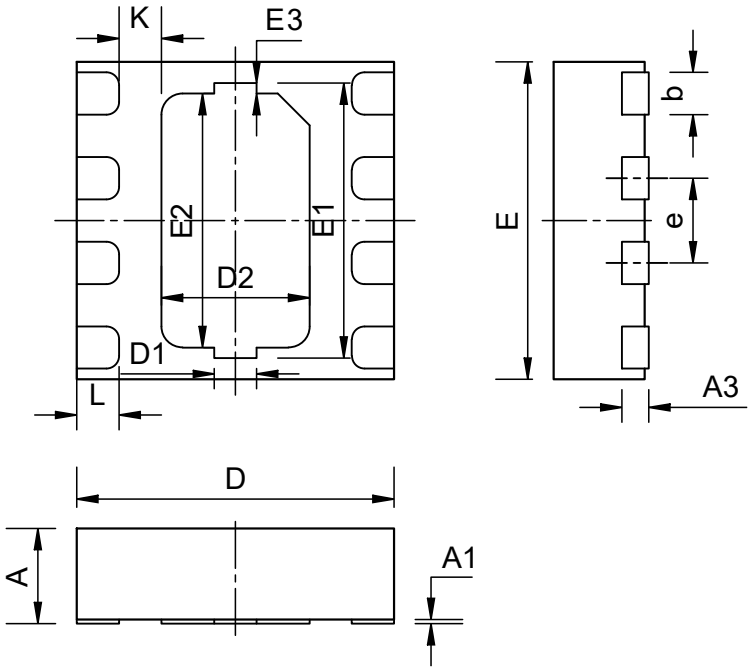


Application Circuits



Package Dimension

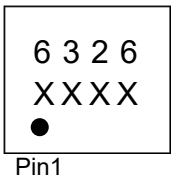
DFN8



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.40	0.45	0.50
A1	0	0.02	0.05
A3		0.127REF	
b	0.15	0.20	0.25
D	1.45	1.50	1.55
D1		0.20REF	
D2	0.60	0.70	0.80
E	1.45	1.50	1.55
E1	1.25	1.30	1.35
E2	1.10	1.20	1.30
E3		0.05REF	
e		0.40BSC	
L	0.15	0.20	0.25
K	0.20	--	--

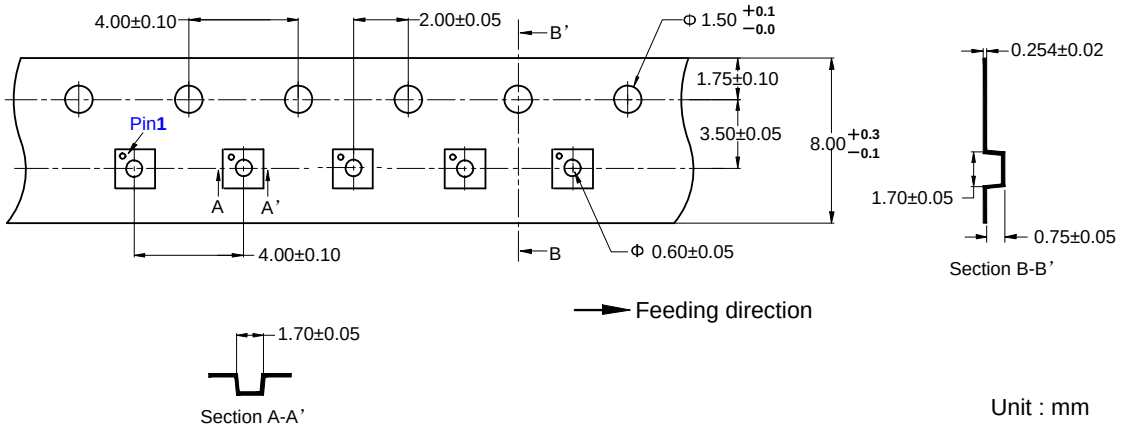
Marking Information



6326 - Part Number

XXXX - Tracking Number

Tape Information



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2016-06-06	Original version	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.1	2017-09-27	Add MSL1	Shi Liang Jun	Shi Liang Jun	Zhu Jun Li
1.2	2022-09-30	Update Typeset	Tianqh Shibo	Shi Liang Jun	Zhu Jun Li
1.3	2023-06-16	Add marking tape	Tianqh Shibo	Shibo	Liujy