A Very Low-Dropout Regulator with 3A Load Current

General Description

The ET5C108 is a CMOS-based very low dropout voltage regulator, offering 3A with NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The device provides very stable, accurate output voltage with high ripple rejection and excellent full load transient performance. The ET5C108 consist of an accurate 0.8V internal voltage-reference, an error amplifier, an under-voltage lock-out (UVLO) block, an output current limit circuit and a thermal-shutdown circuit.

The ET5C108 can set the output voltage through external resistor divider with FB pin. With the SS pin, user can fulfill the soft-start function through the external capacitor. A Power Good pin (PG) is also available. The ET5C108 is offered in DFN10(3mm×3mm) package.

Features

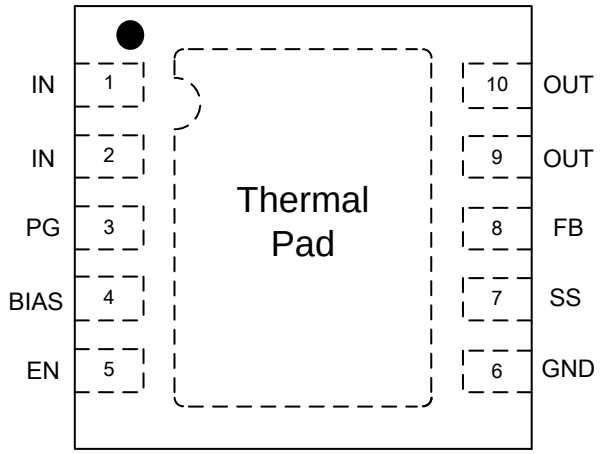
- Output Current:3.0A
- Wide Input Voltage Range: 0.8V to 5.5V
- Wide BIAS Voltage Range: 2.2V to 5.5V
- Output Voltage Range: 0.8V to 3.6V(externally set)
- Dropout Voltage: 95mV at 3A
- Open Drain Power Good (PG) Output
- Excellent Transient Response
- Built-in Soft-start Function
- Built-in Current Limit and Thermal Shutdown Protection
- Package Information:

Part No.	Package	MSL
ET5C108	DFN10 (3mm×3mm×0.75mm,0.5 pitch)	Level 1

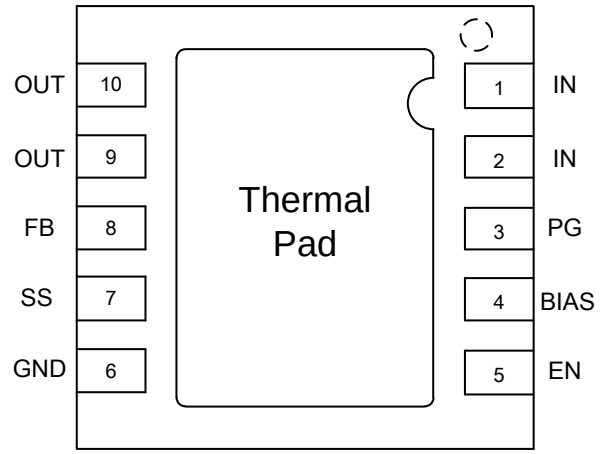
Applications

- Telecom Industrial and Consumer Equipment
- FPGA, DSP and Logic Power Supplies
- Switching Power Supply Post Regulation
- Specific Start−up Time or Sequencing Requirement Applications

Pin Configuration



Top View

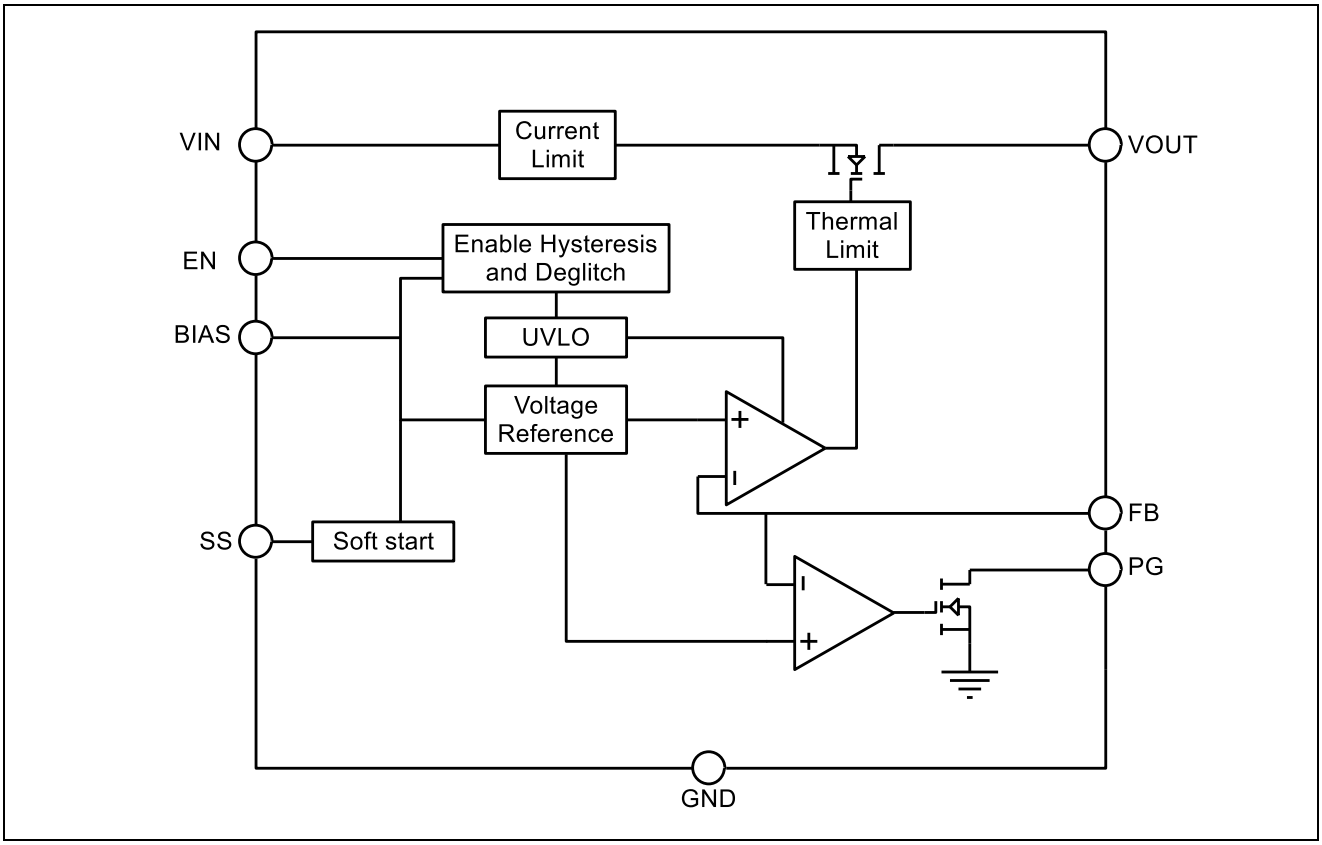


Bottom View

Pin Function

Pin Name	Symbol	Pin Description
1, 2	IN	Unregulated input voltage pin.
3	PG	Power-Good pin is an open-drain, active-high output that indicates the status of V_{OUT}. A pull-up resistor form 10kΩ to 1MΩ should be connected to a supply and the PG pin can be left floating alternatively.
4	BIAS	Input voltage for internal control circuits.
5	EN	Enable pin. Active high and this pin must not be left floating.
6	GND	Ground pin.
7	SS	Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left floating, the regulator output soft-start ramp time is typically 200μs.
8	FB	Connecting to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
9, 10	OUT	Regulated output voltage.
Thermal Pad		Should be soldered to the ground plane for increasing thermal performance.

Block Diagram



Functional Description

The ET5C108 dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the internal control circuit is powered by the BIAS voltage.

The use of an NMOS pass transistor offers several advantages in applications. Comparing to PMOS topology devices, the output capacitor has reduced impact on loop stability. The dropout voltage between V_{IN} and V_{OUT} can be very low compared with standard PMOS regulators in very low V_{IN} applications.

The ET5C108 offers programmable smooth monotonic start-up. The controlled voltage rising limits the inrush current. The soft-start time is programmable by external C_{SS} capacitor value.

The Enable (EN) input is equipped with internal hysteresis and deglitch filter. An Open Drain Power Good (PG) output is available for V_{OUT} monitoring. When V_{OUT} exceeds the PG threshold, the PG pin goes into high-impedance state. When is below this threshold, the PG pin is set to low-impedance state.

The ET5C108 is an adjustable linear regulator. As shown in application circuit, the required output voltage can be adjusted by two external resistors with FB pin.

Dropout Voltage

There are two Dropout voltages specified.

Firstly, the V_{IN} Dropout voltage is the voltage difference between V_{IN} and V_{OUT} when V_{OUT} starts to decrease by 2%. V_{BIAS} is set to high enough, referring to the specific value in the Electrical Characteristics table.

Secondly, the V_{BIAS} dropout voltage is the voltage difference between V_{BIAS} and V_{OUT} when V_{IN} and V_{BIAS} pins are joined together and V_{OUT} starts to decrease by 2%.

Input and Output Capacitors

The device is designed to be stable for all available types and values of output capacitors ≥ 2.2μF. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range.

In applications where no low input supply impedance is available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as an example) the recommended C_{IN} and C_{BIAS} value is 1μF or greater.

Ceramic or other low ESR capacitors are recommended. For the best performance all capacitors should be connected to the ET5C108 respective pins directly in the device PCB copper layer, not through via having not negligible impedance.

Enable Operation

The ET5C108 is turned on by setting the enable pin to High. The threshold limits are covered in the electrical characteristics table in this datasheet. When the enable function is not to be used then the pin should be connected to V_{IN} or V_{BIAS}.

Output Noise

When the ET5C108 device reaches the end of the Soft−Start cycle, the Soft Start capacitor will be switched to be a noise filtering capacitor.

Output Voltage Adjust

The output voltage can be adjusted from 0.8 V to 3.6 V using resistors divider between the output and the FB input. The output voltage can be calculated by:

$$\mathbf{V_{OUT}=0.8\times(1+R1/R2)}$$

For example: choose R_1=2.49kΩ, R_2=4.99kΩ, V_{OUT}=1.2V

Programmable Soft−Start

The Soft-Start ramp time depends on the Soft Start charging current I_{SS}, Soft-Start capacitor value C_{SS} and internal reference voltage V_{REF}.

The Soft – Start time can be calculated by:

$$\mathbf{t_{ss} = C_{SS} \times (V_{REF} / I_{SS})\ [s,F,V,A]}$$

or practically by:

$$\mathbf{t_{SS} = C_{SS} \times 0.8V / 0.45uA = C_{SS} \times 1.78}$$

Where t_{SS} is Soft−Start time in ms.C_{SS} is Soft−Start capacitor value in nF.

For example: t_{SS} is 10ms when C_{SS} is 5.6nF.

Note: The maximal recommended value of C_{SS} capacitor is 15nF. For higher C_{SS} values the capacitor full discharging before new Soft-Start cycle is not guaranteed.

Current Limitation

When output current of V_{OUT} pin is higher than current limit threshold or the V_{OUT} pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage.

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +155° C, allowing the device to cool down. When the junction temperature reduces to approximately +125° C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage Range	-0.3 to +6	V
V_{BIAS}	Input Voltage Range	-0.3 to +6	V
V_{EN}	Enable Voltage Range	-0.3 to +6	V
V_{PG}	Power-Good Pin Voltage Range	-0.3 to +6	V
I_{PG}	PG Sink Current	0 to +1.5	mA
V_{SS}	SS Pin Voltage Range	-0.3 to +6	V
V_{FB}	Feedback Pin Voltage Range	-0.3 to +6	V
V_{OUT}	Output Voltage Range	-0.3 to (V_{IN} + 0.3) ≤ 6	V
P_D	Continuous Total Power Dissipation	2.5	W
T_J	Maximum Junction Temperature	+150	°C
T_{STG}	Storage Junction Temperature Range	-65 to +150	°C

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{IN}	Input voltage range	V_{OUT} +V_{DO} to 5.5	V
V_{BIAS}	Bias pin voltage range	2.2 to 5.5	V
T_A	Operating Ambient Temperature	-40 to +85	ºC

Electrical Characteristics

V_{EN}=1.1V, V_{IN}=V_{OUT}+0.3V, V_{BIAS}=5.0V, C_{BIAS}=C_{IN}=1μF, C_{OUT}=10μF, I_{OUT}=50mA, T_A=-40°C to +85°C, unless otherwise noted. Typical values are at T_A=+25°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage Range	V_{IN}(1)		V_{OUT} +V_{DO}		5.5	V
V_{BIAS} Voltage Range	V_{BIAS}		2.2		5.5	V
Under-voltage Lock-out	V_{UVLO}	V_{BIAS} Rising	1.2	1.6	1.9	V
		Hysteresis		0.2		
Internal Reference	V_{REF}	T_A=+25°C		0.8		V
Output Voltage Range	V_{OUT}	V_{IN}= 5V,I_{OU}=1.5A,V_{BIAS}=5V	V_{REF}		3.6	V
Output Accuracy		2.97V ≤V_{BIAS}≤5.25V, V_{OUT}+1.62V≤V_{BIAS}, 50mA≤I_{OUT}≤3.0A	-1.0		+1.0	%
Line Regulation	Reg_{LINE}	$V_{OUT(NOM)}$+0.3≤V_{IN}≤5.5V		0.01		%/V
Load Regulation	Reg_{LOAD}	0mA≤I_{OUT}≤50mA		0.005		%/mA
		50mA ≤I_{OUT}≤3.0A		0.03		%/A
V_{IN} Dropout Voltage	V_{DROP}(2)	I_{OUT}=3.0A, V_{BIAS}–$V_{OUT(NOM)}$≥1.62V		95	160	mV
V_{BIAS} Dropout Voltage		I_{OUT}=3.0A, V_{IN}=V_{OUT}+0.3V		1.12	1.5	V
Current Limit	I_{LIM}	V_{OUT}=80% x$V_{OUT(NOM)}$	3.8	4.6	7	A
V_{BIAS} Current	I_{BIAS}	0mA ≤I_{OUT}≤3.0A		1.3	2	mA
V_{BIAS} Shutdown Supply Current	I_{SHDN}	V_{EN}=0 V		0.3	2	μA
V_{IN} to V_{OUT} Ripple rejection	PSRR	1kHz,I_{OUT}=1.5A, V_{IN}=1.5V,V_{OUT}=1.2V		75		dB
V_{BIAS} to V_{OUT} Ripple rejection		10kHz, I_{OUT}=1.5A, V_{IN}=1.5V,V_{OUT}=1.2V		78		dB
Output Noise Voltage	e_N(3)	100 Hz to 100 kHz, I_{OUT}=3 A,C_{SS}=1.0nF		18× V_{OUT}		μVrms
%V_{OUT} Droop During Load Transient	V_{TRLD}(3)	I_{OUT}=50mA to 3.0 A at 1 A/μs,C_{OUT}=10μF, V_{OUT}=1.2 V		±2		%V_{OUT}
Minimum Startup Time	t_{ON}	I_{OUT}=1.5A,C_{SS}=open		200		μs
Soft-start Charging Current	I_{SS}	V_{SS}=0.4V		0.45		μA
Enable Input High Level	V_{ENH}		1.1		5.5	V
Enable Input Low Level	V_{ENL}		0		0.4	V
Enable Pin Hysteresis	$V_{EN,HYS}$			100		mV
Enable Pin Deglitch Time	$t_{EN,DG}$			20		μs

Electrical Characteristics(Continued)

V_{EN}=1.1V,V_{IN}=V_{OUT}+0.3V,V_{BIAS}=5.0V,C_{BIAS}=C_{IN}=1μF,C_{OUT}=10μF,I_{OUT}=50mA,T_A=-40°C to +85°C,unless otherwise noted. Typical values are at T_A=+25°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Enable Pin Current	I_{EN}	V_{EN}=5V		0.3	1	μA
PG Threshold	V_{TH}	V_{OUT} decreasing	86.5	90	93.5	%V_{OUT}
PG Hysteresis	V_{HYS}			3		%V_{OUT}
PG Output Low Voltage	V_{PGL}	I_{PG}=1mA (sinking),V_{OUT}<V_{TH}			0.3	V
PG Leakage Current	$I_{PG,LKG}$	V_{PG}=5V,V_{OUT}>V_{TH}		0.03	1	μA
Thermal Shutdown Temperature	T_{TSD}			+155		°C
Thermal Shutdown Released Temperature	T_{TSR}			+125		°C

Notes:

1: The maximum input voltage should take into account the maximum power consumption ($P_{D(MAX)}$).The calculation formula is as follows:

$$\mathbf{P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT}}$$

The maximum power consumption of the circuit is 2500mW.

$$\mathbf{V_{IN(MAX)} = 2500mW / I_{OUT} + V_{OUT}}$$

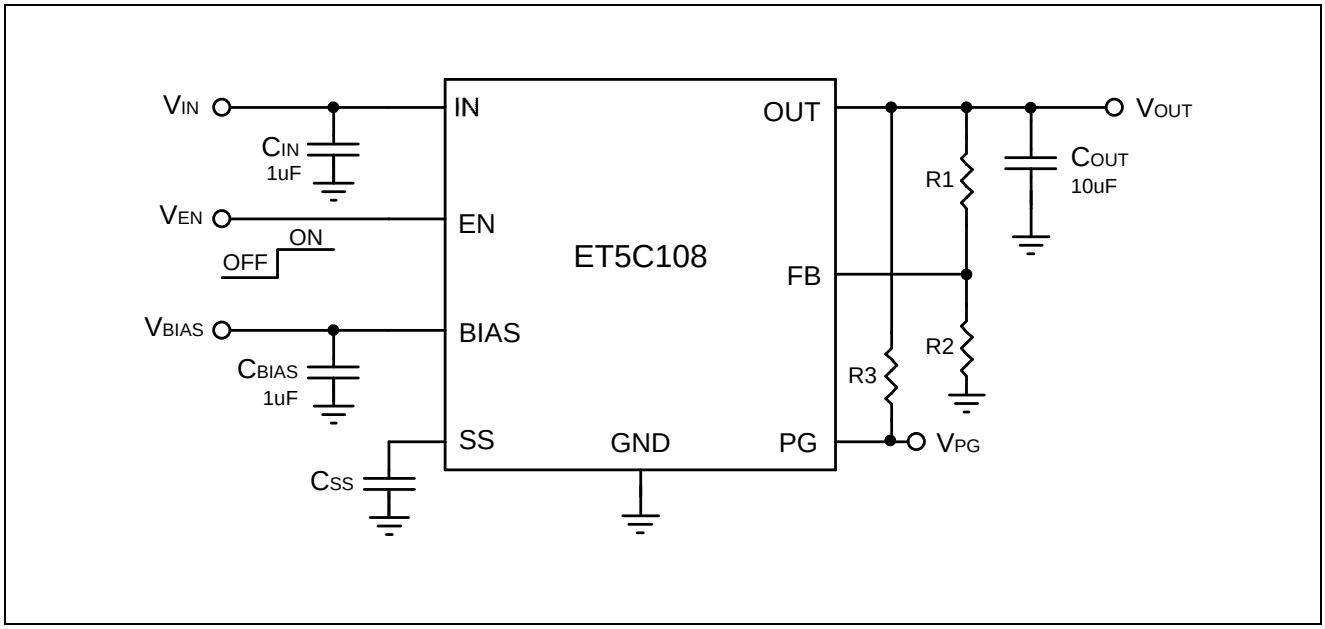
For example:

If V_{OUT}= 1.2V, I_{OUT}=2500mA, The maximum input voltage is $V_{IN(MAX)}$=2500mW / 2500mA+1.2=2.2V

2: V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET} +$V_{DROPMAX}$ with output current.

3: Guaranteed by design and characterization. not a FT item.

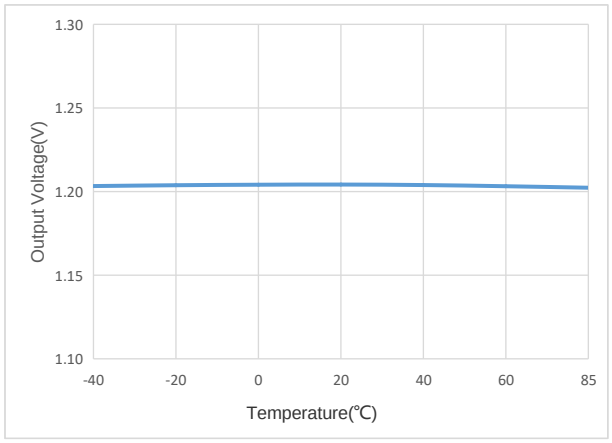
Application Circuits



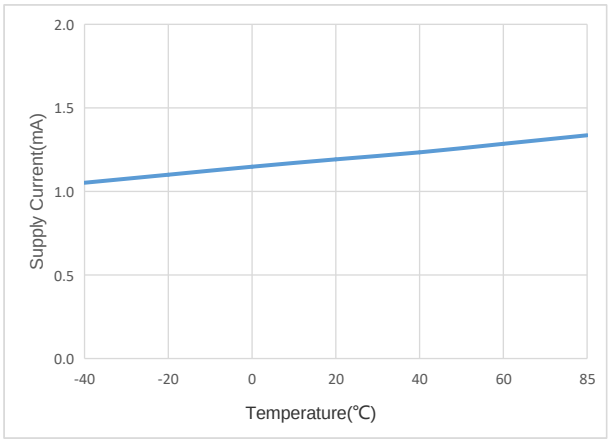
Note*: V_{OUT} = 0.8×(1+R1/R2),R3 should be from 10KΩ to 1MΩ.

Typical Characteristics

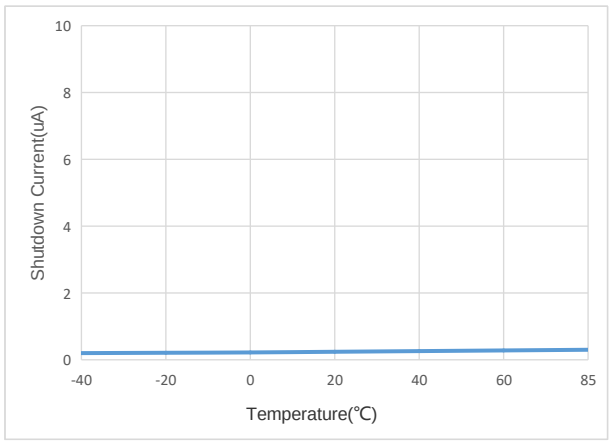
(V_{OUT}=1.2V,V_{IN}=1.5V,V_{BIAS}=5.0V,C_{IN}=C_{BIAS}=1μF,C_{OUT}=10μF,T_A= -40ºC~+85ºC)



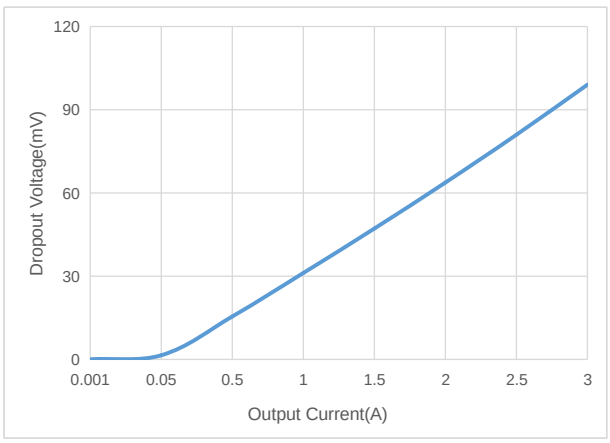
Output Voltage VS Temperature



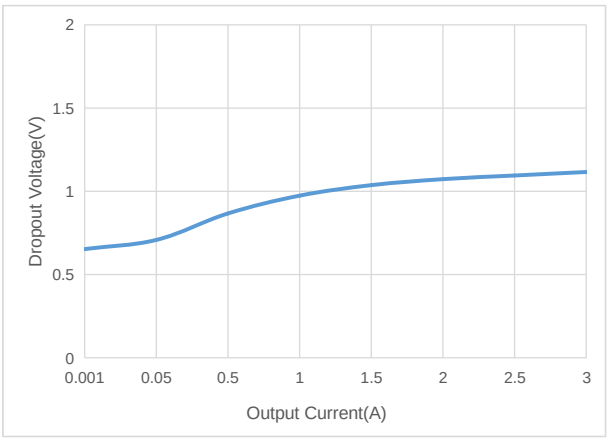
Supply Current VS Temperature



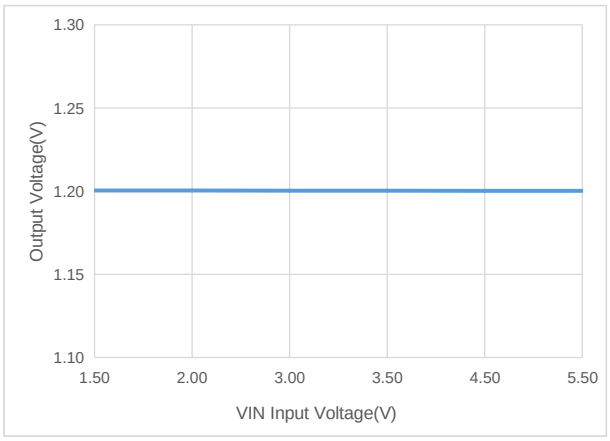
Shutdown Current VS Temperature



VIN Dropout Voltage VS Output Current



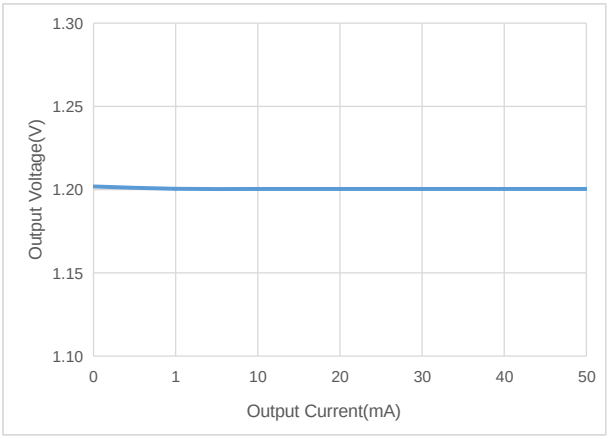
VBIAS Dropout Voltage VS Output Current



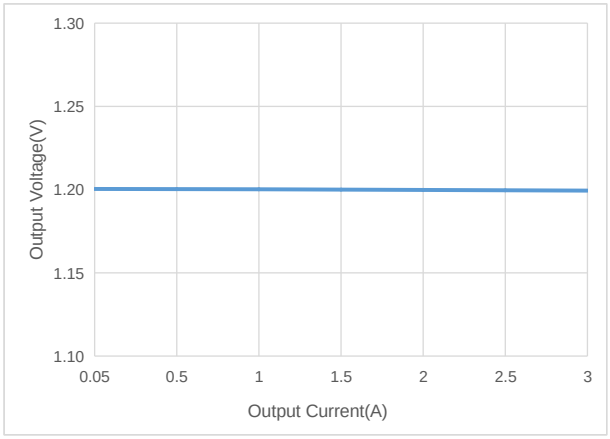
Output Voltage VS VIN Input Voltage

Typical Characteristics(Continued)

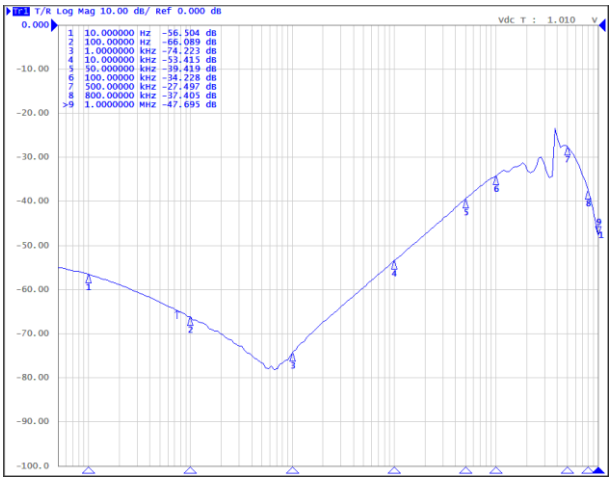
(V_{OUT}=1.2V,V_{IN}=1.5V,V_{BIAS}=5.0V,C_{IN}=C_{BIAS}=1μF,C_{OUT}=10μF,T_A= -40ºC~+85ºC)



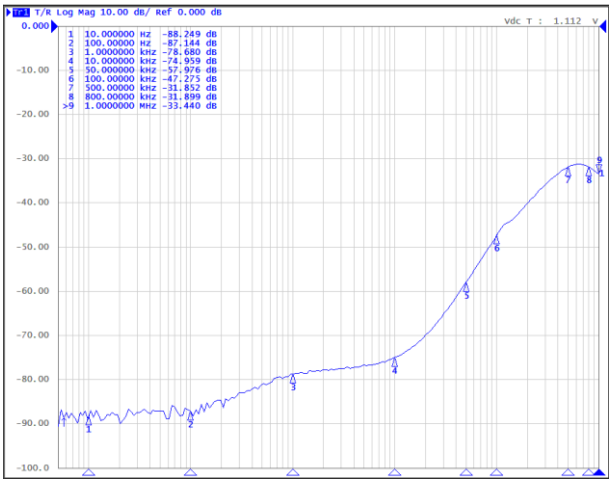
Output Voltage VS Output Current



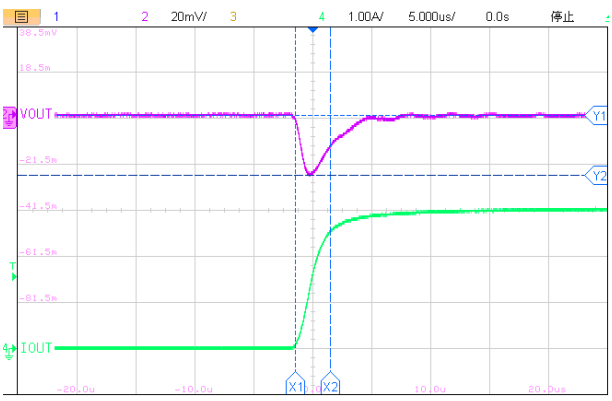
Output Voltage VS Output Current



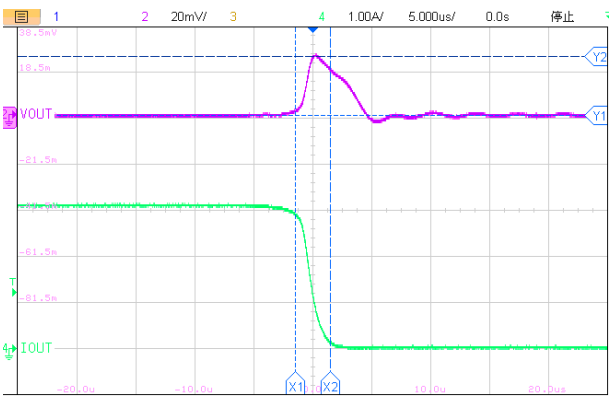
VIN PSRR



VBIAS PSRR



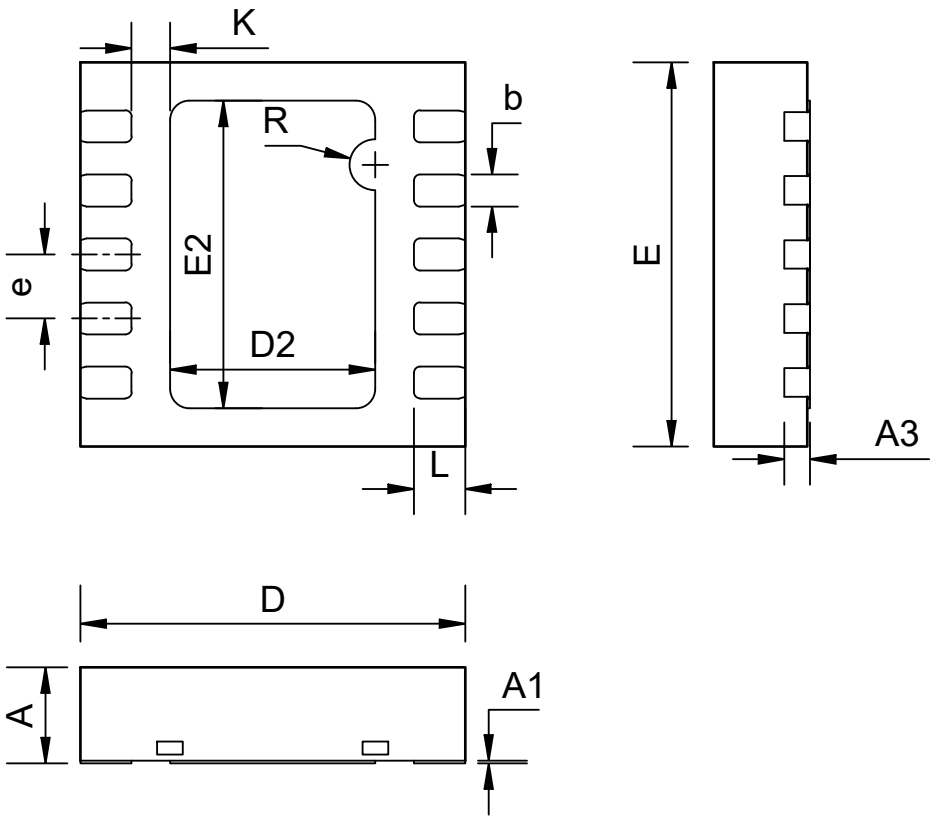
Load Transient(50mA~3A 1A/us)



Load Transient(3A~50mA 1A/us)

Package Dimension

DFN10(3x3)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.55	1.65	1.75
E2	2.30	2.40	2.50
e	0.40	0.50	0.60
K	0.175	0.275	0.375
L	0.35	0.40	0.45
R		0.20REF	

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2019-05-20	Preliminary Version, development stage	Chenh	Chenh	Liujy
1.1	2019-12-11	Update EC table according to EVB test	Chenh	Chenh	Liujy
1.2	2023-3-15	Update Typeset	Tugz	Chenh	Liujy